PAMS Technical Documentation
NSW–1 Series Transceivers

Chapter 3

System Module UT4S

Original 10/98

MODIFICATION RECORD SHEET

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CONTENTS

Schematic Diagrams:

Transceiver NSW-1

Introduction

The NSW-1 is a dualband/dualmode radio transceiver unit for the US TDMA 800/1900 cellular mobile phone networks. The transceiver is a true 3 V transceiver.

The transceiver consists of a System/RF module (UT4S), an User interface module (UE4S) and assembly parts.

The purpose of the baseband module is to control the phone and process audio signals to and from the RF. The module also controls the user interface.

The Dual-band RF-module is capable of seamless operation between 800 MHz and 1900 MHz bands. In practise this means capability for cross-band hand-offs and maca-measurements.

The transceiver has full graphic display and two soft key based user interface.

The antenna is a fixed helix. External antenna connection is provided by rear RF connector

Functional Description

There are five different operation modes:

1. power off mode
2. sleep mode
3. active mode
4. charge mode
5. local mode

In the (1) power off mode only the circuits needed for power up are supplied.

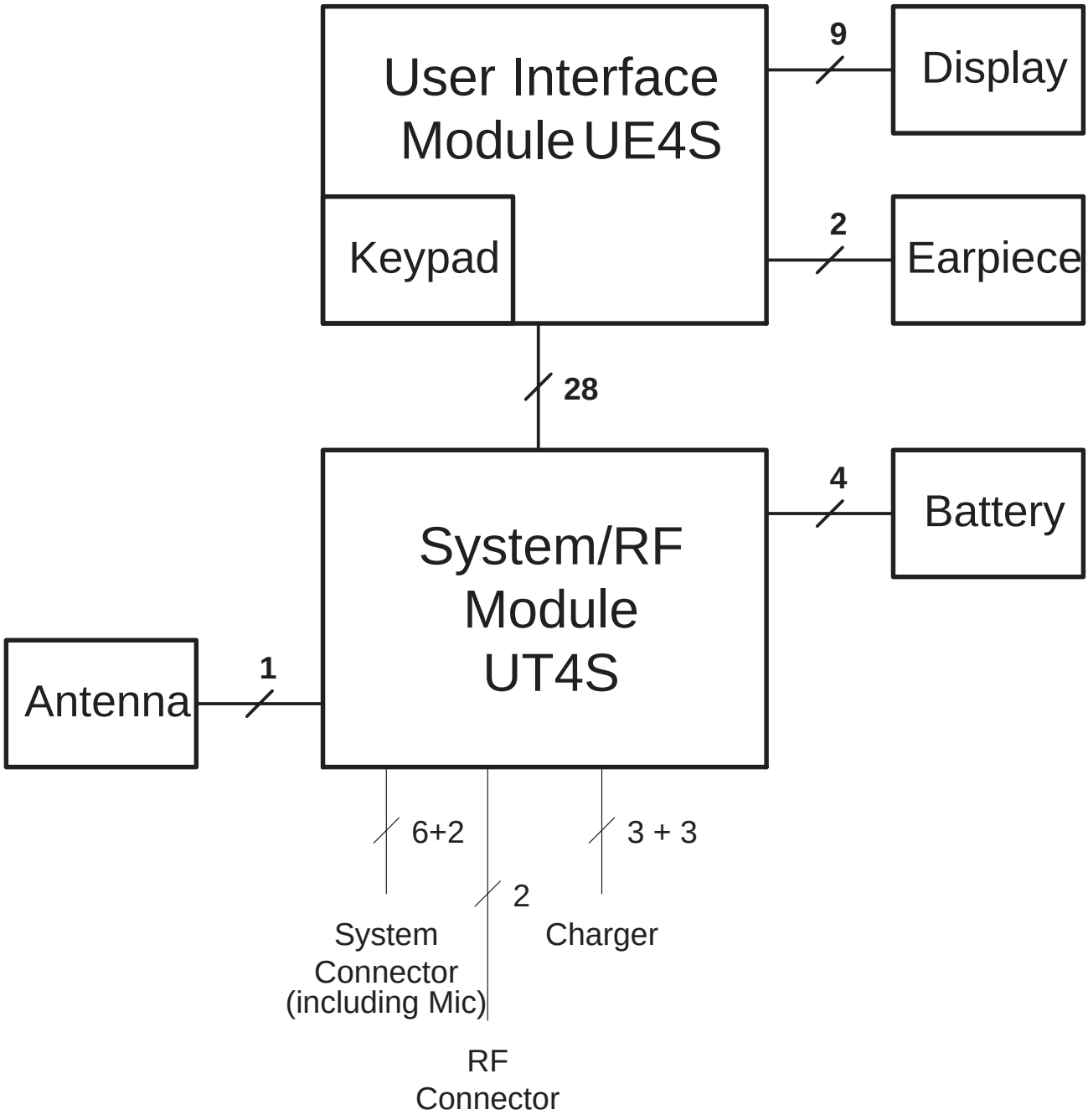
In the (2) sleep mode all circuits are powered down and only sleep clock is running.

In the (3) active mode all the circuits are supplied with power although some parts might be in the idle state part of the time.

The (4) charge mode is effective in parallel with all previous modes. The charge mode itself consists of two different states, i.e. the charge and the maintenance mode.

The (5) local mode is used for alignment and testing.

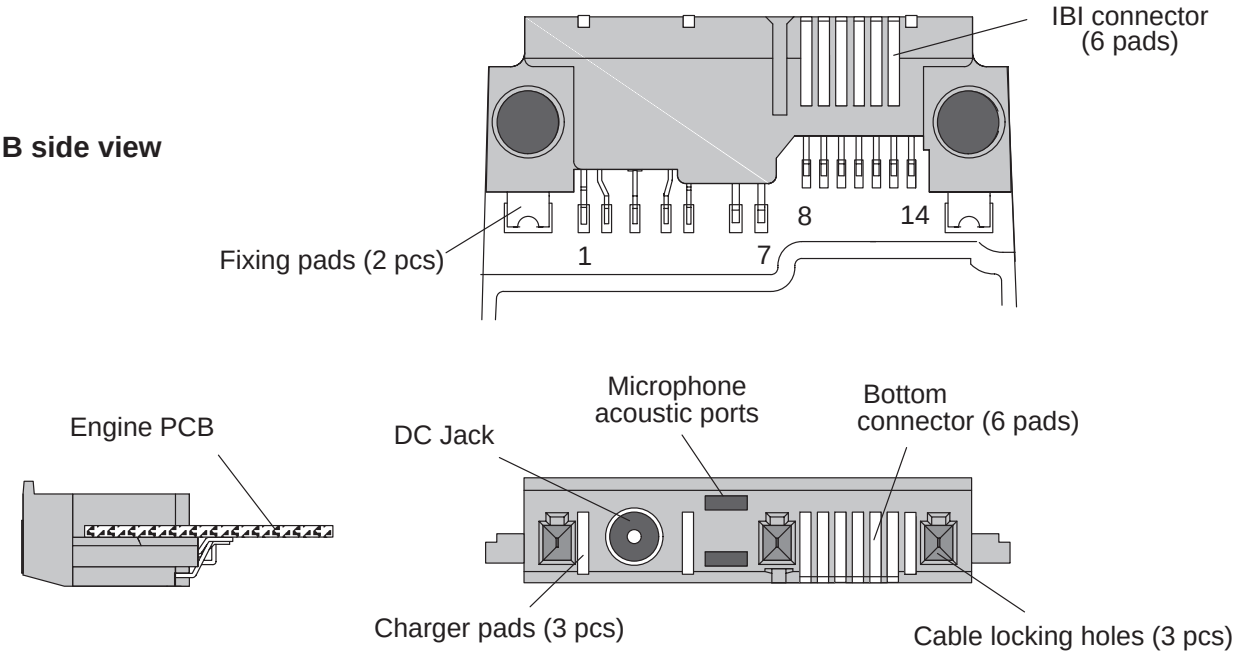
Interconnection Diagram



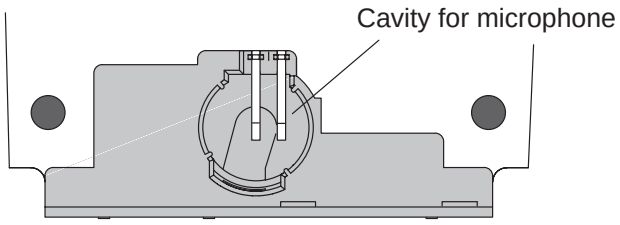
System Module

External and Internal Connectors

B side view



A side view

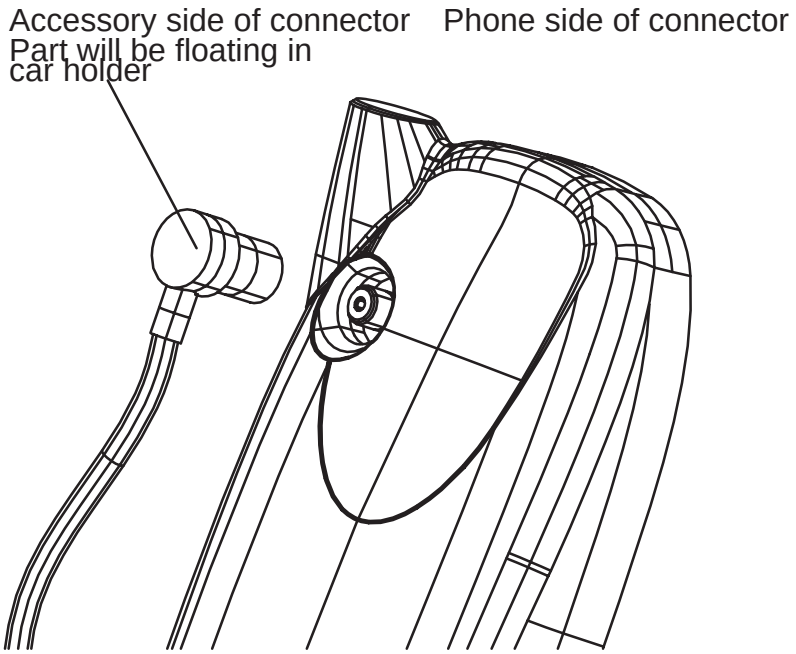


System Connector Signals

Pin	Name	Function	Description
1	V_IN	Bottom charger contacts	Charging voltage.
2	L_GND	DC Jack	Logic and charging ground.
3	V_IN	DC Jack	Charging voltage.
4	CHRG_CTRL	DC Jack	Charger control.
5	CHRG_CTRL	Bottom charger contacts	Charger control.
6	MICP	Microphone	Microphone signal, positive node.
7	MICN	Microphone	Microphone signal, negative node.
8	XMIC	Bottom & IBI connectors	Analog audio input.
9	SGND	Bottom & IBI connectors	Audio signal ground.
10	XEAR	Bottom & IBI connectors	Analog audio output.
11	MBUS	Bottom & IBI connectors	Bidirectional serial bus.
12	FBUS_RX	Bottom & IBI connectors	Serial data in.
13	FBUS_TX	Bottom & IBI connectors	Serial data out.
14	L_GND	Bottom charger contacts	Logic and charging ground.

RF-Connector

The RF-connector is needed to utilize the external antenna with Car Cradle. The RF-connector is located on the back side of the transceiver on the top section. The connector is plug type connector with special mechanical switching.



Battery Contacts

Pin	Name	Function	Description
1	BVOLT	Battery voltage	Battery voltage
2	BSI	Battery Size Indicator	Input voltage
3	BTEMP	Battery temperature indication Phone power up Battery power up PWM to VIBRA BATTERY	Input voltage Input voltage Output voltage PWM output signal frequency
4	BGND		Ground

Operating Conditions

Environmental condition	Ambient temperature	Notes
Normal operation conditions	+7 ^{o}C ... +40 ^{o}C	Specifications fulfilled and fast charging possible
Extreme operation conditions	-10 ^{o}C ... +40 ^{o}C	Specifications fulfilled
Reduced performance conditions	+40 ^{o}C ... +60 ^{o}C	Operational only for short periods
Intermittent operation conditions	-40 ^{o}C ... -30 ^{o}C and +60 ^{o}C ... +80 ^{o}C	Operation maybe not possible but attempt to operate will not damage the phone
Cessation of operation	<-40 ^{o}C and >80 ^{o}C	No storage or operation is allowed
Long term storage conditions	0 ^{o}C ... +40 ^{o}C	Battery only up to +30 ^{o}C !
Short term storage, max. 24 h	-40 ^{o}C ... +80 ^{o}C	Cumulative for life-time of battery
LCD operation	-30 ^{o}C ... +70 ^{o}C	Functions are delayed in low temperatures

Functional Description

The UT4S engine consist of a Baseband/RF module with connections to a separate User Interface module. The baseband and RF submodules are interconnected by the PCB wiring. The engine can be connected to accessories via a bottom system connector and an Intelligent Battery Interface (IBI) connector.

RF Submodule

The RF submodule receives and demodulates radio frequency signals from a base station and transmits modulated RF signals to a base station. It consists of functional submodules:

– Receiver,
– Frequency Synthesizer
– Transmitter

The RF submodule can further be divided into lower band and upper band functions.

Baseband submodule

The Baseband module comprises audio, control, signal processing and power supply functions. It consists of the following functional submodules:

– CTRLU (Control Unit; MCU, DSP, logic and memories),
– PWRU (Power Supply; regulators and charging)
– AUDIO_RF (audio coding, RF–BB interface).

Modes of Operation

The UT4U/UT4RM operates in seven cellular modes and a local mode for service:

– Analog Control Channel (ACCH) 800 MHz Mode,
– Analog Voice Channel (AVCH) 800 MHz Mode,
– Digital Control Channel (DCCH) 800 MHz Mode,
– Digital Traffic Channel (DTCH) 800 MHz Mode,
– Digital Control Channel (DCCH) 1900 MHz Mode,
– Digital Traffic Channel (DTCH) 1900 MHz Mode,
– Out of Range (OOR) Mode,
– Locals mode, used by Production and After Sales.

Analog Control Channel (ACCH) Mode

On analog control channel mode the phone receives continuous signalling messages on Forward Control Channel (FOCC) from the base station, being

most of the time in IDLE mode. Only the receiver part is on. The phone scans the preferred dedicated control channels to find and lock to the strongest channel for reading information from this control channel.

DSP is not used on ACCH (it stays in sleep mode), except during channel scanning for loading the synthesizers.

As a separate sleep clock is used, also the VCTCXO can be turned off periodically with the RF parts. Only the sleep clock and necessary timers in the MCU are operational.

When registration is demanded the phone sends (TX on) its' data on Reverse Control Channel (RECC) to the base station. The phone's location is updated in the switching office.

If a call is initiated, either by the user or the base station, the phone moves to the allocated analog voice channel or digital traffic channel depending on the orders by the base station.

Analog Voice Channel (AVCH) Mode

The phone receives and transmits analog audio signal. All circuitry is powered on (except the receiver parts used only in digital modes). DSP does the audio processing and in Hands Free mode also performs the echo–cancellation and HF algorithms. The COBBA IC makes A/D conversion for the MIC signal, and D/A conversion for the EAR signal.

With audio signal also the Supervisory Audio Tone (SAT) is being received from the base station. The SAT frequency can be 5970 Hz, 6000Hz or 6030 Hz, defined by the base station. The DSP phase lock loop locks to the SAT, detects if the frequency is the expected one and examines the signal quality. DSP reports SAT quality figures regularly to the MCU. The received SAT signal is transmitted back (transponded) to the base station.

The base station can send signalling messages on Forward Voice Channel (FVC) to the phone, by replacing the audio with a burst of Wide Band Data (WBD). These are typically hand–off or power level messages. The RX modem in System Logic receives the signalling message burst and gives an interrupt to the MCU for reading the data. MCU gives a message to DSP to mute the audio path during the burst. MCU can acknowledge the messages on Reverse Voice Channel (RVC), where DSP sends the WBD to transmitter RF.

Digital Control Channel (DCCH) 800 MHz Mode

On digital control channel (DCCH) DSP receives the paging information from the Paging channels and sends the messages to MCU for processing.

Each Hyperframe (HFC) comprises two Superframes (SF), the Primary (p) and the Secondary (s) paging frame. The assigned Page Frame Class (PFC) defines the frames which must be received, and thus defines when the receiver must be on.

The phone is in sleep mode between the received time slots. The sleep clock timer is set and the MCU, DSP and RF parts (including VCTCXO) are powered down. Only the sleep clock and the respective timers are running.

From DCCH the phone may be ordered to analog control channel or to analog or digital traffic channel.

Digital Traffic Channel (DTCH) 800 MHz Mode

Digital Voice Channel (S–DTCH)

On digital voice channel mode the DSP processes the speech signal in 20 ms time slots. The DSP performs the speech and channel functions in time shared fashion and is in sleep mode whenever possible. The RX and TX parts are powered on and off according to the slot timing. The MCU is waken up mainly by DSP, when there is signalling information for the Cellular Software.

Digital Data Channel (D–DTCH)

In Digital Data Channel Mode audio processing is not needed and the audio circuitry can be shut down. Otherwise the mode is similar to Digital Voice Channel Mode.

Digital Control Channel (DCCH) 1900 MHz Mode

Similar to Digital Control Channel 800 MHz Mode.

Digital Traffic Channel (DTCH) 1900 MHz Mode

Similar to Digital Traffic Channel 800 MHz Modes.

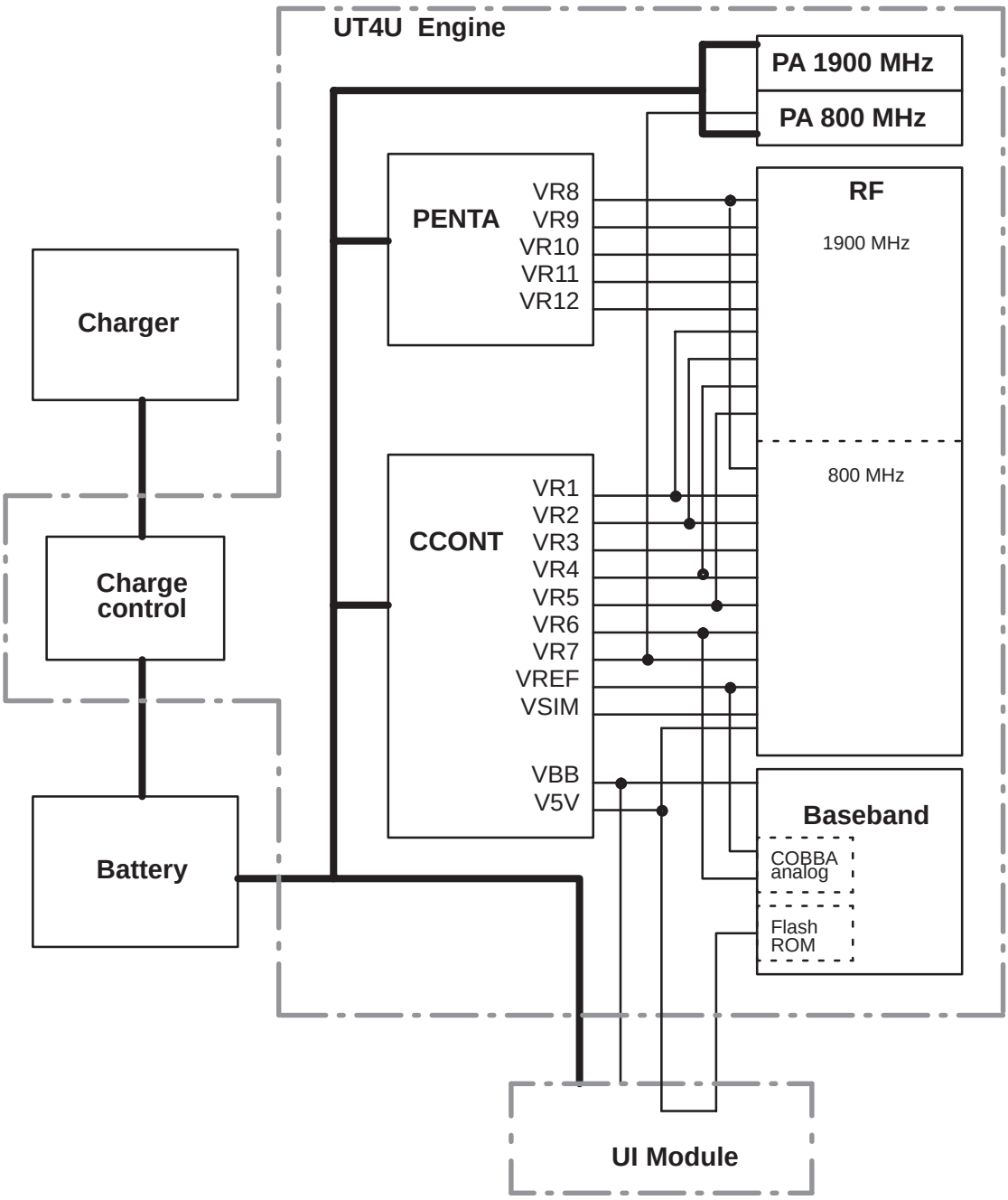
Out of Range (OOR) Mode

If the phone can’t find a signal from the base station on any control channel (analog or digital) it can go into OOR mode for power saving. All RF circuits are powered down and the baseband circuits in a low power mode, the VCTCXO stopped and only the sleep clock running. After a programmable timer in the MCU has elapsed the phone turns the receiver on and tries to receive signalling data from a base station. If it succeeds, the phone goes to standby mode on analog or digital control channel. If the connection can not be established the phone returns to OOR mode until the timer elapses again.

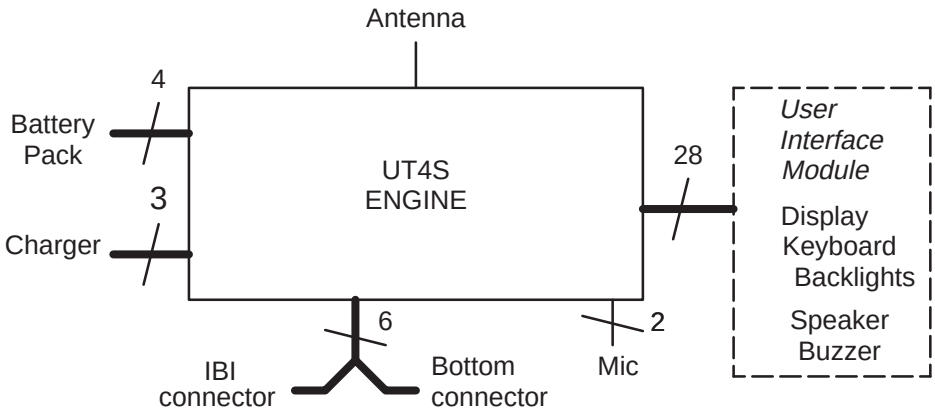
Locals Mode

Locals mode is used for testing purposes. The Cellular Software is stopped (no signalling to base station), and the phone is controlled by MBUS/FBUS messages by the controlling PC.

Power Distribution Diagram



External interfaces



Accessories

Connector Name	Notes
Bottom connector + IBI connector	Includes control, data, charging and audio signals
UI–connector	includes keyboard, backlight, display,buzzer, call led, and earpiece signals
Battery connector	VBAT, GND, BTYPE, BTEMP
RF–interface	Connection

Signals between baseband and User Interface section

The User interface section is implemented on a separate UI board, which connects to the engine board with a board to board spring connector.

User Interface module connection

The User interface section comprises the keyboard with keyboard backlights, display module with display lights, an earphone and a buzzer.

Earphone

The internal earphone is connected to the UI board by means of mounting springs . The low impedance, dynamic type earphone is connected to a differential output in the COBBA audio codec. The voltage level at each output is given as reference to ground. The earphone levels are given to 32 ohm load.

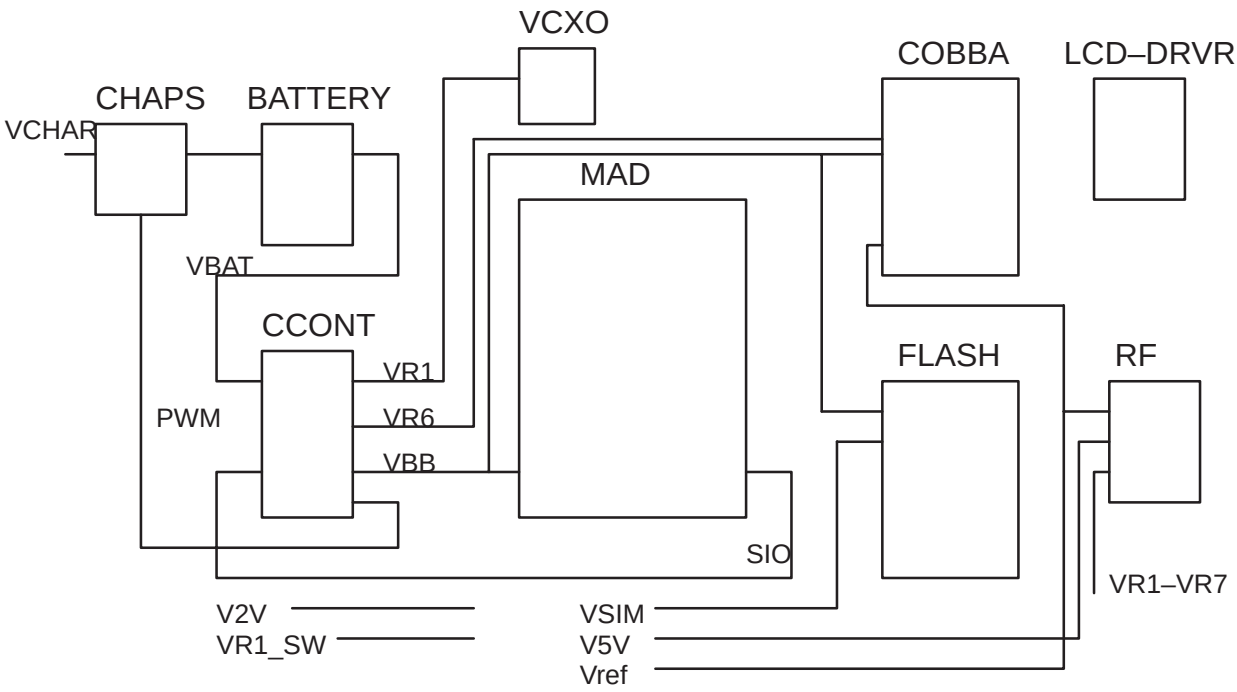
Buzzer

Alerting tones and/or melodies as a signal of an incoming call are generated with a buzzer that is controlled with a PWM signal by the MAD. The buzzer is a SMD device placed on the UI board.

Baseband Module

Power Distribution

In normal operation the baseband is powered from the phone‘s battery. The battery consists of three Nickel-cells. There is also a possibility to use batteries consisting of one Lithium-cell. An external charger can be used for recharging the battery and supplying power to the phone. The charger can be either so called fast charger, which can deliver supply current up to 850 mA or a standard charger that can deliver around 300 mA.



Battery voltage VBAT is connected to the CCONT which regulates all the supply voltages VBB, VR1–VR7, V2V, VR1_SW, VSIM and V5V. VR7 is divided into VR7 and VR7_bias. VR7_bias is for PA in RF analog mode to change its operation point to optimum for nonlinear FM modulation. CCONT enables automatically VR1, VBB, V2V_core, VR6 and Vref in power–up.

VBB is used as baseband power supply for all digital parts, and it is constantly on whenever the phone is powered up. There is also another Baseband voltage, V2V, which is reserved for later version of MAD circuit. V2V will be used as a lower core voltage for MAD internal parts, by supplying it to specific MAD core voltage pins. Until that moment, the VBB is be used for all MAD pins. The VSIM can be used as programming voltage for the Flash memory, if re–flashing is needed after initial flash programming in production. V5V is used for RF parts only.

VR1 is used for the VCXO supply. VR1_SW is derived from VR1 inside the CCONT, and is actually the same voltage, but it can be separately

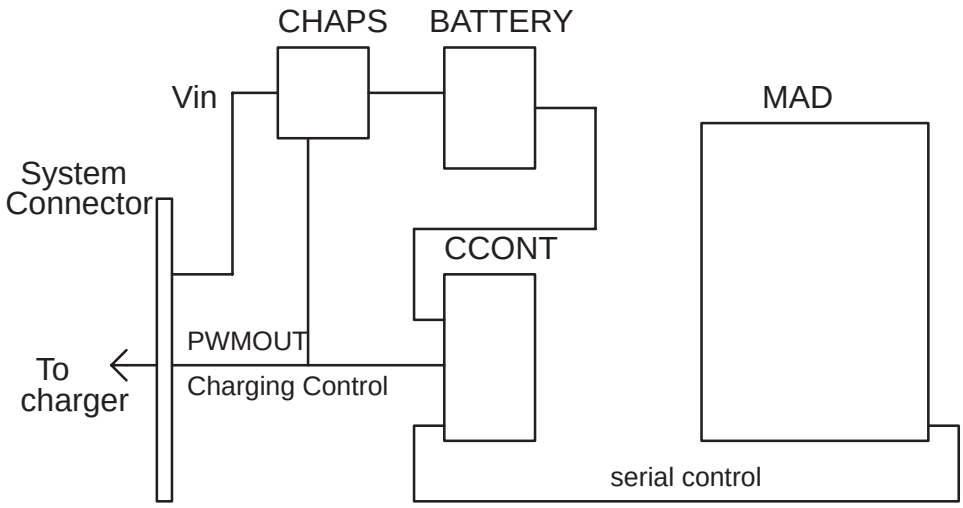
switched on and off. This VR1_SW is used as bias voltage for microphone, during talk modes. Voltage VR6 is used in the COBBA for analog parts and also in RF parts. The RFCEN signal to the CCONT controls both the VR1 and VR6 regulators; they can be switched off in sleep modes, during standby.

The CCONT regulators are controlled either through the SIO from the MAD or timing sensitive regulators are controlled directly to their control pins. These two control methods form a logical OR–function, i.e. the regulator is enabled when either of the controls is active. Most of the regulators can be individually controlled.

The CHAPS connects the charger voltage (VCHAR) to battery. The MCU of the MAD controls the charging through the CCONT. The MAD sets the parameters to the PWM–generator in the CCONT and PWM–output controls the charging voltage in the charger.

When the battery voltage is under 3.0V, the CHAPS controls independently the charging current to battery.

Charging Control



Charging is controlled by the MCU SW, which writes control data to the CCONT via the serial bus. The CCONT output pin PWMOUT (Pulse Width Modulation) can be used to control both the charger and the CHAPS circuit in the phone.

2–wire charging

With 2–wire charging the charger provides constant output current, and the charging is controlled by the PWMOUT signal from the CCONT to the CHAPS. The PWMOUT signal frequency is selected to be 1 Hz, and the charging switch in the CHAPS is pulsed on and off at this frequency. The

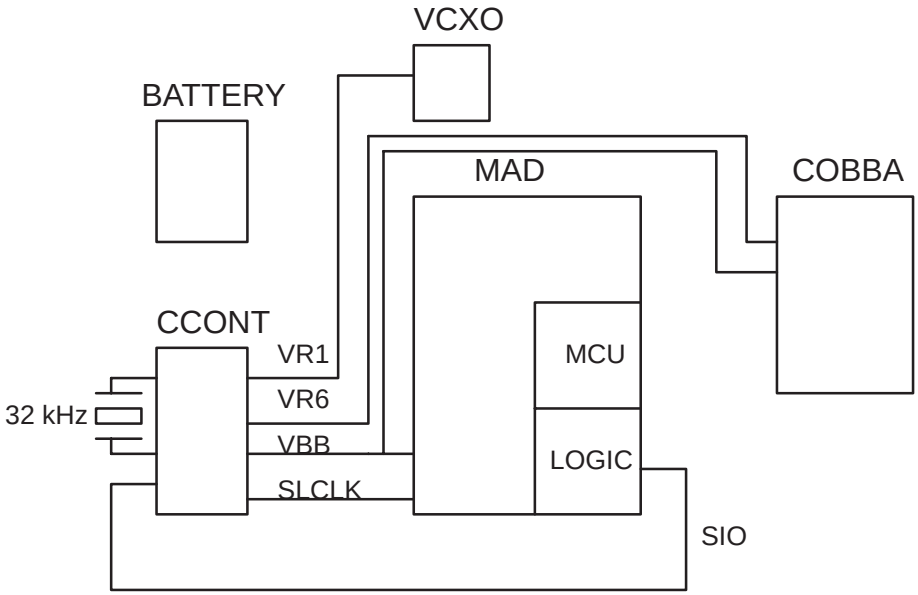
final charged energy to the battery is controlled by adjusting the PWMOUT signal pulse width.

Both the PWMOUT frequency selection and the pulse width control are made by the MCU which writes these values to the CCONT.

3–wire charging

With 3–wire charging the charger provides an adjustable output current, and the charging is controlled by the PWMOUT signal from the CCONT to the Charger, with the bottom connector signal. The PWMOUT signal frequency is selected to be 32 Hz, and the charger output voltage is controlled by adjusting the PWMOUT signal pulse width. The charger switch in the CHAPS is constantly on in this case.

Watchdog



Both MAD and CCONT include a watchdog, and both use the 32 kHz sleep clock. The watchdog in MAD is the primary one, and this is called SW–watchdog. MCU has to update it regularly. If it is not updated, logic inside MAD gives reset to MAD. After the reset, MCU can read an internal status bit to see the reason for reset, whether it was from MAD or CCONT. The SW–watchdog delay can be set between 0 and 63 seconds at 250 millisecond steps; and after power–up the default value is the max. time.

MAD must reset CCONT watchdog regularly. CCONT watchdog time can be set through SIO between 0 and 63 seconds at 1 second steps. After power–up the default value is 32 seconds. If watchdog elapses, CCONT will cut off all supply voltages.

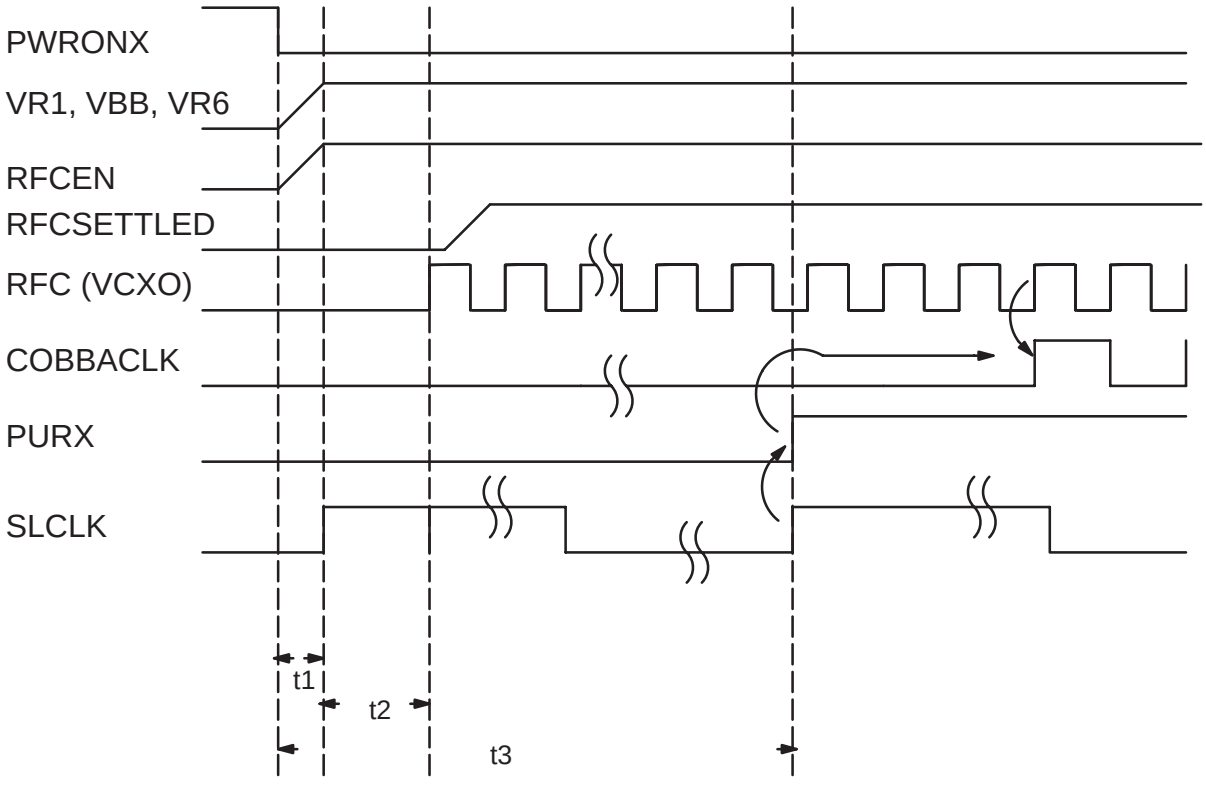
After total shut down the phone can be re–started through any normal power–up procedure.

Power up

When the battery is connected to the phone, nothing will happen until the power–up procedure is initiated, for instance by pressing the power–button (or by connecting charger voltage). After that the 32kHz crystal oscillator of CCONT is started (can take up to 1 sec), as well as the regulators are powered up.

If power down is done, and the battery remains connected, the 32 kHz crystal oscillator keeps still running in the CCONT. When power–up is initiated again, the complete power–up sequence is described in the figure below. This time the power–up sequence is faster, because the oscillator is already running.

Power up when power–button is pushed



t1	< 1 ms
t2	1 – 6 ms, VCXO settled
t3	62 ms, PURX delay generated by CCONT

After the PWR–key has been pushed, the CCONT gives PURX reset to the MAD and COBBA, and turns on the VR1, VBB and VR6 regulators (if battery voltage has exceeded 3.0 V). VR1 supplies the VCXO, VBB supplies the MAD and digital parts of the COBBA, and VR6 supplies analog

parts of the COBBA and some RF parts. After the initial delay t2 the VCXO starts to give proper RFC to the COBBA that further divides it to COBBACLK for the MAD. The COBBA will output the COBBACLK only after the PURX reset has been removed. After delay t3 the CCONT releases PURX and the MAD can take control of the operation of the phone.

After that the MCU–SW in the MAD detects that the PWR–key is still pushed and shows the user that the phone is powering up by starting the LCD and turning on the lights. The MCU–SW must start also the RF receiver parts at this point.

The CCONT will automatically power–up also the VSIM–regulator (used for possible reFlashing), regardless of the control pin SIMPWR state, and the regulator default voltage is 3V.

The V5V–regulator (for RF) default value is OFF in power–up, and can be controlled to ON via serial bus when needed.

IBI (Intelligent Battery Interface)

The phone can be powered up by external device (accessory or similar) by providing a start pulse to the battery signal BTEMP; this is detected by the CCONT. After that the power–up procedure is similar to pushing the power-button.

Mixed trigger to power up

It is possible that the PWR–key is pushed during a charger initiated power–up procedure or that the charger is connected during a PWR–key initiated power up procedure. In this kind of circumstances the power–up procedure (in HW point of view) continues as nothing had happened.

When the Baseband HW is working normally and the SW is running, the SW detects that both conditions are fulfilled and then acts accordingly.

Power Off

Power off by pushing Power–key

The MAD (MCU SW) detects that the PWR–key is pressed long enough time. After that the lights and LCD are turned off. The MCU stops all the activities it was doing (e.g. ends a call), sends power off command to CCONT (i.e. gives a short watchdog time) and goes to idle–task. After the delay the CCONT cuts all the supply voltages from the phone. Only the 32 kHz sleep clock remains running.

Note that the phone doesn’t go to power off (from HW point of view) when the charger is connected and PWR–key is pushed. It is shown to the user that the phone is in power off, but in fact the phone is just acting being powered off (this state is usually called ”acting dead” state).

Power off when battery voltage low

During normal discharge the phone indicates the user that the battery will drain after some time. If not recharged, the SW detects that battery voltage is too low and shuts the phone off through a normal power down procedure.

Anyway, if the SW fails to power down the phone, the CCONT resets and powers down the phone if the battery voltage drops below 2.8V.

Power off when fault in transmitter

If the MAD receives fault indication from the line TXF, that the transmitter is on although it shouldn't be, the control SW will power down the phone.

Sleep Mode

The phone can enter the SLEEP only when both the MCU and DSP request it. A substantial amount of current is saved in the SLEEP. When going to the SLEEP following things happen :

1. Both the MCU and DSP enable sleep mode, set the sleep timer and enter sleep mode
2. RFCEN and RFCSETTLED –> 0 –> COBBACLK will stop (gated in the COBBA). Also VR1 is disabled –> the VCXO supply voltage is cut off –> the RFC stops.
3. LCD display remains the same, no changes
4. Sleep clock (SLCLK) and watchdog in the CCONT running
5. Sleep counter in the MAD running, uses SLCLK

Waking up from Sleep–mode

In a typical case the phone leaves the SLEEP–mode when the SLEEP–counter in MAD expires. After that MAD enables VR1 ⇒ the VCXO starts running ⇒ after a pre–programmed delay RFCSETTLED rises => the MAD receives COBBACLK clock ⇒ the MAD operation re–starts.

There are also many other cases when the SLEEP mode can be interrupted, in these cases the MAD enables the VR1 and operation is started similarly

- some MCU or DSP timer expires
- DSP regular event interrupt happens
- MBUS activity is detected
- FBUS activity is detected
- Charger is connected, Charger interrupt to the MAD
- any key on keyboard is pressed, interrupt to the MAD
- HEADSETINT, from system connector XMIC line (EAD)
- HOOKINT, from system connector XEAR line

Baseband submodules

CTRLU

The CTRLU comprises the MAD ASIC (MCU, DSP, System Logic) and Memories.

The environment consists of three memory circuits (FLASH, SRAM, EEPROM), a 22–bit address bus and a 8/16–bit data bus. Besides there are ROM1SELX, ROM2SELX, RAMSELX and EEPROMSELX signals for chip selection.

MCU main features

System control

Cellular Software (CS)

The Cellular Software takes care of communication with the switching office, as well call set–up, maintenance and termination.

Communication control

M2BUS is used to communicate with external devices. This interface is also used for testing, service and maintenance purposes.

User Interface (UI)

PWR–key, keyboard, LCD, backlight, mic, ear and alert (buzzer, vibra, led) control. Serial interface from the MAD to the LCD (common for CCONT).

Authentication

Authentication is used to prevent fraudulent usage of the cellular phone.

RF monitoring

RF temperature monitoring by VCXOTEMP, ADC in CCONT. Received signal strength monitoring by RSSI, ADC in CCONT. False transmission detection by TXF signal, digital IO–pin.

Power up/down and Watchdog control

When the power key is pressed, the initial reset (PURX) has happened and default regulators have powered up in the CCONT, The MCU and DSP take care of the rest of power up procedures (LCD, COBBA, RF). The MCU must regularly reset the Watchdog counter in CCONT, otherwise the power will be switched off.

Accessory monitoring

Accessory detection by EAD (XMIC/HEADSETINT), AD–converter in the CCONT. Connection (FBUS) for data transfer.

Battery and charging monitoring

The MCU reads the battery type (BTYPE), temperature (BTEMP) and voltage (VBAT) values by AD–converter in CCONT, and the phone's operation is allowed only if the values are reasonable. Charging current is controlled by writing suitable values to the PWM control in the CCONT. The MCU reads also the charger voltage (VCHAR) and the charging current values (ICHAR).

Production/after sales tests and tuning

Flash and EEPROM loading, baseband tests, RF tuning

Control of CCONT via serial bus

The MCU writes controls (regulators on/off, Watchdog reset, charge PWM control) and reads the AD–conversion values. For AD–conversions the MCU gives the clock for the CCONT (bus clock), because the only clock in the CCONT is the sleep clock, which has a too low frequency.

DSP main features

The DSP (Digital Signal Processor) is in charge of the channel and speech coding according to the IS–136 specification. The block consists of a DSP and internal ROM and RAM memory. The input clock is 9.72 MHz, and the DSP has its' own internal PLL–multiplier. Main interfaces are to the MCU, and via System Logic to the COBBA and the RF.

System Logic main features

– MCU related clocking, timing and interrupts (CTIM)
– DSP related clocking, timing and interrupts (CTID)
– DSP general IO–port
–reset and interrupts to MCU and DSP
– interface between MCU and DSP (API)

– MCU interface to System Logic (MCUif)
– MCU controlled PWMs, general IO–port and USART for MBUS (PUP)
– Receive Modem (Rxmodem)
– Interface to Keyboard, CCONT and LCD Drivers (UIF)
– Interface to MCU memories, address lines and chip select decoding (BUSC)

– DSP interface to System Logic (DSPif)
– serial accessory interface (AccIf, DSP–UART)
– Modulation, transmit filter and serial interface to COBBA (MFI)
– Serial interface for RF synthesizer control (SCU)

Memories

The speed of FLASH and SRAM is 120 ns.

FLASH
– Ssize 8 Mbit (512k * 16 bit), optional 4 Mbit and 16 Mbit, all made layout compatible by having additional higher address lines ready in the layout. Flash memory contains the main program code for the MCU, and the EEPROM default values.

SRAM
–Size 128k/256 * 8 bit, in STSOP32 package

EEPROM
– Size 16k * 8 bit
– Serial interface is used.

AUDIO–RF

The audio interface and the baseband–RF interface converters are integrated into the COBBA circuit.

Cobba main features

The codec includes the microphone and earpiece amplifier and all the necessary switches for routing. There are 2 different possibilities for routing; internal and external devices. There are also all the AD- and DA-converters for the RF interface.

The DEMO block is used for FM–demodulation in analog mode.

A slow speed DA–converter provides the automatic frequency control (AFC). In addition, there is a DA–converter for the transmitter power control (TXC).

The COBBA also passes the RFC (19.44 MHz) to MAD as COBBACLK (9.72 MHz).

The COBBA is connected to the MAD via two serial buses:

– RXTXSIO, for interfacing the RF–DACs and DEMO; and also for audio codec and general control. Signals used: COBBACLK (9.72 MHz, from COBBA), COBBACSX, COBBASD (bi–directional data) and COBBADAX (data ready flag for rx–samples).
– Codec SIO, for interfacing the audio ADCs / DACs (PCM–samples). Signals: PCMDCLK (data clock 1.08 MHz / 1.215 MHz), PCMSCLK (frame sync 8.0 kHz / 8.1 kHz), PCMTxdata and PCMRxdata.

Speech processing

The speech coding functions are performed by the DSP in the MAD and the coded speech blocks are transferred to the COBBA for digital to analog conversion, down link direction. In the up link direction the PCM coded speech blocks are read from the COBBA by the DSP.

There are two separate interfaces between the MAD and the COBBA: 2 serial buses. The first serial interface is used to transfer all the COBBA control information (both the RFI part and the audio part). The second serial interface between the MAD and COBBA includes transmit and receive data, clock and frame synchronization signals. It is used to transfer the PCM samples. The frame synchronization frequency is 8 kHz (the sample rate is in digital mode 8.0 kHz and in analog mode 8.1 kHz) which indicates the rate of the PCM samples and the clock frequency is 1 MHz. The COBBA is generating both clocks.

Alert Signal Generation

.A dynamic type buzzer is used for giving alerting tones and/or melodies as a signal of an incoming call. The buzzer is controlled with a BuzzerPWM output signal from the MAD. The low impedance buzzer is connected to an output transistor that gets the drive current from the PWM output. The alert volume can be adjusted either by changing the pulse width causing the level to change or by changing the frequency to utilize the resonance frequency range of the buzzer.

A vibra alerting device is used for giving silent signal to the user of an incoming call. The device is controlled with a VibraPWM output signal from the MAD. The vibra alert can be adjusted either by changing the pulse width or by changing the pulse frequency. The vibra device is not inside the phone, but in a special vibra battery.

PWRU

The PWRU comprises the CCONT circuit and the CHAPS circuit.

CCONT main features

The CCONT generates regulated supply voltages for the baseband and the RF. There are seven 2.8 V linear regulators for the RF, one 2.8 V regulator for baseband, one special switched output (VR1_SW), one programmable 2V output (V2V), one 3/5 V output (VSIM), one 5V output (V5V), and one 1.5 V +/– 1.5% reference voltage for RF and COBBA.

Other functions include:

– power up/down procedures and reset logic
– charging control (PWM), charger detection
– watchdog
– sleep clock (32 kHz) and control
– 8–channel AD–converter.

CHAPS main features

The CHAPS comprises the hardware for charging the battery and protecting the phone from over–voltage in the charger connector.

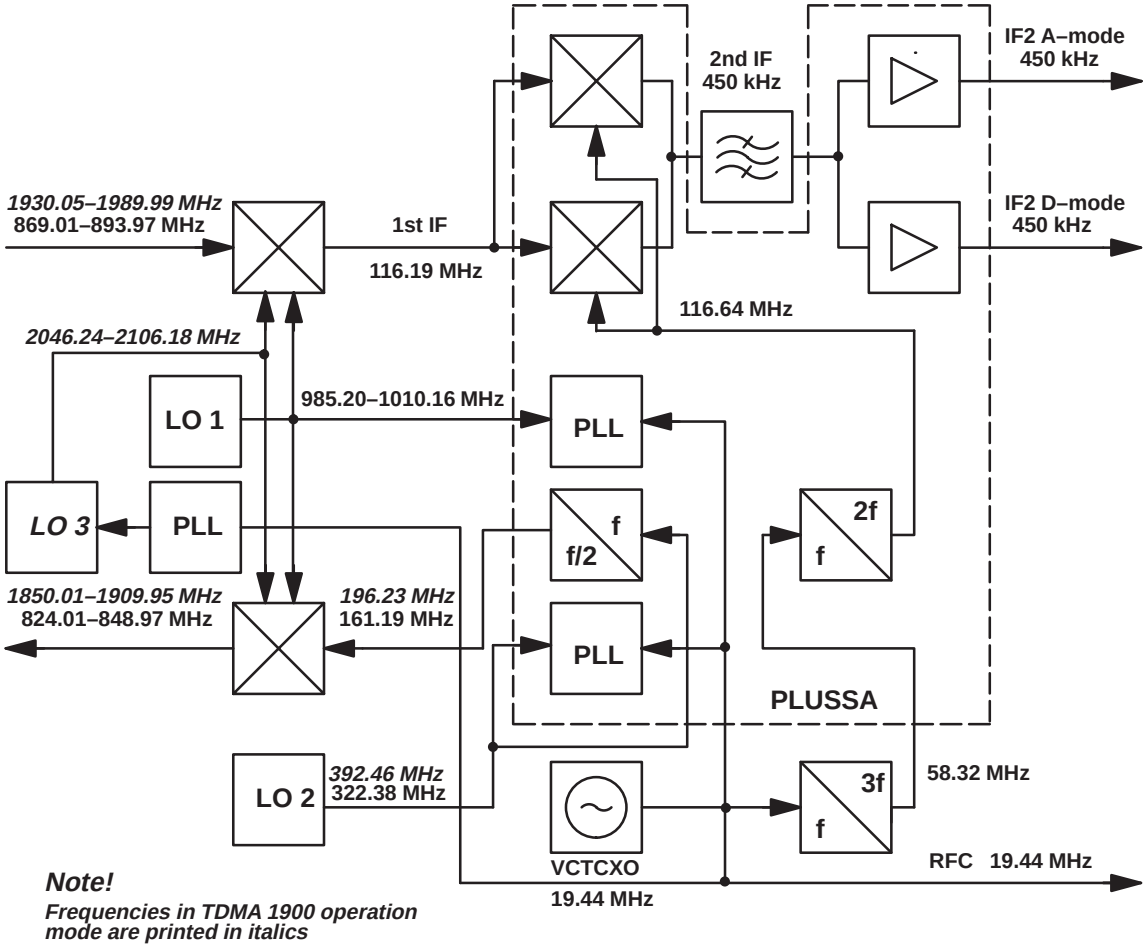
The main functions include:

– transient, over–voltage and reverse charger voltage protection
– limited start–up charge current for a totally empty battery
– voltage limit when the battery removed
– with SW protection protection against too high charging current

RF Module

RF Frequency Plan

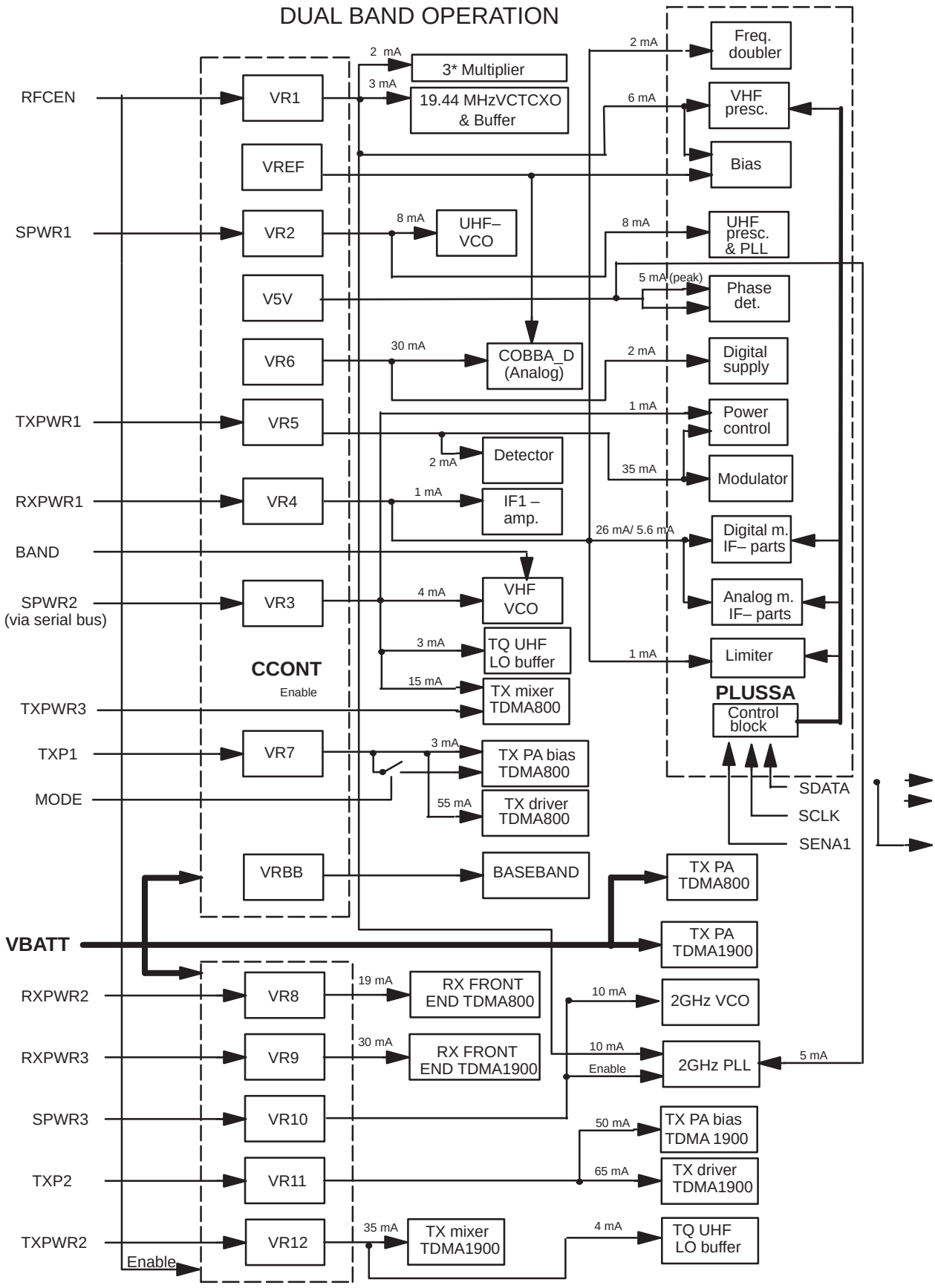
Intermediate frequencies of the RX are the same in all operation modes. The LO and modulator frequencies are different in TDMA800 and TDMA1900 operation modes. See the figure below for details.



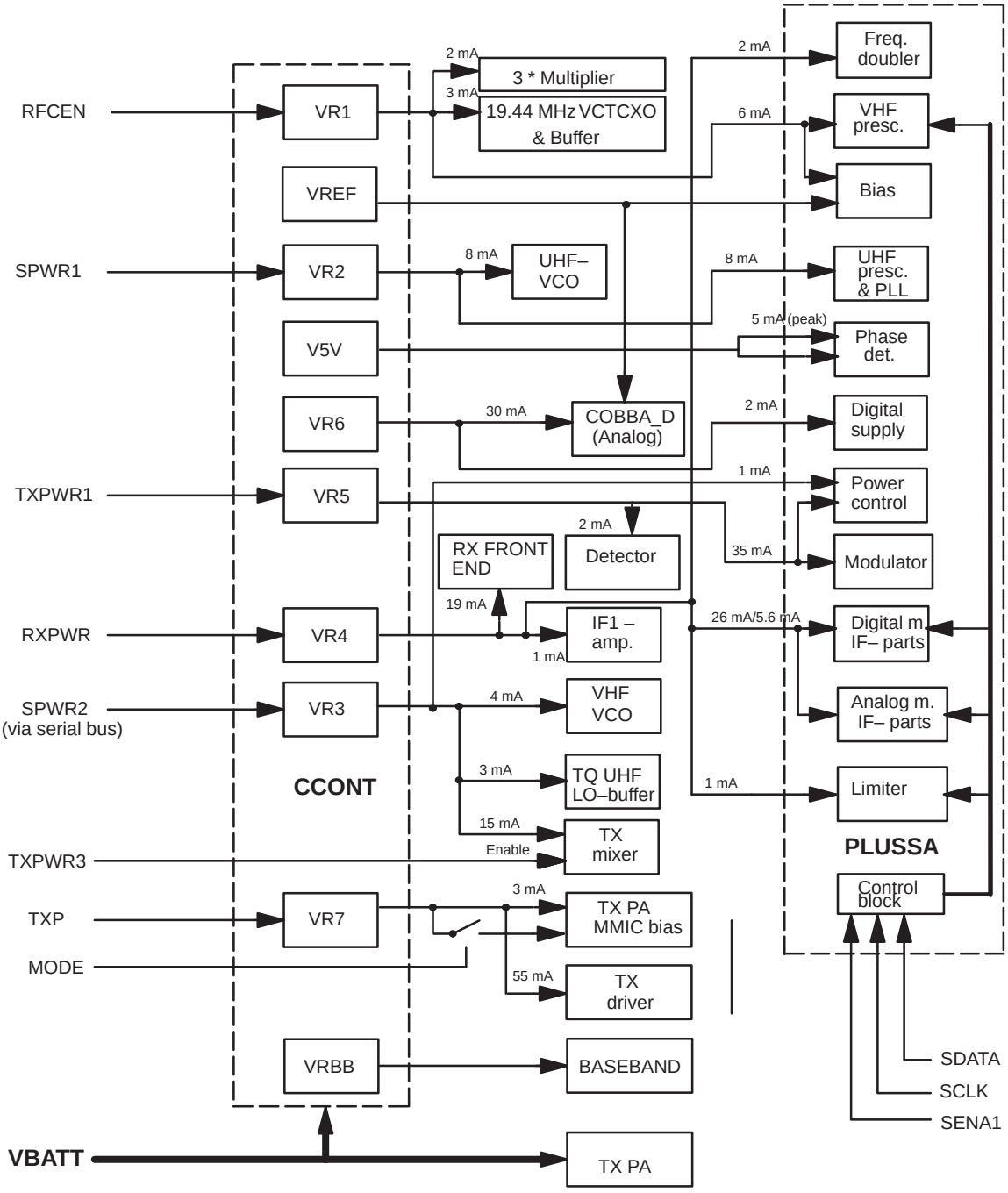
DC Characteristics

Power Distribution Diagram

There are two options for power distribution. The1st option is a dual band phone. 2nd option is a 800 MHz DAMPS phone, which is done by removing redundant components of the 1900 MHz band operation. Current consumptions in the diagrams are only suggestive.


DUAL BAND OPERATION
RFCEN
SPWR1
TXPWR1
RXPWR1
BAND
SPWR2
(via serial bus)
TXPWR3
TXP1
MODE
VBATT
RXPWR2
RXPWR3
SPWR3
TXP2
TXPWR2
Enable
VR1
VREF
VR2
V5V
VR6
VR5
VR4
VR3
VR7
VRBB
VR8
VR9
VR10
VR11
VR12
CCONT
Enable
2 mA
3* Multiplier
3 mA
19.44 MHzVCTCXO
& Buffer
8 mA
UHF–
VCO
30 mA
COBBA_D
(Analog)
2 mA
Detector
1 mA
IF1 –
amp.
4 mA
VHF
VCO
3 mA
TQ UHF
LO buffer
15 mA
TX mixer
TDMA800
3 mA
TX PA bias
TDMA800
55 mA
TX driver
TDMA800
BASEBAND
19 mA
RX FRONT
END TDMA800
30 mA
RX FRONT
END TDMA1900
35 mA
TX mixer
TDMA1900
4 mA
TQ UHF
LO buffer
2 mA
Freq.
doubler
6 mA
VHF
presc.
Bias
8 mA
UHF
presc.
& PLL
5 mA (peak)
Phase
det.
2 mA
Digital
supply
1 mA
Power
control
35 mA
Modulator
26 mA/ 5.6 mA
Digital m.
IF– parts
Analog m.
IF– parts
1 mA
Limiter
PLUSSA
Control
block
SDATA
SCLK
SENA1
TX PA
TDMA800
TX PA
TDMA1900
10 mA
2GHz VCO
10 mA
Enable
2GHz PLL
5 mA
50 mA
TX PA bias
TDMA 1900
65 mA
TX driver
TDMA1900

DAMPS ONLY OPERATION



Power Distribution – Typical Currents (dual band)

	800 MHz Ext. Standby [mA]	800 MHz Analog Control Channel [mA]	800 MHz Analog Traffic Channel [mA]	800 MHz Digital Control Channel [mA]	800 MHz Digital Traffic Channel [mA]	1900 MHz Digital Control Channel [mA]	1900 MHz Digital Traffic Channel [mA]
VR1	3.0 / 0.0	3.0	9.0	3.0 / 0.0	9.0	13.0 / 0.0	19.0
VR2	16.0 / 0.0	16.0	16.0	16.0 / 0.0	16.0	0.0	0.0
VR3	0.0	0.0	23.0	0.0	13.0	0.0	8.0
VR4	11.6 / 0.0	11.6	11.6	32 / 0.0	12.8*	32 / 0.0	12.8*
VR5	0.0	0.0	37.0	0.0	13.0 **	0.0	13.0 **
VR6	2.0 / 0.1	2.0	32.0 ***	2.0 / 0.1	32.0 ***	2.0 / 0.1	32.0 ***
VR7	0.0	0.0	58.0	0.0	19.2 ’	0.0	0.0
VR8	19.0 / 0.0	19.0	19.0	19.0 / 0.0	7.6 ’’	0.0	0.0
VR9	0.0	0.0	0.0	0.0	0.0	30.0 / 0.0	12.0 ’’’
VR10	0.0	0.0	0.0	0.0	0.0	10.0 / 0.0	10.0
VR11	0.0	0.0	0.0	0.0	0.0	0.0	38^
VR12	0.0	0.0	0.0	0.0	0.0	0.0	12.9^^
V5V	5.0 / 0.0	5.0	5.0	5.0 / 0.0	5.0	5.0 / 0.0	5.0
Total	56.6 / 0.1	56.6	210.6	77.0 / 0.1	127.6	92.0 / 0.1	162.7

NOTES: * Mean value (ON/OFF=8/20ms), peak current 32.0 mA
** Mean value (ON/OFF=7/20ms), peak current 37.0 mA
*** Cobba_D mean current consumption estimated to be 30 mA
’ Mean value (ON/OFF=6.6/20ms), peak current 180.0 mA
’’ Mean value (ON/OFF=8/20ms), peak current 10.0 mA
’’’ Mean value (ON/OFF=8/20ms), peak current 15.0 mA when AGC2=1
^ Mean value (ON/OFF=6.6/20ms), peak current 115.0 mA
^^ Mean value (ON/OFF=6.6/20ms), peak current 39.0 mA

Functional Description

Receiver

DAMPS800 RX

The receiver is a double conversion receiver. Most of the RX functions are integrated in two ICs, namely receiver front end and the PLUSSA. The receiver front end contains a LNA and the 1st mixer. Analog and digital IF–parts are integrated in the PLUSSA.

The received RF signal from the antenna is fed via a duplex filter to the receiver unit. The signal is amplified by a low noise preamplifier. In the digital mode the gain of the amplifier is controlled by the AGC2 control line. The nominal gain of 17 – 19 dB is reduced in the strong signal condition about 15 dB (in the digital mode). After the preamplifier the signal is filtered by a SAW RF filter. The filter rejects spurious signals coming from the antenna and spurious emissions coming from the mixer and IF parts. The AGC2 gain step is also used to improve the receiver's performance against spurious responses in real field situations, when the received signal level is high enough for reduced gain and there are radio signals causing on channel intermodulation results.

The filtered RF–signal is down converted by an active mixer. The frequency of the first IF is 116.19 MHz. The first local signal is generated in the UHF synthesizer. The IF signal is fed to a SAW IF–filter. The filter rejects intermodulating signals and the second IF image signal. The filtered 1st IF is amplified and fed to the receiver section of the integrated RF circuit PLUSSA, which has separate IF paths for analog and digital modes of operation.

In the digital mode the IF1 signal is amplified by an AGC amplifier, which has a gain control range of 57 dB. The gain is controlled by an analog signal via AGC1–line. The amplified IF signal is down converted to the second IF in the mixer of the PLUSSA. The second local signal is the 6th overtone of the 19.44 MHz VCTCXO. The LO frequency multiplier is implemented in two stages. The first multiplication by 3 is done within the VCTCXO–module and the second multiplication by 2 is done in the PLUSSA.

The second IF frequency is 450 kHz. The second IF is filtered by a ceramic filter. The filter rejects signals of the adjacent channels. The filtered second IF is fed back to PLUSSA, where it is amplified and fed out to the COBBA_D via balanced IF2D lines.

In the analog mode the filtered and amplified IF1 signal is fed to a mixer. This mixer has been optimized for low current consumption. After this the mixer down converted signal is fed through the same IF2 filter as in digital mode and finally it is amplified in the limiter amplifier. The limited IF2 signal is fed via balanced IF2A lines to COBBA_D, which has a FM–detector.

The limiter amplifier produces also a RSSI voltage for analog mode field strength indication.

TDMA 1900 RX

On the 1900 MHz band the receiver operates only in digital mode. There is a separate front end for this band. The IF–parts are common for both bands. Operation of the receiver is similar to the digital mode operation on 800 MHz band.

Transmitter

DAMPS800 TX

The TX intermediate frequency is modulated in digital mode by an I/Q modulator contained in the transmitter section of the PLUSSA IC. The TXI and TXQ signals are generated in the COBBA_D interface circuit and they are fed differentially to the modulator. In the analog mode the FM modulation is also generated in the I/Q modulator.

The intermediate frequency level at the modulator output is controlled via a serial bus. The modulator output level control is used to tune out tolerances of the TX chain and expand the range of the VGA. The output level of the modulator is typically –18dBm on the highest power level (PL2). For lower power levels modulator output is reduced by 4 dB for each power level. In the analog mode the PLUSSA modulator has a fixed output level. All power levels are defined by adjusting the driver amplifier's gain.

The output signal from the PLUSSA modulator is filtered to reduce harmonics and RX–band noise. The final TX signal is achieved by mixing the UHF VCO signal and the modulated TX intermediate signal in an active mixer. After the mixing the TX signal is amplified by a driver stage. Driver amplifier has a gain control stage, which is used for power level adjustment and generating ramps. From driver stage the signal is fed trough a TX filter to the PA MMIC.

The PA amplifies the signal TX 27–30 dB. The amplified TX signal is filtered in a duplex filter. Then signal is fed to the antenna switch, where the signal is coupled either to the antenna or to the external antenna connector. The typical maximum output level is 600 mW.

The power control loop controls the gain of the driver amplifier. The power detector consists of a directional coupler and a diode rectifier. The output voltage of the detector is compared to TXC voltage in the PLUSSA. The power control signal (TXC), comes from the RF interface circuit, the COBBA_D. The TXP signal sets driver power down to ensure off–burst level requiremensts.

False transmission indication is used to protect the transmitter against false transmission caused by component failure. Protection circuit is in the PLUSSA . The level for TXF is set by internal resistor values in the PLUSSA.

TDMA 1900 RX

See 800 MHz digital mode transmitter.

Frequency Synthesizers

The stable frequency reference for the synthesizers and base band circuits is the voltage controlled, temperature compensated crystal oscillator VCTCXO. The frequency of the oscillator is 19.44 MHz. It is controlled by an AFC voltage, which is generated in the base band circuits. In the digital mode operation, the receiver is locked to a base station frequency by the AFC. Next to the detector diode, there is a sensor for temperature measurement. The voltage RFTEMP from this sensor is fed to the baseband for A/D conversion. This information of the RF PA–block temperature is used as input for compensation algorithms.

The ON/OFF switching of the VCTCXO is controlled by the sleep clock in the baseband via RFCEN. Other parts of the synthesizer section are 1 GHz VCO, 2 GHz VCO, VHF VCO, PLL for 2 GHz VCO and PLL sections of the PLUSSA IC.

DAMPS800 operation

The 1GHz UHF synthesizer generates the down conversion injection for the receiver and the up conversion injection for the transmitter. The UHF frequency is 985.20 ... 1010.16 MHz, depending on the channel which is used. The 1GHz UHF VCO is a module. The PLL circuit is a dual PLL, common for both UHF and VHF synthesizers. These PLLs are comprised in the PLUSSA IC.

The LO signal for the 2nd RX mixer is multiplied from the VCTCXO frequency as described above.

The VHF synthesizer is running only on digital or analog traffic channel. The 322.38 MHz signal (divided by 2 in the PLUSSA) is used as a LO signal in the I/Q modulator of the transmitter chain.

TDMA 1900 operation

The 2 GHz VCO with external PLL circuit generates a 2046.24 ... 2106.18 MHz injection signals for 1st RX mixer and TX upconverter.

The VHF synthesizer is running only on a digital traffic channel. Operating frequency 392.46 MHz is fed to the PLUSSA modulator, where it is divided by 2 and used as the modulator LO signal.

Supply voltages in different modes of operation

	800 MHz Ext. Stadby	800 MHz Analog Control Channel	800 MHz Analog Traffic Channel	800 MHz Digital Control Channel	800 MHz Digital Traffic Channel	1900 MHz Digital Control Channel	1900 MHz Digital Traffic Channel
VR1	ON/OFF	ON	ON	ON/OFF	ON	ON/OFF	ON
VR2	ON/OFF	ON	ON	ON/OFF	ON	ON/OFF*	ON/OFF*
VR3	OFF	OFF	ON	OFF	ON	OFF	OFF
VR4	ON/OFF	ON	ON	ON/OFF	ON/OFF	ON/OFF	ON/OFF
VR5	OFF	OFF	ON	OFF	ON/OFF	OFF	ON/OFF
VR6	ON	ON/OFF	ON	ON/OFF	ON	ON/OFF	ON
VR7	OFF	OFF	ON	OFF	ON/OFF	OFF	OFF
VR8	ON/OFF	ON	ON	ON/OFF	ON/OFF	OFF	OFF
VR9	OFF	OFF	OFF	OFF	OFF	ON/OFF	ON/OFF
VR10	OFF	OFF	OFF	ON/OFF*	ON/OFF*	ON	ON
VR11	OFF	OFF	OFF	OFF	OFF	OFF	ON/OFF
VR12	OFF	OFF	OFF	OFF	OFF	OFF	ON/OFF
VSIM	ON/OFF	ON	ON	ON/OFF	ON	ON/OFF	ON
NOTE: * ON during interband MAHO							

Software Compensations

Power Levels (TXC) vs. Temperature

It is necessary to compensate the effect of temperature on the phone output power. To monitor this environment change, the temperature measurement is done by using a NTC resistor. A factor table is used for temperature compensation. The table contains common values for all power levels and operating modes. The table values are defined without factory measurements. The temperature is measured and right compensation value is added to the TXC–value. The requirement for compensation update is for every 1 minute or after every 5 degrees C of temperature change. This means, that during analog mode transmission there will be a need for temperature reading and TXC compensation update. Because of poor cooling of RF block and insufficient linearity in high temperatures, the output power is reduced from level 2 to level 2.5 when temperature inside the phone is above +55 C in analog mode and above +60 C in digital mode.

Power Levels (TXC) vs. Channel

The duplexer frequency response ripple is compensated by the software. The power levels are calibrated on four channels. The values for chan-

nels between these tuned channels are calculated by using linear interpolation.

Power levels vs. Battery Voltage

For saving battery capacity and because of insufficient linearity in digital mode, output power is decreased from level 2 to level 2.5, when battery voltage drops below 3.3V. (tbd.). The power reduction is done linearly as a function of battery voltage Vcc 3.3V ... 3.1V –> PL2 ... PL2.5.

TX Power Up/Down Ramps

The transmitter output power up/down ramps are controlled by the SW. A special ramp table is used for that. Requirement is for nine different ramps in digital mode for both operating bands and one ramp for analog mode. Separate ramps are used in power up and power down ramps.

Modulator Output Level

For optimum linearity and efficiency the output level of the modulator is adjusted in the production. The AGC amplifier is used as 2 dB step attenuator to define power levels. The 0 dB level is the production tuned reference level.

Digital Mode RSSI

Digital mode RSSI vs. input signal is calibrated in production, but RSSI vs. temperature and RSSI vs. channel are compensated by software.

RF Block Specifications

Receiver

DAMPS 800 Mhz Front End

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Gain, LNA gain enabled (gain variations vs temp. included)	19	21	24	dB
Gain, LNA gain disabled		4		dB
Gain step	14	17		dB
Gain variation vs temp –30...+85 °C, amplifier enabled, ref. to nominal gain			±1.5	dB
Noise figure, LNA enabled		2.5	3.0	dB

TDMA 1900 Mhz Front End

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Gain, LNA gain enabled (gain variations vs temp. included)	19	21	23	dB
Gain, LNA gain disabled		–4		dB
Gain step	14	17		dB
Gain variation vs temp –30...+85 °C, amplifier enabled, ref. to nominal gain			±1.5	dB
Noise figure, LNA enabled		3.0	3.5	dB

First IF Amplifier

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Operation frequency		116.19		MHz
Supply voltage	2.7	2.8	2.9	V
Current consumption		1.0	1.5	mA
Insertion gain	10		14	dB
Noise figure			3	dB
IIP3	–20			dBm
Input impedance		TBD		matched to the IF filter
Output impedance		TBD		matched to PLUSSA

Transmitter

RF Characteristics

Item	DAMPS	TDMA1900
TX frequency range	824.01...848.97 MHz	1850.01...1909.95 MHz
Type	Upconversion	
Intermediate frequency	161.19 MHz	196.23 MHz
Nominal power on highest power level	0.6 W (≈ 27.8 dBm)	0.4 W (≈ 26 dBm)
Power control range	30+38 dB	
Maximum rms error vector	12.5 %	

Power Levels

Power level	Analog mode	Digital mode 800 MHz	Digital mode 1900 MHz	Design target	Unit / Notes
	Class III	Class IV	Class IV	Class IV	dBm
2 Reduced 2 (*	27 +2 ,–4 26 +2 ,–2	28 +2 ,–4 26 +2 ,–2	26 +2 ,–4 25 +2 ,–2	+0.5 ,–1 +0.5, –1	dBm
3	24 +2 ,–4	24 +2 ,–4	24 +2 ,–4	+2 ,–2	dBm
4	20 +2 ,–4	20 +2 ,–4	20 +2 ,–4	+2 ,–2	dBm
5	16 +2 ,–4	16 +2 ,–4	16 +2 ,–4	+2 ,–2	dBm
6	12 +2 ,–4	12 +2 ,–4	12 +2 ,–4	+2 ,–2	dBm
7	8 +2 ,–4	8 +2 ,–4	8 +2 ,–4	+2 ,–2	dBm
8	–	4 +2 ,–6	4 +2 ,–6	+2 ,–2	dBm
9	–	0 +2 ,–6	0 +2 ,–6	+2 ,–2	dBm
10	–	–4 +2 ,–6	–4 +2 ,–6	+2 ,–2	dBm

(* Used when battery voltage goes lower than 3.3V and in high temperature.

Synthesizers

UHF

Parameter	UHF 800MHz analog mode rx/tx injection	UHF 800MHz digital mode rx/tx slot	UHF 1900MHz rx/tx slot	Unit / Notes
Frequency range	985.20 ... 1010.16	985.20 ... 1010.16	2046.24 ... 2106.18	MHz
Reference frequency	30	30	30	kHz
Reference peaks @ 30 kHz @ 60 kHz	–31 –70	–38 –57	–38 –57	dBc, max

Parameter	UHF 800MHz analog mode rx/tx injection	UHF 800MHz digital mode rx/tx slot	UHF 1900MHz rx/tx slot	Unit / Notes
2 x fo level	–20	–20	–20	dBc
Phase noise, fo ± 60 kHz fo ±120 kHz	–115	–101 –121	–101 –121	dBc/Hz, max
Phase error	–	4	4	$^{\circ}_{rms}$, max
Residual FM Filters: 300 Hz HP 3 kHz LP	150	–	–	Hz, max
Frequency settling time within ± 3 kHz within ± 30 Hz	 20	 1.4 2.0	 1.4 2.0	ms, max
Start up settling time	30	3	3	ms, max

VHF

Parameter	VHF, 800MHz analog mode tx injection	VHF, 800MHz digital mode rx/tx slot	VHF, 1900MHz –mode tx injection	Unit / Notes
Frequency range	322.38	322.38	392.46	MHz
Reference frequency	30	30	30	kHz
Reference peaks @ 30 kHz @ 60 kHz	–31 –66	–41 –60	–41 –60	dBc, max
2 x fo level	–30	–30	–30	dBc
Phase noise, fo ± 60 kHz fo ±120 kHz	–105	–105	–105	dBc/Hz, max
Phase error	2	2	2	$^{\circ}_{rms}$, max
Frequency settling time within ± 3 kHz within ± 30 Hz	 20	 20	 20	ms, max
Start up settling time	20	20	20	ms, max

Output Levels

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
2G UHF synthesizer to Lo buffer				
level			–10	dBm
resistive load		tbd		Ω
parallel capacitance		tbd		pF
1G UHF synthesizer to TX mixer				
level			–5	dBm
impedance		tbd		Ω
VHF synthesizer to PLUSSA				
level	100			mV_{pp}
resistive load	1k			Ω
parallel capacitance		tbd		pF
VCTCXO 19.44 MHz to BB				
level	1000			mV_{pp}
resistive load	10k			Ω
parallel capacitance			10	pF
VCTCXO 19.44 MHz to PLUSSA				
level	100			mV_{pp}
resistive load		tbd		Ω
parallel capacitance		tbd		pF
VCTCXO 58.32 MHz to PLUSSA				
3 * fo level	50		100	mV_{pp}
fo and 2xfo level	–25			dBc
harmonic supression	–25			dBc
resistive load		5k		Ω
parallel capacitance		tbd		pF

Connections

RF–Baseband signals

Signal name	From/ *Control*	To	Parameter	Min	Typ	Max	Unit	Function
VBAT	battery	RF 2V8 regul., PA	Voltage	3.1	3.6	5.3	V	Supply voltage for discrete 2V8 regulators in dual band phone and PA
			Voltage during TX	3.0	3.6	5.0	V	
			Current			1200	mA	
VREF	CCONT	PLUSSA	Voltage	1.478	1.50	1.523	V	PLUSSA reference voltage
			Current			10	uA	
VR1	CCONT / *RFCEN*	PLUSSA, VCTCXO, 2GHz PLL	Voltage	2.7	2.8	2.85	V	Supply for VCTCXO & multiplier, PLUSSA VHF prescaler and bias and 2 GHz PLL
			Current, tdma 800	3.0	7	9	mA	
			Current, tdma1900	3.0	17	19	mA	
VR2	CCONT / *SPWR1*	PLUSSA, UHF VCO1	Voltage	2.7	2.8	2.85	V	Supply voltage for tdma 800 UHF VCO and prescaler
			Current, tdma800	14	16	20	mA	
			Current, tdma1900		off		mA	
VR3	CCONT / *SPWR2 (via serial bus)*	VHF–VCO, LO–buff, TX mixer	Voltage	2.7	2.8	2.85	V	Supply for VHF VCO, LO buffer, tdma800 TX mixer and TXF
			Current, tdma800	20	24	30	mA	
			Current, tdma1900	4	9	12	mA	
VR4	CCONT / *RXPWR1*	PLUSSA, VCTCXO IF1–amp	Voltage	2.7	2.8	2.85	V	Supply for PLUSSA IF–parts, IF1–amp.
			Current, anal.RX	10	12	15	mA	
			Current, digi.RX	30	32	34	mA	
VR5	CCONT / *TXPWR1*	PLUSSA, TX pwr control	Voltage	2.7	2.8	2.85	V	Supply for PLUSSA modulator, TX pwr control
			Current, TX–mode	33	37	41	mA	
VR6	CCONT	PLUSSA disc.PLL Cobba_D	Voltage	2.7	2.8	2.85	V	PLUSSA & disc PLL: digital supply, Cobba_D: analog supply
			Current (RF block)		2.0	3.0	mA	
VR7	CCONT *TXP1*	TX PA	Voltage	2.7	2.8	2.85	V	TX PA and driver supply
			Current, tdma800		55	60	mA	
VR7_bias	CCONT TXP1 & MODE	TX PA	Voltage	2.7	2.8	2.85	V	TX PA bias 800 band
			Current, tdma800		3		mA	
V5V	CCONT / *RFCEN*	PLUSSA	Voltage	4.8	5.0	5.2	V	PLUSSA and discrete synthesizer phase det
			Current		3.0	5.0	mA	
RFTEMP	RF	CCONT	Voltage	0		1.5	V	RF temperature sensor (47 k NTC to GND)

Signal name	From/ *Control*	To	Parameter	Min	Typ	Max	Unit	Function
AFC	Cobba_D	VCTCXO	Voltage Min	0.05	1.2	2.25	V	Automatic frequency control signal for VCTCXO. When DAC is switched OFF AFC output is in high–Z mode
			Resolution		11		bits	
			Load resistance (dynamic)		10		kΩ	
			Load resistance (DC)		110		kΩ	
AGC1	Cobba_D	PLUSSA	Voltage Min	0.5		1.40	V	Digital mode receiver gain control.
			Load resistance	10			kΩ	
			Load capacitance			10	pF	
			Resolution		10		bits	
			Timing inaccuracy			8	us	DSP
AGC2	MAD (CTID AGC2, genpio)	RX LNA	Logic high ”1”	2.0			V	LNA gain switch. Polarity: 0=reduced 1=normal
			Logic low ”0”			0.7	V	
			Sink/source curr.			20	uA	
			Load capacitance			10	pF	
			Timing inaccuracy			8	us	DSP
BAND **1)**	Cobba_D	VHF VCO	Logic high ”1”	2.1			V	TDMA1900 operation
			Logic low ”0”	0		0.4	V	TDMA800 operation
			Sink/source curr.			1.0	mA	
			Load capacitance			10	pF	
			Timing inaccuracy			1	ms	DSP, MCU
MODE	MAD	Analog/ digital mode PA bias con-trol	Logic high ”1”	2.1			V	Digital 800 operation
			Logic low ”0”	0		0.4	V	Analog 800 operation
			Sink/source curr.			2.0	mA	
			Load capacitance			tbd	pF	
			Timing inaccuracy				ms	DSP
IF2AP/ IF2AN	PLUSSA	Cobba_D	IF2 frequency		450		kHz	Differential IF2–signal from limiter to DEMO detector in Cobba_D
			Output level,		0.6		V_{pp}	
			Load resistance	10			kΩ	
			Load capacitance			5	pF	
IF2DP/ IF2DN	PLUSSA	Cobba_D	IF2 frequency		450		kHz	Differential IF2–signal to RX A/D–converter, PGA = 0 dB
			Output level		170	1400	mVpp	
			Source imp.			600	Ω	

Signal name	From/ *Control*	To	Parameter	Min	Typ	Max	Unit	Function
RFC	VCTCXO	Cobba_D	Frequency		19.44		MHz	High stability clock signal for the locig circuits
			Signal amplitude	0.2		1.0	Vpp	
			Load resistance	10			kΩ	
			Load capacitance			5	pF	
RFCEN	MAD (CTID, *RFCEN*)	CCONT, Cobba_D	Logic high ”1”	2.0			V	Supply voltage VR1 ON, RFC enable
			Logic low ”0”			0.5	V	Supply voltage VR1 OFF, RFC disable
			Current			100	uA	
			timing inaccuracy			50	us	MCU, DSP
RSSI	PLUSSA	CCONT	Voltage	0.1		1.5	V	Analog mode field strength indicator voltage
			Load resistance	1			MΩ	
			Load capacitance			50	pF	
			Voltage			0.1	V	Digital mode
RXPWR1	MAD (CTID, LNASEL)	CCONT	Logic high ”1”	2.0			V	Supply voltage VR4 ON
			Logic low ”0”			0.5	V	Supply voltage VR4 OFF
			Current			100	uA	
			timing inaccuracy			30	us	DSP
RXPWR2 **1)**	MAD (CTID, *DSP* FTC) MUX	RF block 2V8 regulator	Logic high ”1”	2.0			V	Supply voltage VR8 ON
			Logic low ”0”			0.5	V	Supply voltage VR8 OFF
			Current			100	uA	
			timing inaccuracy			30	us	DSP
RXPWR3 **1)**	MAD (CTID, *DSP* FTC) MUX	RF block 2V8 regulator	Logic high ”1”	2.0			V	Supply voltage VR9 ON
			Logic low ”0”			0.5	V	Supply voltage VR9 OFF
			Current			100	uA	
			timing inaccuracy			30	us	DSP
SCLK	MAD (SCU, *SCLK*)	PLUSSA, UHF PLL tdma1900	Logic high ”1”	2			V	Synthesizer and control clock
			Logic low ”0”			0.8	V	
			Load resistance	50			kΩ	
			Load capacitance			20	pF	
			Data rate freq.		1.62		MHz	

Signal name	From/ *Control*	To	Parameter	Min	Typ	Max	Unit	Function
SDATA	MAD (SCU, *SDATA*)	PLUSSA, UHF PLL tdma1900	Logic high ”1”	2.0			V	Synthesizer and control data
			Logic low ”0”			0.8	V	
			Load resistance	50			kΩ	
			Load capacitance			20	pF	
			Timing accuracy			20	us	
SENA1	MAD (SCU, *SENA1*)	PLUSSA	Logic high ”1”	2.0			V	Synthesizer and PLUSSA control enable
			Logic low ”0”			0.8	V	
			Load resistance	50			kΩ	
			Load capacitance			20	pF	
SENA2 **1)**	MAD (SCU, *SENA2*)	UHF PLL tdma1900	Logic high ”1”	2.0			V	TDMA1900 UHF synthesizer enable
			Logic low ”0”			0.8	V	
			Load resistance	50			kΩ	
			Load capacitance			20	pF	
SPWR1	Cobba_D	CCONT	Logic high ”1”	2.0			V	Supply voltage VR2 ON
			Logic low ”0”			0.5	V	Supply voltage VR2 OFF
			Current			100	uA	
			timing inaccuracy			200	us	DSP
SPWR2	Cobba_D	CCONT	Control sent via CCONT serial bus ”1”					Supply voltage VR3 ON
			Control sent via CCONT serial bus ”0”					Supply voltage VR3 OFF
			Current			100	uA	
			timing inaccuracy			200	us	DSP
SPWR3 **1)**	Cobba_D	RF 2v8 regul.	Logic high ”1”	2.0			V	Supply voltage VR10 ON
			Logic low ”0”			0.5	V	Supply voltage VR10 OFF
			Current			100	uA	DSP
			timing inaccuracy			200	us	
TXA	MAD (MFI, *TXA*)	PLUSSA	Logic high ”1”	2.5			V	Power control loop mode during tx burst
			Logic low ”0”			0.2	V	Power control loop mode during ramp up/down
			Load resistance	10			kΩ	
			Load capacitance			20	pF	
			Timing inaccuracy			10	us	DSP

Signal name	From/ *Control*	To	Parameter	Min	Typ	Max	Unit	Function
TXC	Cobba_D	PLUSSA	Voltage Min value Max value	0.12 2.27	0.15 2.30	0.18 2.33	V	Makes transmitter power ramps and sets transmitter power level
			Load resistance	10			kΩ	
			Load capacitance			10	pF	
			Number of bits		10			
TXF	PLUSSA	MAD	Logic high ”1”	2.5		3.0	V	False transmission indicator, function controlled via PLUSSA register
			Logic low ”0”	0		0.5	V	
			Load capacitance			10	pF	
TXIP/ TXIN	Cobba_D	PLUSSA	Differential voltage swing			1.18	V_{pp}	Differential in–phase TX baseband signal for the RF modulator.
			Common mode v. (digital mode)		0.8		V	
			Load resistance (differential)	200			kΩ	
TXQP/ TXQN	Cobba_D	PLUSSA	Differential voltage swing			1.18	V_{pp}	Differential quadrature phase TX baseband signal for the RF modulator.
			Common mode v. (digital mode)		0.8		V	
			Load resistance (differential)	200			kΩ	
TXLX1	MAD (CTID, *TXLX*)	RF tdma800	Logic high ”1”	2.1			V	Low power level mode for power detector
			Logic low ”0”	0		0.6	V	High power level mode for power detector
			Sink/source curr.			8.0	mA	Timing tied to TXPWR1
			Load capacitance			10	pF	
			Timing inaccuracy			8	us	DSP
TXLX2 **1)**	MAD *(TXLX2, DSPGen-Pio(6))* **2)**	RF tdma1900	Logic high ”1”	2.1			V	Low power level mode for power detector
			Logic low ”0”	0		0.6	V	High power level mode for power detector
			Sink/source curr.			8.0	mA	Timing tied to TXPWR1
			Load capacitance			10	pF	
			Timing inaccuracy			8	us	DSP
TXP1	MAD (MFI, *TXP*) **3)**	CCONT, TX driver, TX PA, in tdma800 mode	Logic high ”1”	2.0			V	Supply voltage VR7 ON
			Logic low ”0”			0.5	V	Supply voltage VR7 OFF
			Current			100	uA	
			Load capacitance			10	pF	
			Timing inaccuracy			10	us	DSP

Signal name	From/ *Control*	To	Parameter	Min	Typ	Max	Unit	Function
TXP2 **1)**	MAD (MFI, *TXP*) **3)**	Penta reg, TX driver, TX PA, in tdma1900 mode	Logic high ”1”	2.0			V	Supply voltage VR11 ON
			Logic low ”0”			0.5	V	Supply voltage VR11 OFF
			Current			100	uA	DSP
			Load capacitance			10	pF	
			Timing inaccuracy			10	us	
TXPWR1	MAD (CTID, *TXPWR1*)	CCONT	Logic high ”1”	2.0			V	Supply voltage VR5 ON, TX power control enable. 800 tx–mixer enable
			Logic low ”0”			0.5	V	Supply voltage VR5 OFF, TX power control disable 800 tx–mixer disable
			Current			50	uA	DSP
			Timing inaccuracy			8	us	
TXPWR2 **1)**	MAD (CTID, *BENA*)	RF 2v8 regul.	Logic high ”1”	2.0			V	Supply voltage VR12 ON
			Logic low ”0”			0.5	V	Supply voltage VR12 OFF
			Current			50	uA	DSP
			Timing inaccuracy			1	us	
TXPWR3	MAD (CTID, *BENA*)	RF 800 MHz upcon.	Logic high ”1”	2.0			V	Upconv enabled
			Logic low ”0”			0.5	V	Upconv disabled
			Current			50	uA	DSP
			Timing inaccuracy			1	us	

1) Signal in use only in dual band engine
2) Valid from MAD80
3) Multiplexed with band signal at BB

Data Interface and Timing

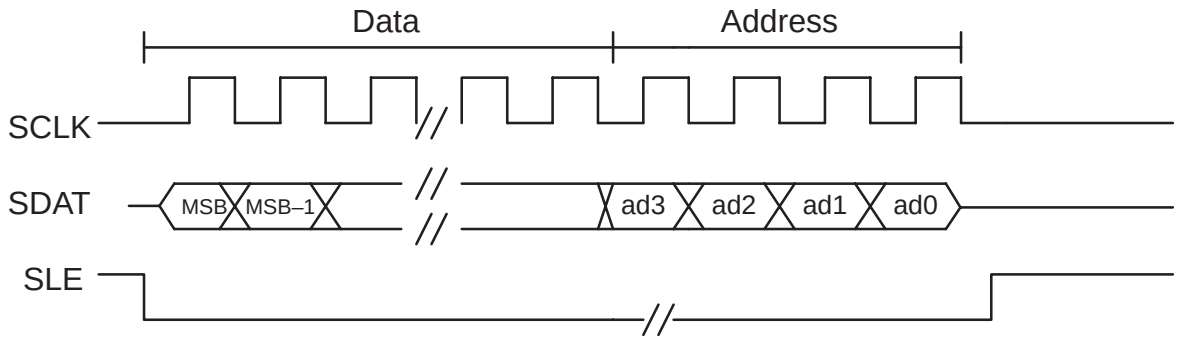
The PLUSSA is programmed via a 3 wire serial bus. Control wires in the RF/BB interface are named SENA1, SDATA and SCLK.

SDAT: Serial data input
The PLUSSA programming data is applied to that pin. The data is qualified by SCLK clock.

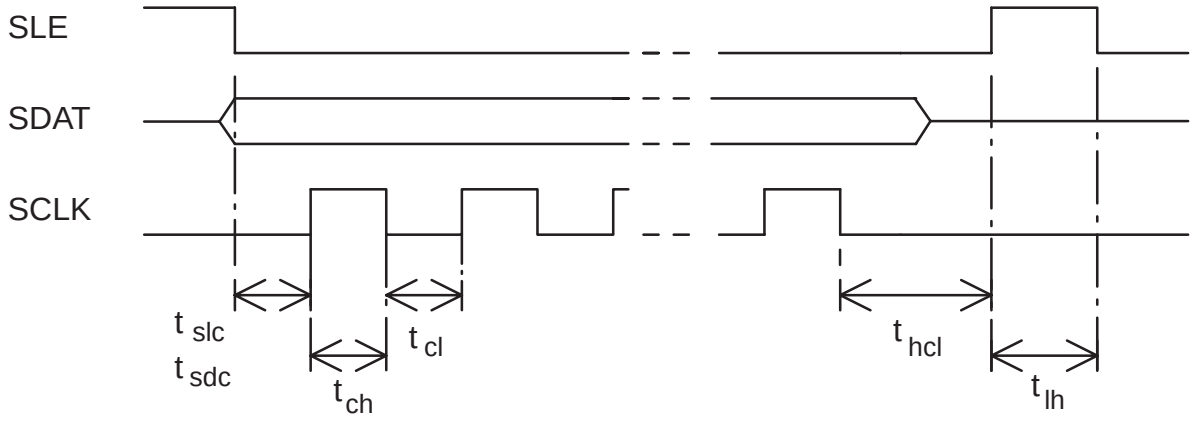
SCLK: Serial clock input
Qualifies the data applied to SDAT pin. Rising edge of the SCLK signal shifts the data to the PLUSSA's internal shift register. The falling edge after the third rising edge qualifies the internal addressing

SLE: Serial latch enable (active low)
By forcing SLE line down the serial interface of the PLUSSA is activated. During the active state the PLUSSA interface accepts the clocking and the data applied to the SCLK and SDAT pins. While SLE is high the interface is completely inactive, so multiple devices can share the same SCLK and SDAT lines.

TDMA 1900 UHF Synthesizer Timing Control



Programming timing

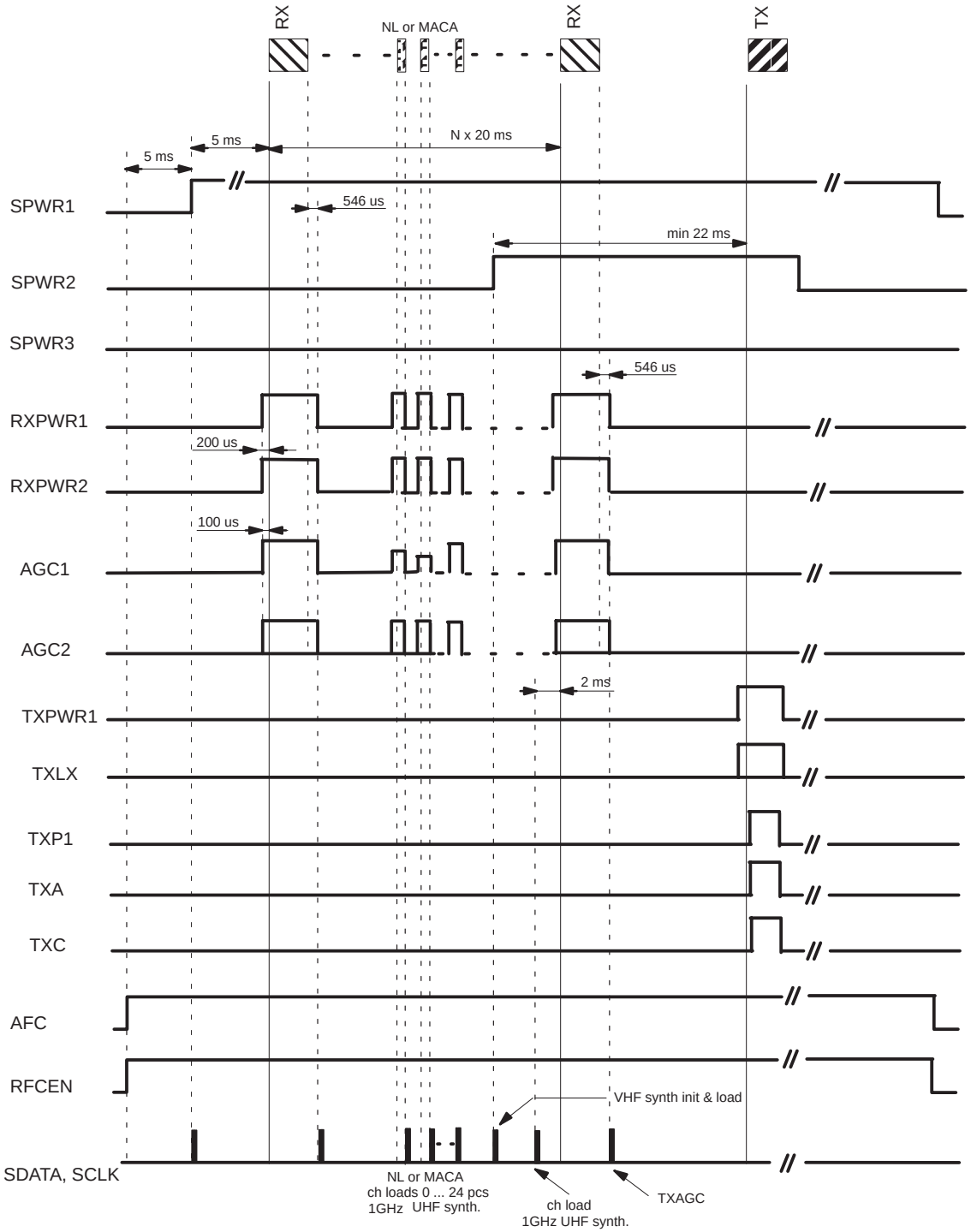


Serial data input timing

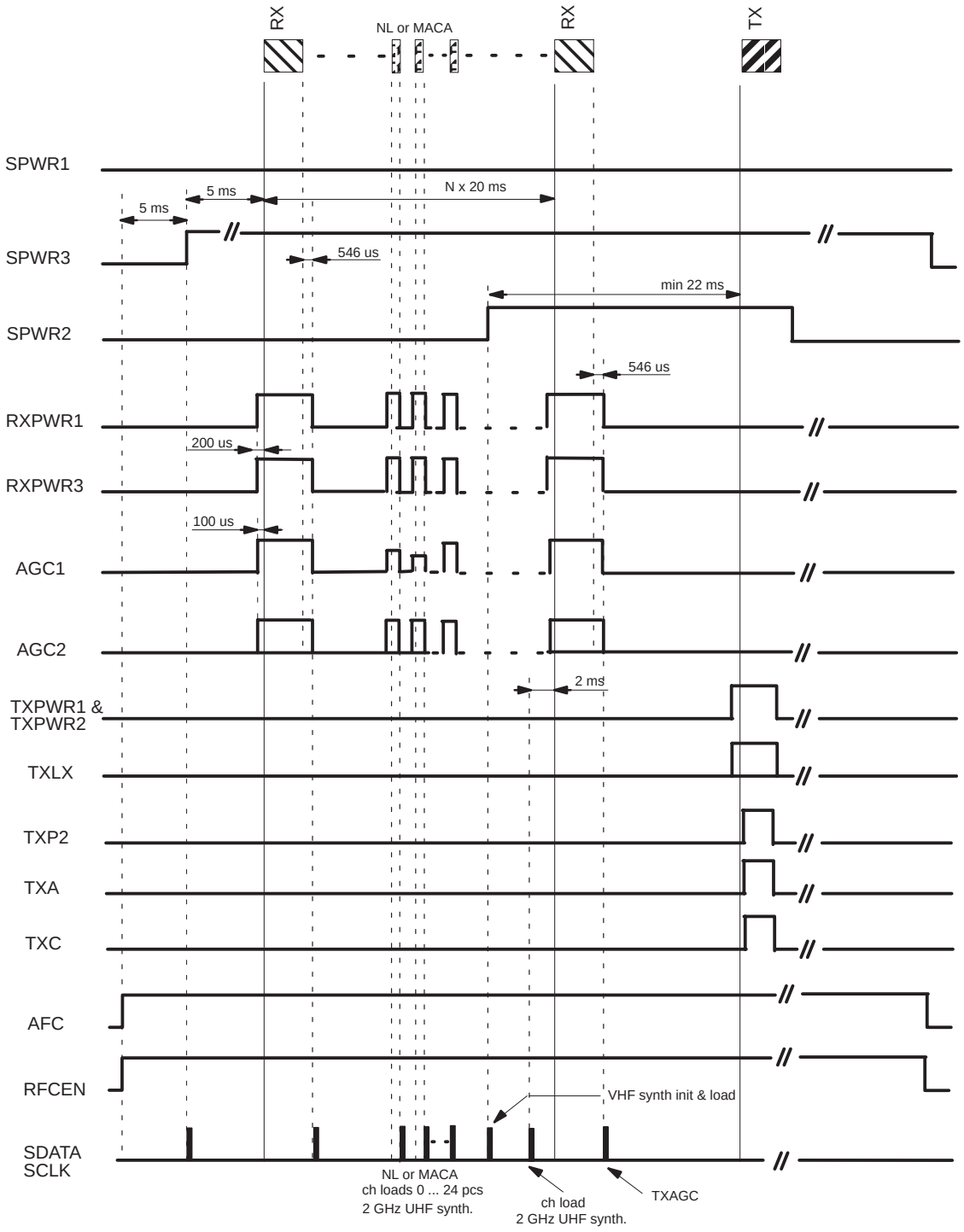
Timing ratings.

abbr	Definition	Min [ns]	Max [ns]
tslc	SLE to SCLK setup time	40	
tsdc	SDAT to SCLK setup time	20	
tch	SCLK high period	50	
tcl	SCLK low period	50	
thcl	SCLK to SLE hold time	20	
tlh	SLE high period	4000	

Digital control channels

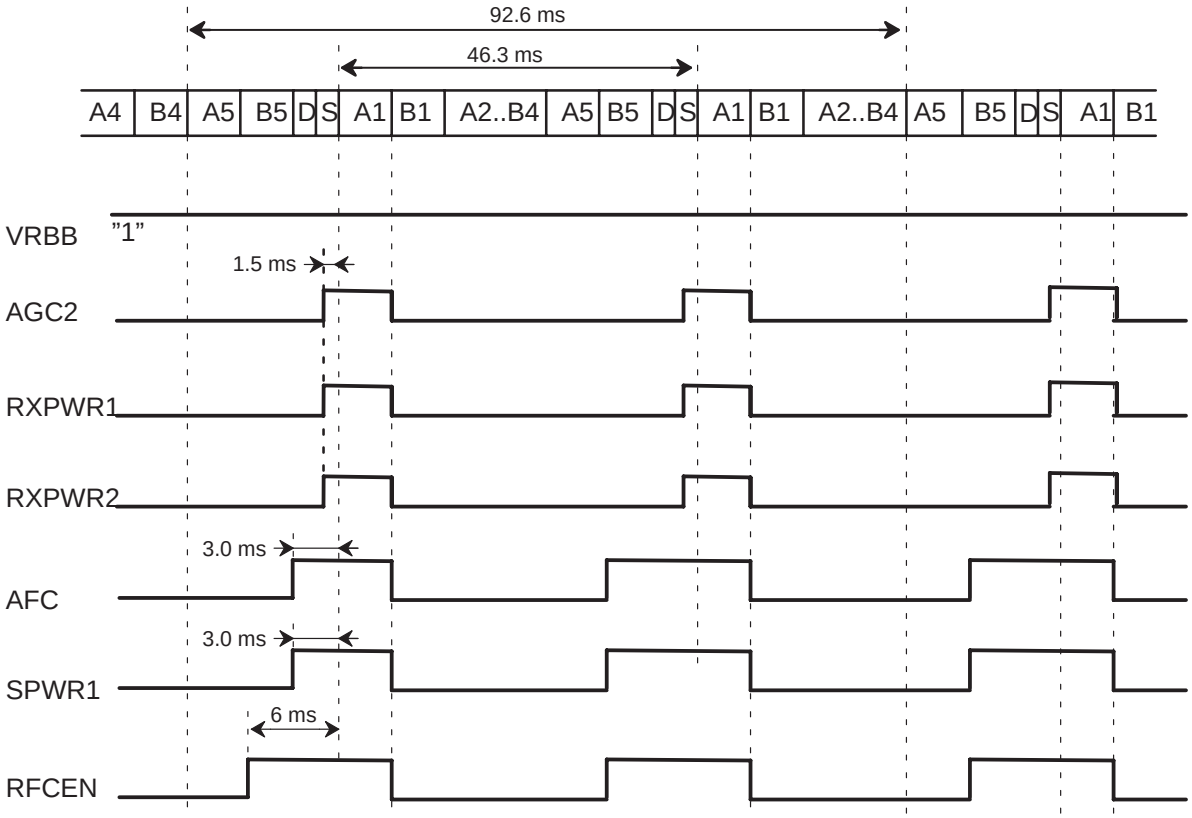


TDMA800 digital control channel timing diagram



TDMA1900 digital control channel timing diagram

Analog control channel



Extended stand by mode timings

Parts list of UT4S system module (EDMS Issue 5.1)

Code: 0201301

ITEM	CODE	DESCRIPTION	VALUE	TYPE
R150	1620019	Res network 0w06 2x10k j	0404	0404
R152	1620025	Res network 0w06 2x100k j	0404	0404
R153	1422881	Chip resistor	0.22	5 % 1 W 1218
R154	1430826	Chip resistor	680 k	5 % 0.063 W 0402
R156	1430853	Chip resistor	2.2 M	5 % 0.063 W 0402
R159	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R161	1620025	Res network 0w06 2x100k j	0404	0404
R163	1620019	Res network 0w06 2x10k j	0404	0404
R164	1620019	Res network 0w06 2x10k j	0404	0404
R165	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R166	1825005	Chip varistor vwm14v vc30v	0805	0805
R168	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R169	1430690	Chip jumper		0402
R200	1620025	Res network 0w06 2x100k j	0404	0404
R201	1620025	Res network 0w06 2x100k j	0404	0404
R202	1620031	Res network 0w06 2x1k0 j	0404	0404
R203	1620031	Res network 0w06 2x1k0 j	0404	0404
R204	1620031	Res network 0w06 2x1k0 j	0404	0404
R205	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R206	1620101	Res network 0w06 2x470r j	0404	0404
R207	1620027	Res network 0w06 2x47r j	0404	0404
R208	1430744	Chip resistor	470	5 % 0.063 W 0402
R209	1430812	Chip resistor	220 k	5 % 0.063 W 0402
R210	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R211	1620025	Res network 0w06 2x100k j	0404	0404
R212	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R213	1620027	Res network 0w06 2x47r j	0404	0404
R214	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R215	1620031	Res network 0w06 2x1k0 j	0404	0404
R216	1620031	Res network 0w06 2x1k0 j	0404	0404
R218	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R256	1620025	Res network 0w06 2x100k j	0404	0404
R257	1430690	Chip jumper		0402
R258	1430718	Chip resistor	47	5 % 0.063 W 0402
R259	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R260	1620023	Res network 0w06 2x47k j	0404	0404
R261	1430740	Chip resistor	330	5 % 0.063 W 0402
R264	1620027	Res network 0w06 2x47r j	0404	0404
R265	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R266	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R267	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R268	1430812	Chip resistor	220 k	5 % 0.063 W 0402

R270	1430812	Chip resistor	220 k	5 % 0.063 W 0402
R272	1430744	Chip resistor	470	5 % 0.063 W 0402
R273	1430710	Chip resistor	22	5 % 0.063 W 0402
R275	1620031	Res network 0w06 2x1k0 j	0404	0404
R701	1430700	Chip resistor	10	5 % 0.063 W 0402
R725	1430710	Chip resistor	22	5 % 0.063 W 0402
R731	1430820	Chip resistor	470 k	5 % 0.063 W 0402
R741	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R742	1430784	Chip resistor	15 k	5 % 0.063 W 0402
R743	1430730	Chip resistor	150	5 % 0.063 W 0402
R744	1430730	Chip resistor	150	5 % 0.063 W 0402
R745	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R746	1430740	Chip resistor	330	5 % 0.063 W 0402
R747	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R751	1430812	Chip resistor	220 k	5 % 0.063 W 0402
R752	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R756	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R758	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R759	1620023	Res network 0w06 2x47k j	0404	0404
R760	1620023	Res network 0w06 2x47k j	0404	0404
R761	1430812	Chip resistor	220 k	5 % 0.063 W 0402
R762	1430851	Chip resistor	15 k	2 % 0.063 W 0402
R763	1430758	Chip resistor	1.5 k	5 % 0.063 W 0402
R764	1430744	Chip resistor	470	5 % 0.063 W 0402
R765	1430744	Chip resistor	470	5 % 0.063 W 0402
R768	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R770	1430700	Chip resistor	10	5 % 0.063 W 0402
R771	1430700	Chip resistor	10	5 % 0.063 W 0402
R772	1430700	Chip resistor	10	5 % 0.063 W 0402
R774	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R775	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R776	1430726	Chip resistor	100	5 % 0.063 W 0402
R786	1430726	Chip resistor	100	5 % 0.063 W 0402
R787	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R788	1430744	Chip resistor	470	5 % 0.063 W 0402
R789	1430744	Chip resistor	470	5 % 0.063 W 0402
R801	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R802	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R803	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R804	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R805	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R806	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R807	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R808	1430772	Chip resistor	5.6 k	5 % 0.063 W 0402
R809	1430740	Chip resistor	330	5 % 0.063 W 0402
R810	1430726	Chip resistor	100	5 % 0.063 W 0402
R811	1430788	Chip resistor	22 k	5 % 0.063 W 0402

R812	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R813	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R814	1430700	Chip resistor	10	5 % 0.063 W 0402
R821	1430710	Chip resistor	22	5 % 0.063 W 0402
R822	1430700	Chip resistor	10	5 % 0.063 W 0402
R823	1430710	Chip resistor	22	5 % 0.063 W 0402
R830	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R831	1430700	Chip resistor	10	5 % 0.063 W 0402
R832	1430734	Chip resistor	220	5 % 0.063 W 0402
R833	1430700	Chip resistor	10	5 % 0.063 W 0402
R840	1430784	Chip resistor	15 k	5 % 0.063 W 0402
R841	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R842	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R843	1430726	Chip resistor	100	5 % 0.063 W 0402
R850	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R851	1430726	Chip resistor	100	5 % 0.063 W 0402
R852	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R853	1430784	Chip resistor	15 k	5 % 0.063 W 0402
R854	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R855	1430726	Chip resistor	100	5 % 0.063 W 0402
R860	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R861	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R862	1430726	Chip resistor	100	5 % 0.063 W 0402
R864	1430700	Chip resistor	10	5 % 0.063 W 0402
R865	1430700	Chip resistor	10	5 % 0.063 W 0402
R866	1430700	Chip resistor	10	5 % 0.063 W 0402
R867	1430700	Chip resistor	10	5 % 0.063 W 0402
R880	1430700	Chip resistor	10	5 % 0.063 W 0402
R881	1430726	Chip resistor	100	5 % 0.063 W 0402
R886	1430772	Chip resistor	5.6 k	5 % 0.063 W 0402
R893	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R895	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R901	1430700	Chip resistor	10	5 % 0.063 W 0402
R904	1430734	Chip resistor	220	5 % 0.063 W 0402
R906	1430718	Chip resistor	47	5 % 0.063 W 0402
R907	1430690	Chip jumper		0402
R910	1430726	Chip resistor	100	5 % 0.063 W 0402
R911	1430690	Chip jumper		0402
R930	1430726	Chip resistor	100	5 % 0.063 W 0402
R931	1430726	Chip resistor	100	5 % 0.063 W 0402
R933	1430726	Chip resistor	100	5 % 0.063 W 0402
R934	1620101	Res network 0w06 2x470r j	0404	0404
R936	1620031	Res network 0w06 2x1k0 j	0404	0404
R937	1620029	Res network 0w06 2x4k7 j	0404	0404
R938	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R939	1620029	Res network 0w06 2x4k7 j	0404	0404
R940	1800659	NTC resistor	47 k	10 % 0.12 W 0805

R941	1430726	Chip resistor	100	5 % 0.063 W 0402
R942	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R943	1430740	Chip resistor	330	5 % 0.063 W 0402
R960	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R961	1430710	Chip resistor	22	5 % 0.063 W 0402
R980	1430740	Chip resistor	330	5 % 0.063 W 0402
R982	1430690	Chip jumper		0402
C101	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C103	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C104	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C105	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C150	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C151	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C154	2320548	Ceramic cap.	33 p	5 % 50 V 0402
C155	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C157	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C158	2320469	Ceramic cap.		Y5 V 0603
C159	2320469	Ceramic cap.		Y5 V 0603
C160	2320469	Ceramic cap.		Y5 V 0603
C161	2310781	Ceramic cap.	220 n	10 % 16 V 0805
C162	2310781	Ceramic cap.	220 n	10 % 16 V 0805
C163	2320469	Ceramic cap.		Y5 V 0603
C164	2320469	Ceramic cap.		Y5 V 0603
C166	2320469	Ceramic cap.		Y5 V 0603
C167	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C169	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C170	2320469	Ceramic cap.		Y5 V 0603
C171	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C172	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C173	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C174	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C175	2312403	Ceramic cap.	2.2 u	10 % 10 V 1206
C176	2312403	Ceramic cap.	2.2 u	10 % 10 V 1206
C177	2610005	Tantalum cap.	10 u	20 % 16 V 3.5x2.8x1.9
C178	2610005	Tantalum cap.	10 u	20 % 16 V 3.5x2.8x1.9
C179	2604127	Tantalum cap.	1.0 u	20 % 35 V 3.5x2.8x1.9
C180	2320469	Ceramic cap.		Y5 V 0603
C181	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C185	2610005	Tantalum cap.	10 u	20 % 16 V 3.5x2.8x1.9
C187	2320469	Ceramic cap.		Y5 V 0603
C188	2610005	Tantalum cap.	10 u	20 % 16 V 3.5x2.8x1.9
C189	2320469	Ceramic cap.		Y5 V 0603

C190	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C200	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C201	2320469	Ceramic cap.		Y5 V 0603
C202	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C203	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C204	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C205	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C206	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C207	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C209	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C210	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C212	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C214	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C217	2320469	Ceramic cap.		Y5 V 0603
C218	2320469	Ceramic cap.		Y5 V 0603
C219	2320469	Ceramic cap.		Y5 V 0603
C220	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C221	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C223	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C225	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C227	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C228	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C250	2320564	Ceramic cap.	150 p	5 % 50 V 0402
C255	2320564	Ceramic cap.	150 p	5 % 50 V 0402
C256	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C258	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C259	2312296	Ceramic cap.		Y5 V 1210
C260	2312296	Ceramic cap.		Y5 V 1210
C261	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C262	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C263	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C264	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C265	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C266	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C268	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C269	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C270	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C271	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C273	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C275	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C277	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C278	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C279	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C281	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C282	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C283	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C284	2320544	Ceramic cap.	22 p	5 % 50 V 0402

C285	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C286	2320469	Ceramic cap.		Y5 V 0603
C701	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C703	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C706	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C707	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C708	2320520	Ceramic cap.	2.2 p	0.25 % 50 V 0402
C709	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C710	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C729	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C733	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C734	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C735	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C739	2320520	Ceramic cap.	2.2 p	0.25 % 50 V 0402
C741	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C743	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C744	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C745	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C746	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C747	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C748	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C755	2320728	Ceramic cap.	220 p	10 % 50 V 0402
C756	2320618	Ceramic cap.	4.7 n	5 % 25 V 0402
C757	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C758	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C759	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C760	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C761	2320618	Ceramic cap.	4.7 n	5 % 25 V 0402
C762	2320618	Ceramic cap.	4.7 n	5 % 25 V 0402
C763	2320618	Ceramic cap.	4.7 n	5 % 25 V 0402
C764	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C765	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C766	2320592	Ceramic cap.	2.2 n	5 % 50 V 0402
C767	2320618	Ceramic cap.	4.7 n	5 % 25 V 0402
C768	2320618	Ceramic cap.	4.7 n	5 % 25 V 0402
C769	2320618	Ceramic cap.	4.7 n	5 % 25 V 0402
C770	2320618	Ceramic cap.	4.7 n	5 % 25 V 0402
C773	2320618	Ceramic cap.	4.7 n	5 % 25 V 0402
C778	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C779	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C780	2320586	Ceramic cap.	1.2 n	5 % 50 V 0402
C781	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C782	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C783	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C784	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C785	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C786	2320620	Ceramic cap.	10 n	5 % 16 V 0402

C787	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C788	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C789	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C790	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C791	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C792	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C793	2310424	Ceramic cap.	100 p	5 % 50 V 0805
C794	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C795	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C796	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C797	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C798	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C801	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C802	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C803	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C805	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C806	2320604	Ceramic cap.	18 p	5 % 50 V 0402
C807	2611668	Tantalum cap.	4.7 u	20 % 10 V
3.2x1.6x1.6				
C808	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C809	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C810	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C811	2320520	Ceramic cap.	2.2 p	0.25 % 50 V 0402
C815	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C816	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C821	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C824	2610005	Tantalum cap.	10 u	20 % 16 V
3.5x2.8x1.9				
C825	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C830	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C831	2310248	Ceramic cap.	4.7 n	5 % 50 V 1206
C833	2320564	Ceramic cap.	150 p	5 % 50 V 0402
C834	2320564	Ceramic cap.	150 p	5 % 50 V 0402
C840	2320548	Ceramic cap.	33 p	5 % 50 V 0402
C841	2320728	Ceramic cap.	220 p	10 % 50 V 0402
C842	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C843	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C844	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C845	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C850	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C851	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C853	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C854	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C855	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C856	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C857	2320728	Ceramic cap.	220 p	10 % 50 V 0402
C858	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402

C860	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C861	2420017	Ceramic cap.	18 n	5 % 16 V 1206
C864	2320564	Ceramic cap.	150 p	5 % 50 V 0402
C865	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C866	2320564	Ceramic cap.	150 p	5 % 50 V 0402
C867	2611668	Tantalum cap.	4.7 u	20 % 10 V
3.2x1.6x1.6				
C868	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C869	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C881	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C882	2611668	Tantalum cap.	4.7 u	20 % 10 V
3.2x1.6x1.6				
C885	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C886	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C887	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C898	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C900	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C901	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C902	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C903	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C904	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C905	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C906	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C907	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C908	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C910	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C914	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C917	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C920	2320917	Ceramic cap.		25 V 0402
C921	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C923	2320941	Ceramic cap.		10 V 0402
C924	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C925	2320913	Ceramic cap.		25 V 0402
C926	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C927	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C928	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C929	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C930	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C931	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C932	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C933	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C934	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C937	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C938	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C939	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C940	2320602	Ceramic cap.	4.7 p	0.25 % 50 V 0402
C941	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402

C943	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C950	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C951	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C952	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C953	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C954	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C955	2320516	Ceramic cap.	1.5 p	0.25 % 50 V 0402
C960	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C961	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C962	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C963	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C964	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C965	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C967	2320915	Ceramic cap.		25 V 0402
C968	2320921	Ceramic cap.	3.9 p	5 % 16 V 0402
C969	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C970	2320931	Ceramic cap.		25 V 0402
C972	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C980	2320520	Ceramic cap.	2.2 p	0.25 % 50 V 0402
C981	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C982	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C983	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C990	2320602	Ceramic cap.	4.7 p	0.25 % 50 V 0402
C992	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
L103	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L104	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L105	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L150	3203701	Ferrite bead 33r/100mhz 0805		0805
L701	3641572	Chip coil	22 n	5 % Q=45/250 MHz
0805				
L702	3643101	Chip coil	270 n	10 % Q=20/25 MHz
0805				
L703	3640051	Chip coil	12 n	5 % Q=45/250 MHz
0805				
L705	3608319	Chip coil	270 n	10 % 1206
L721	3641521	Chip coil	6 n	5 % Q=50/250 MHz
0805				
L723	3645157	Chip coil	100 n	10 % Q=12/100 MHz
0603				
L724	3608407	Chip coil	470 n	5 % 1206
L741	3641620	Chip coil	180 n	5 % Q=35/100 MHz
0805				
L750	3643067	Chip coil	100 u	5 % Q=15/796 kHz
1008				
L801	3645043	Chip coil	47 n	2 % Q=40/200 MHz
0805				
L840	3641620	Chip coil	180 n	5 % Q=35/100 MHz

0805				
L841	3641575	Chip coil	100 n	5 % Q=40/150 MHz
0805				
L850	3645045	Chip coil		10 % Q=45/10 MHz
0805				
L900	3645157	Chip coil	100 n	10 % Q=12/100 MHz
0603				
L901	3645005	Chip coil	15 n	10 % Q=12/100 MHz
0603				
L902	3645005	Chip coil	15 n	10 % Q=12/100 MHz
0603				
L903	3645005	Chip coil	15 n	10 % Q=12/100 MHz
0603				
L904	3645157	Chip coil	100 n	10 % Q=12/100 MHz
0603				
L905	3645005	Chip coil	15 n	10 % Q=12/100 MHz
0603				
L906	3645157	Chip coil	100 n	10 % Q=12/100 MHz
0603				
L907	3203701	Ferrite bead 33r/100mhz	0805	0805
L930	3645157	Chip coil	100 n	10 % Q=12/100 MHz
0603				
L931	3645157	Chip coil	100 n	10 % Q=12/100 MHz
0603				
L940	3645001	Chip coil	4 n	10 % Q=10/100 MHz
0603				
L950	3645005	Chip coil	15 n	10 % Q=12/100 MHz
0603				
L951	3645001	Chip coil	4 n	10 % Q=10/100 MHz
0603				
L960	3645171	Chip coil	6 n	10 % Q=10/100 MHz
0603				
L961	3645005	Chip coil	15 n	10 % Q=12/100 MHz
0603				
L962	3645005	Chip coil	15 n	10 % Q=12/100 MHz
0603				
L964	3643001	Chip coil	10 n	5 % Q=30/250 MHz
0805				
L980	3645157	Chip coil	100 n	10 % Q=12/100 MHz
0603				
L993	3640013	Chip coil	8 n	5 % Q=50/250 MHz
0805				
B150	4510159	Crystal	32.768 k	+–20PPM
G820	4350121	Vco 985.2–1010.2mhz 2.8v 8ma tdma		TDMA
G850	4510165	VCTCXO	19.44 M	+–2.5PPM 2.8V
G860	4350117	Vco 2046–2106mhz 2.8v 10ma		
F150	5119019	SM, fuse f 1.5a 32v	0603	

Z100	3640069	Filt 47pf 25v 0r01 6a	1206	
Z701	4510121	Saw filter	881.5+–12.5 M	/3.5DB 4X4
Z726	4550053	Cer.filt 1960+–30mhz	8.4x5.95	8.4x5.95
Z741	4511011	Saw filter	116.19+–0.015 M	9.3X5
Z750	4550057	Cer.filt 450+–12.5khz	11.8x7.5	11.8x7.5
Z900	4511031	Saw filter	161.2/196.2 M	5X5
Z901	4510127	Saw filter	836.5+–12.5 M	/3.5DB 4X4
Z910	4512013	Dupl 824–849/869–894mhz	19.2x11.2	19.2x11.2
Z950	4550049	Cer.filt 1880+–30mhz/4.5db	8.4x6.2	
Z951	4511023	Saw filter	1880+–30 M	/4.2DB 3X3
Z960	4512069	Dupl 1850–1910/1930–1990mhz	19x11	19x11
Z961	3640069	Filt 47pf 25v 0r01 6a	1206	
V150	4210037	Transistor	BCW30	pnp 32 V 0.1 A SOT23
V151	4110067	Schottky diode	MBR0520L	20 V 0.5 A SOD123
V152	4210052	Transistor	DTC114EE	npn RB V EM3
V153	4211202	DM MosFet		p–ch 50 V 0.13 A SOT23
V200	4110072	Diode x 2	BAV99W	70 V 0.2 A SOT323
V201	4110072	Diode x 2	BAV99W	70 V 0.2 A SOT323
V202	4110072	Diode x 2	BAV99W	70 V 0.2 A SOT323
V250	4210100	Transistor	BC848W	npn 30 V SOT323
V254	4110072	Diode x 2	BAV99W	70 V 0.2 A SOT323
V741	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323
V800	4219903	Transistor x 2	BFM505	npn 20 V 20V18 mA SOT363
V801	4112441	Pin diode	BA592	35 V 0.1 A SOD323
V802	4110018	Cap. diode	BB135	30 V SOD323
V803	4110027	Cap. diode	SV239	
V840	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323
V850	4210100	Transistor	BC848W	npn 30 V SOT323
V929	4110008	Schottky diode	HSMS2825	8 V SOT143
V930	4110008	Schottky diode	HSMS2825	8 V SOT143
V932	4112469	Pindix2 bar64–07 200v 0.1a sot143		SOT143
D200	4340397	IC, SRAM		STSOP3
D201	4340261	IC, flash mem.		TSO48
D202	4370249	Mad1 rom2 f711857 c12	tqfp144	TQFP144
D203	4340357	IC, EEPROM		SO8
D801	4340126	IC, 1xnand 2input cmos	ssTC7S00F	SSO5
N150	4370391	Ccont2h dct3 bb asic	tqfp64	TQFP64
N151	4370165	Chaps charger control	so16	SO16
N250	4370413	Cobba_d b05 bb asic damps	tqfp64	TQFP64
N701	4370063	Sc3918 tdma rec 869–894mhz	qsop16	QSOP16
N702	4340247	IC, regulator	MC33765	2.8 V TSSOP16
N721	4370065	Sc3919 tdma rec 1930–1990	qsop16	QSOP16

N750	4370273	Plussa txmod+rxif+2pll tqfp64	TQFP64
N880	4340237	IC, PLL UMA1021M	SSOP20
N900	4340171	IC, upconv 1.9ghz 3v so uPC8106T	SO6S
N902	4340515	Fmm5024ml power amp 800mhz sso6	SSO6
N903	4370311	Rf9103p1 pw amp	824–849 mhz
N950	4340517	Fmm5026ml power amp 1900mhz	SSO6
N960	4370313	Rf9111p1 pw amp 1850–1910mhz	
N980	4340381	Mrfic1813 upconvgaas 1.9g tssop16	TSSOP16
X100	5469061	SM, system conn 6af+3dc+mic+jack	
X102	5460021	SM, conn 2x14m spring p1.0 pcb/p	PCB/PCB
X104	5469069	SM, batt conn 2pol spr p3.5 100v	100V2A
X105	5469069	SM, batt conn 2pol spr p3.5 100v	100V2A
X991	5429007	SM, coax conn m sw 50r 0.4–2ghz	
A950	9517018	Shield assembly 3m dmc01006 hd96	HD963
	9854295	PCB UT4R 41.0X124.3X0.9	M6 4/PA