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Digital Voltmeter 7075

Part No. 70750011

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Schlumberger

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TECHNICAL MANUAL

CONTENTS

Servicing: Data Systems Options

Solartron pursue a policy of continuous development and product improvement. The specification in this document thus may be changed without notice.

Operation

SECTION 1 General Description

The 7075, with its simple to use controls and clear, easy-to-read display enables the most inexperienced user to discover that precise digital measurement is now within his grasp.

Automatic range selection means that there is, basically, only one operator decision to be made - that of the quantity to be measured : dc volts, ac volts or resistance. The instrument instantaneously evaluates the order of magnitude of the applied input and selects the appropriate range.

Ranging Points: (5 x 9's)

Range-up $>$ 140 000 digits reading.

Range-down $<$ 12 000 digits reading.

N.B. Excessive series mode signals may cause range-up to occur earlier.

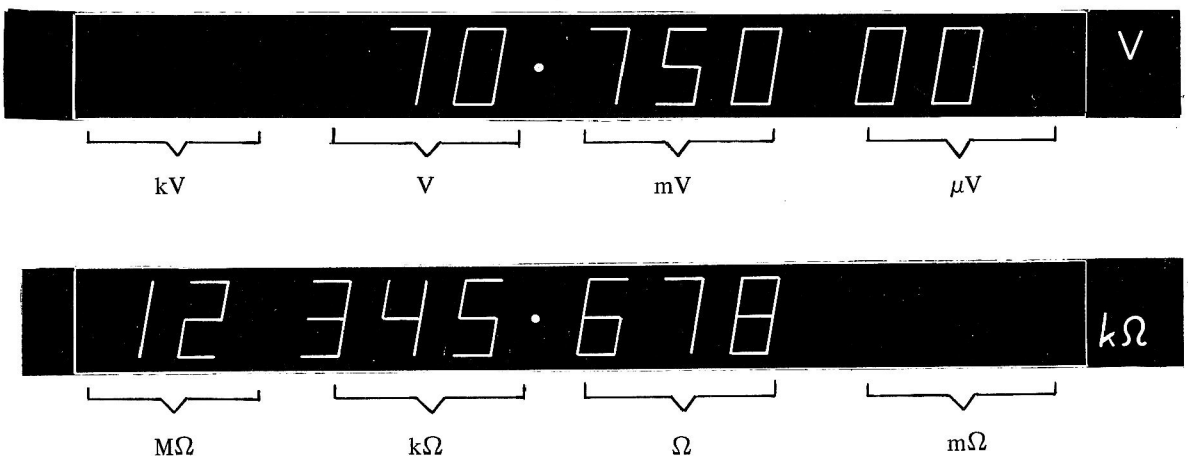
The facilities available are those of:-

DC Voltage	continuous range from 1μV to 1kV
AC (RMS) Voltage	continuous range from 1μV to 750V rms (1.1kV Peak).
Resistance	continuous range from 1mΩ to 14MΩ

True rms measurement: many instruments in the past presented the mean value of an alternating quantity or if rms value was displayed, it was arrived at by some method of 'doctoring' the mean value actually measured. The disadvantage of that system is that validity of the reading is very much dependent on waveform shape, only a pure sinusoidal input giving acceptable results.

The 7075 is a true rms measuring instrument, in which the input is directly converted to its root mean square at the measurement stage. The displayed reading, therefore, is the precisely computed rms value of the alternating quantity being measured.

A twelve decade display is used, bright and sharply defined, no extraneous light being permitted to degrade the displayed reading. The **fixed decimal point** and unique grouping of the displayed digits makes possible an instant appreciation of the order of magnitude of the reading thus obviating the need for multiple and submultiple unit annunciators.



Scale length from 3 x 9's to 7 x 9's can be selected by the user, the above being typical 7 x 9's displays.

The display 'moves' to the right as the applied input reduces in magnitude; leading zeros, except that to the immediate left of the decimal point, are suppressed; and if the quantity is negative the minus sign travels with the display always maintaining its position immediately to the left of the most significant whole digit.

The new conversion technique used is capable of obtaining linearities two orders better than those possible using dual ramp and related techniques. An important property of this method is that the applied input is being continuously averaged. Together with the very fast autoranging system, this feature makes conventional filters, with their associated problems, unnecessary. A new exclusive **digital filtering** technique is utilised whereby the difficulty that used to be associated with low frequency ac measurement has, with the 7075, become a thing of the past.

Operator confidence is increased by a self check facility. At the touch of a button the instrument can be commanded to carry out a series of tests designed to prove the correct functioning of all its circuits, displaying the result of each check instantaneously.

SAFETY

Your 7075 has been carefully engineered with ease of use as one of the primary considerations. Attention has also been given to making the instrument immune to most inadvertent overloads and to ensuring operator safety. However it should be appreciated that even the most sophisticated of measuring instruments can be dangerous when connected to high voltages, unless elementary safety precautions are observed.

The voltage limit of 1.1kV means that no damage will be caused to the instrument at this level of input. Other than the displayed reading, however, no indication is given to the user that a voltage of such a magnitude is present at the input terminals. Care should therefore be exercised whenever the dvm input leads are being connected to/removed from live circuits, especially where high voltages are known to exist or high transients could occur.

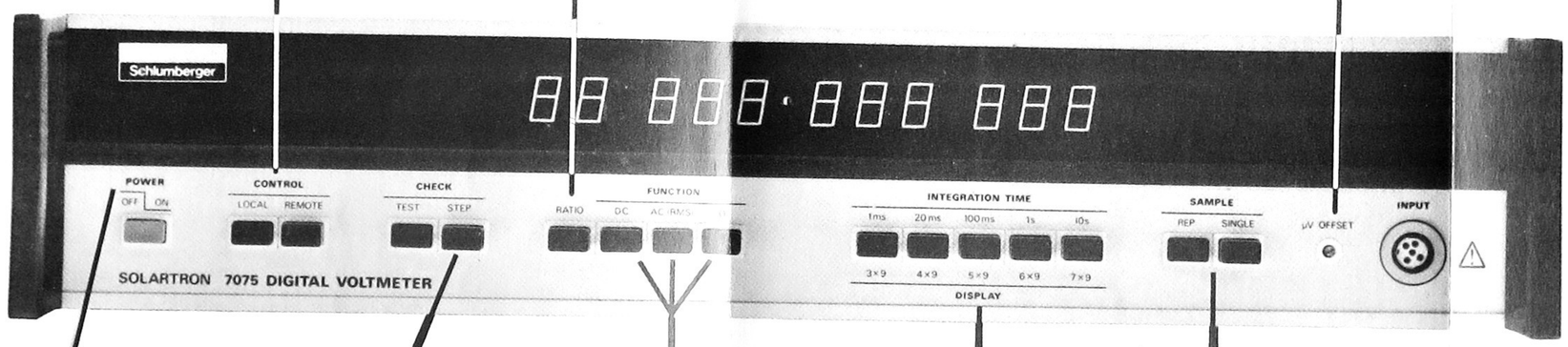
Similarly, when using the instrument on mains operated equipment capable of delivering high voltage outputs, it is strongly recommended that the equipment under test is NOT switched off with the dvm still connected. For example, consider the 7075 connected across the secondary winding of a large mains transformer. The instrument's very high input resistance is such that, in the event of the mains supply being interrupted, the resultant back emf induced in the undamped secondary could be of the order of 100kV. This is obviously hazardous to the user and would certainly harm the voltmeter.

A High Voltage Probe (70757A) may be used with the 7075. Before the High Voltage Probe is used, careful attention must be paid to the safety precautions listed on page 3.4

CONTROL: Permits operation by means of front panel switches, when on LOCAL; or under the control of an external system when REMOTE is selected. REMOTE has no effect in the absence of an Interface Unit. (Note 1).

RATIO: Disconnects internal reference and connects external reference applied to the rear input terminals.

μV OFFSET: Facility for offsetting the effects of externally generated emf's. Applicable on DC and Ω.



DC, AC (RMS), Ω: Used for selection of measurement mode.

TEST: Initiates a series of self-check operations.

STEP: Progresses the test routine step-by-step.

POWER: Push-on/push-off. Applies mains power to the instrument. No remote control facility.

INTEGRATION TIME: Choice of 5 scale lengths by selecting one of 5 integration periods. The longer scale lengths give greater resolution.

REP: Display is repeatedly updated at a rate set by the selected Integration Time.

SINGLE: Display retains last commanded reading. Update occurs each time button is pressed (Note 2).

NOTES

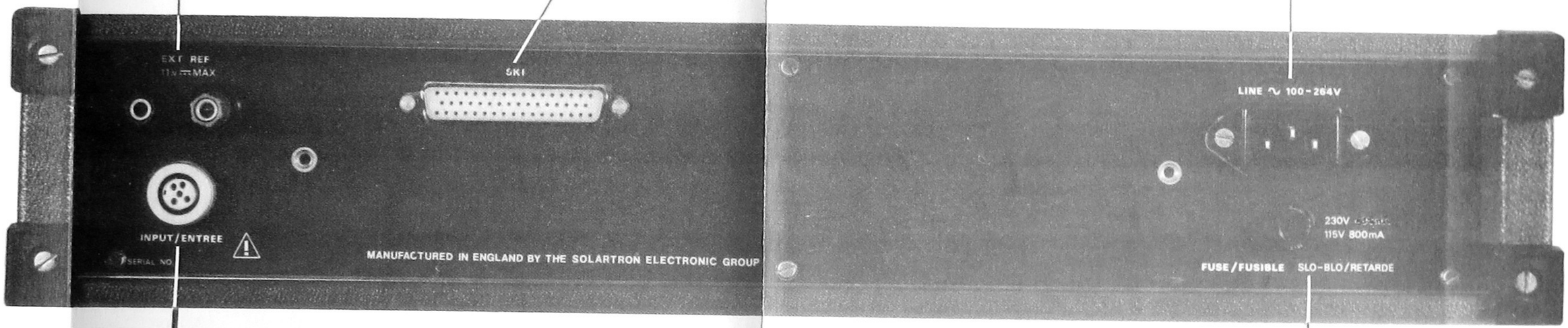
1. An external command from the Interface Unit, FRONT PANEL LOCKOUT, can be used to inhibit all front panel controls (except POWER).

2. When in SINGLE operation, changes of FUNCTION or INTEGRATION TIME will not be implemented until the SINGLE button is again pressed.

CONNECTOR SOCKET SK1 for use with Systems Interface Unit or data processing options.

EXTERNAL REFERENCE terminals used only for RATIO measurement.

POWER INLET SOCKET. No voltage tappings are required over the stated range.



REAR INPUT SOCKET wired in parallel with normal front input.

SUPPLY FUSE: 800mA value for both 115V and 230V supply voltage.

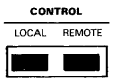
CONTROLS

The push button controls are arranged in groups in accordance with the decisions which have to be made for any measurement.

1. POWER

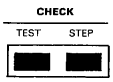
This mains switch operates with a push on - push off action and is clearly marked to indicate whether on or off. The display is always illuminated when the instrument is switched on, thus obviating the need for separate button illumination. The switch cannot be remotely controlled, however remote switch-off can be achieved by interrupting the power supply.

2. CONTROL



With the (optional) interface unit fitted, selection of LOCAL inhibits the effect of all remote command inputs except FRONT PANEL LOCKOUT (a command signal from the interface unit) and control is via the front panel push buttons. When REMOTE is selected all functions except SAMPLE are controlled by remote command inputs (see Section 5). the remaining three groups of push-buttons being disabled. With no interface unit fitted selecting REMOTE has no effect.

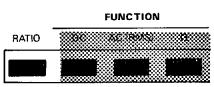
3. CHECK



When TEST is selected the Self Test programme is initiated, designed to check the overall function of the instrument. Progression from one test to the next is effected by pressing the STEP button. The 5 tests check the function of:-

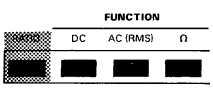
1. The DC Measurement system	Should display 7V DC ± 0.005V
2. The A - D converter internal zero	Should read zero ± 0.0002V
3. The AC converter	Should display 10V AC ± 0.01V
4. The Ohms converter	Should display 10kΩ ± 0.02kΩ
5. The Display	Should display a "full house" of eleven 8's.

4.a. RATIO



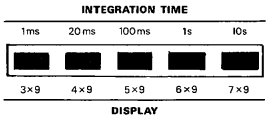
This push on - push off switch, when selected, replaces the internal reference with the user's choice of external reference applied to the terminals on the Rear Panel. A suitable reference voltage between 2 and 11 volts should be used. This function is not available with resistance measurement.
N.B. It is important to disconnect any external reference supply when not making Ratio measurements.

b. FUNCTION



These three push buttons are mechanically linked, mutually exclusive and left-justified electronically. The mechanical linkage ensures that, barring misuse, selection of one switch automatically disengages any other which had previously been selected. Should accident or misuse result in the forcing in of two of these buttons simultaneously, left-justification causes the left hand one of the pair to be the function selected electronically.

5. INTEGRATION TIME

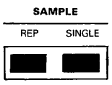


Each push button selects one of five available measurement times and, as can be seen from the legend below the switches, causes the display length to vary between 3 × 9's and 7 × 9's. The switches are of the mutually exclusive mechanically linked type with left justification as described above (4b).

The tables in Section 2 show the results of varying integration time. It should be particularly noted here, however, that when the longer integration times are used, there is a finite delay between successive updatings of the reading. This lengthening of the conversion time is true for both REP and SINGLE operation. During the delay any alteration the operator might make to the front panel controls will not be effective.

For more detailed information on the significance of integration time, the user is referred to Section 4 (Measurement Techniques).

6. SAMPLE



When REP is selected (i.e. normal operation) the instrument makes repeated readings at the rate determined by the selected Integration Time, each reading updating the display. When SINGLE is selected the display presents the next complete reading, and holds it. Updating of the displayed information is achieved by a further pressing of the SINGLE button, which initiates one further measurement. As a safety precaution the autorange circuits will still cause range-up while SINGLE is selected and overload protection remains operative. However care must still be exercised to ensure that the specified limits of input for the displayed mode of operation are never exceeded.

7. μV OFFSET

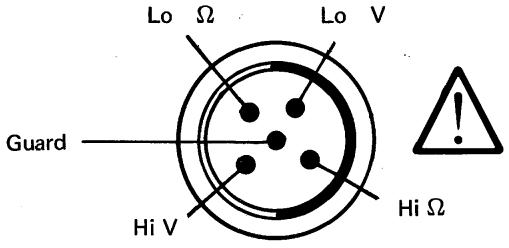
The instrument's internal zero is extremely stable and no operator adjustment is necessary. The μV OFFSET is provided to 'back-off' any small disturbances to the instrument zero which might be generated externally to the dvm. In those applications where, for example, thermal effects generated in the external circuit could be of significance and degrade the measured result, use of the μV offset will provide a correction of approximately $\pm$ 10μV.

FRONT PANEL LOCKOUT

Not apparent from the front panel legends is a facility known as Front Panel Lockout. Under the control of an external electrical command applied via the optional interface unit the action of all front panel controls, except POWER, can be inhibited. This command signal even disables "LOCAL" and can be used to prevent unauthorised use of the dvm when it is committed within a system or, with suitable remote programming, enables a test sequence to include both automatic and manual control.

INPUT CONNECTOR

The input connector simply pushes into the front panel socket with a 'snap-in' action. This cannot be released by pulling on the cable, but separation occurs when the skirt of the connector is pulled away from the panel.



Input connector socket, showing pin identification (front panel view).

The skirt of the connector acts as an isothermal chamber thus preventing errors which could otherwise result from temperature differentials across the input terminals.

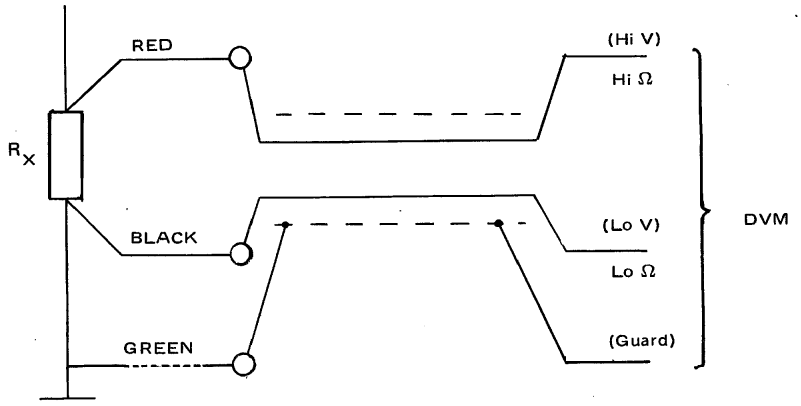
Three types of input lead are available as follows:-

(a) **2 Way Lead** (supplied as standard).

This input lead may be used for all standard measurements. The RED lead is connected to HiV and should be used as Hi, normally at the largest potential with respect to earth. The BLACK lead is connected to LoV and provides the return path. The 2 cores are enclosed in a braided screen which is connected to Guard. At the free-end of the cable, this screen is connected to the black lead thus effectively preserving the guard right up to the signal source. This prevents the measurement being affected in any way by common mode current flowing in the screen and via leakage to earth. The input may be floated above mains' earth by up to 500V, the use of higher common mode voltages is not recommended purely to ensure safety for equipment and the user. The guard is not made available as a separate termination.

(b) **3 Way Lead**

In some rare measurement situations, common mode voltages can have an affect on the readings. Most users will never encounter the problem, but those who do can still eliminate error by using this lead which has 2 cores and a screen which is available to the user. The RED should be used for Hi and the BLACK for Lo as above. The screen is available as Guard and colour-coded GREEN.



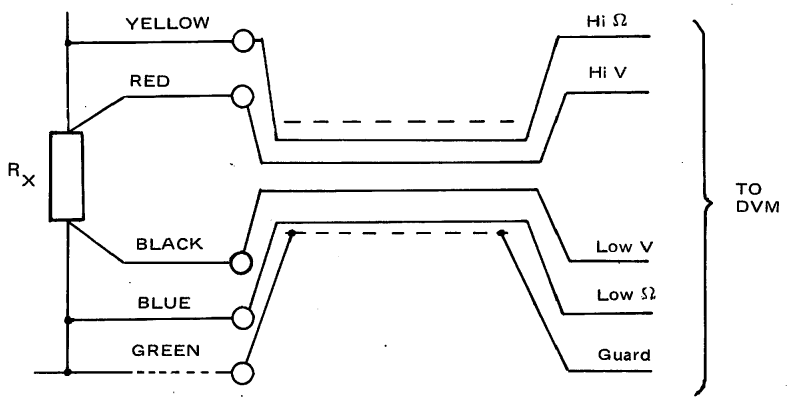
Note. In both (a) and (b) HiΩ and LoΩ are internally connected within the lead to HiV and LoV respectively. The same lead can thus be used for both voltage and resistance measurement.

When the 3-way lead is not being used as illustrated the GREEN wire should be connected to Lo (BLACK).

(c) **5 Way Lead**

This lead has 4 cores and a screen which is available to the user. The RED lead is connected to HiV, the BLACK lead to LoV, the YELLOW to HiΩ, the BLUE to LoΩ and the GREEN to GUARD.

When measuring low values of resistance, the voltage dropped along the leads can sometimes introduce errors. This effect may be eliminated by employing the 4 wire technique in which two wires supply the current to the resistor and two others sense the potential developed across it.



The example shows the correct method of using the lead, the order of connections is important, i.e. the RED and BLACK leads should be as close to the resistor as possible. The GREEN (guard) may be used as previously detailed to reduce common mode interference if this introduces errors.

These and other leads are available to order as Optional Accessories. (see full Accessories List Section 2).

To preserve the integrity of readings obtainable with this instrument it is recommended that only copper connecting clips, as supplied, are used with the input connector.

Rear Input

A rear input socket is fitted as standard, wired in parallel with the normal front input. This is provided as an alternative (e.g. in rack mounting use of the instrument) and connections should never be made to both front and rear input sockets.

N.B. The symbol which appears in places on the instrument of an exclamation mark enclosed within a triangle, ⚠ , is an indication to the user that reference should now be made to relevant sections of this book.

A pull-out instruction card, repeating the basic operating parameters, is mounted below the front panel.

DISPLAY

The display area is covered by a tinted screen laminated with a circularly polarised membrane to inhibit stray light or reflected light which might otherwise reduce the clarity of the reading. The front surface is lightly frosted to eliminate surface reflection from overhead lights or light coloured garments worn by the user. Very slight de-focussing results from this frosting.

The reading is updated at the selected integration rate or on pressing the SINGLE button as described earlier.

From left to right the displayed information is:-

(a) RATIO Selection of RATIO operation illuminates this legend.

(b) ∿ This sign is displayed when AC (RMS) is selected.

(c) **Numerical Indication.** Plasma discharge tubes are used to present the result of measurement. The numerals are grouped in threes, for ease of reading.

(d) **Decimal Point.** This is a fixed point, floating display instrument, leading zeroes being suppressed.

(e) **Units.** V and kΩ annunciators are illuminated as a result of selecting the required mode of measurement with the FUNCTION buttons.

(f) REMOTE An indication that the instrument is under REMOTE control - only applicable when the (optional) interface unit is fitted.

BUSY Should this legend be illuminated it advises the operator that the reading currently being displayed should be regarded as invalid. The legend is extinguished when the new result is displayed. The BUSY signal has the additional function of inhibiting the front panel push buttons. Thus once a command has initiated a measurement, the instrument will not abort that reading.

INVALID READINGS

In addition to 'BUSY' described above, an indication that a reading is invalid is that of a flashing display. Normally this occurs as a result of an overload on the range in use. Notwithstanding this automatic warning, the user is reminded that **the limits of input specified should never be exceeded.**

The limits are:-

DC **1100V DC**

AC **750V RMS (1100V Peak)**
above 20kHz limit is 200V RMS
400V dc when on AC

N.B. These limits only apply to LOCAL operation - for details of limits applicable when instrument is under REMOTE control see Technical Specification and Section 5.

RACK MOUNTING

The overall dimensions conform to international standards for rack mounting. The instrument can if desired be rack mounted within its case, no additional protection being necessary. Users who so wish can remove the covers which are simply secured by four screws. For rack mounting either the handle-less rack mounting fittings, or the combination handle/ears should be substituted for the normal handles. Rack mounting fixtures of both types are included in the accessory pack supplied with the voltmeter, (See Accessories list in Section 2).

SECTION 2 Specifications and General Information

This section contains a copy of the technical specification applicable to the voltmeter.

The 7075 has been designed and manufactured to the highest specification possible for an instrument of its type. Where typical figures are quoted, they are realistic estimates of obtainable performance based on known component tolerances and stability. Guaranteed performance, on the other hand, is specified from the results of exhaustive tests, stringently controlled, applied to every instrument produced. "Worst-case" figures are quoted in many instances, hence your 7075 may be found to exhibit a performance better in some particulars than the tables suggest. However no additional claims are made for the instrument above that published in the current data sheet.

SPECIFICATIONS

Manufacturers calibration temperature 20°C.

Table 1 GUARANTEED PERFORMANCE 1s Integration

Nominal Range	Input Sensitivity	Displayed Full Scale	Limits of Error 24 hrs ± 1°C ±[% rdg. + % f.s.]		6 mnth ± 5°C ±[% rdg. + % f.s.]		1 yr ± 5°C ±[% rdg. + % f.s.]		Input Resistance
10mV	1μV	0.013 999V	———	0.007		0.007		0.007	> 10GΩ
100mV	1μV	0.139 999V	0.0014	0.0014	0.002	0.0014	0.003	0.0014	> 10GΩ
1V	1μV	1.399 999V	0.0006	0.0004	0.002	0.0008	0.003	0.001	> 10GΩ
10V	10μV	13.999 99 V	0.0003	0.0002	0.0015	0.0005	0.002	0.0008	> 10GΩ
100V	100μV	139.999 9 V	0.0007	0.0005	0.003	0.0008	0.004	0.001	10MΩ
1000V	1mV	1 000.000 V	0.0007	0.0007	0.003	0.0008	0.004	0.001	10MΩ

Table 2 TYPICAL PERFORMANCE 10s Integration

Nominal Range	Input Sensitivity	Displayed Full Scale	Limits of Error 24 hrs ± 1°C ±[% rdg. + % f.s.]		6 mnth ± 5°C ±[% rdg. + % f.s.]		1 yr ± 5°C ±[% rdg. + % f.s.]		Input Resistance
10mV	1μV	0.013 999V		0.007		0.007		0.007	15GΩ
100mV	1μV	0.139 999V		0.0007	0.001	0.0007	0.0015	0.0007	20GΩ
1V	1μV	1.399 999V	0.0004	0.00015	0.001	0.0003	0.0015	0.0005	200GΩ
10V	1μV	13.999 999V	0.00015	0.0001	0.0005	0.00025	0.001	0.0004	1000GΩ
100V	10μV	139.999 99 V	0.0005	0.0002	0.0015	0.0005	0.002	0.0007	10MΩ
1000V	100μV	1 000.000 0 V	0.0005	0.0003	0.0015	0.0005	0.002	0.0008	10MΩ

Reduced scale lengths

Scale Length	Integration Time	Input Sensitivity	Limits of Error [1 year ± 5°C]
5 x 9	100ms	1μV	± 0.004% rdg ± 1 digit ± 1μV
4 x 9	20ms	1μV	± 1 digit ± 2μV
3 x 9	1ms	10μV	± 1 digit ± 10μV

Temp. coeff.

Range	<± [% rdg. + % f.s.] per °C	
10mV	0.0004	0.0015
100mV	0.0004	0.0002
1V	0.0004	0.0001
10V	0.0002	0.00007
100V	0.0005	0.0001
1000V	0.0005	0.0001

Zero offset <± 0.2μV per °C

Input Current
Typically < 20pA at 20°C

Overload protection:
Autorange: 1.1kV
Commanded ranges:
up to 10V: 350V
100V & 1000V: 1.1kV

Linearity:
error due to non-linearity is less than 1ppm and is included in the above specification.

Temperature corrections:
need be applied only when operating beyond the temperature limits quoted under Limits of Error.

Manufacturers calibration temperature 20°C.

Performance guaranteed above 10% of f.s. (i.e. Range-change point).

Table 3 24 hrs at 20°C ± 1°C 1s integration

Nominal Range	Input Sensitivity	Displayed Full Scale	Limits of Error 10Hz to 40Hz	40Hz to 10kHz	10kHz to 100kHz
100mV	1μV	0.139 999V	± 0.3% rdg. ± 0.05% f.s.	± 0.05% rdg. ± 0.05% f.s.	± 0.5% rdg. ± 0.2% f.s.
1V	10μV	1.399 99 V			
10V	100μV	13.999 9 V			
100V	1mV	139.999 V			
1000V	10mV	750.00§ V	± 0.3% rdg. ± 0.1% f.s.	± 0.05% rdg. ± 0.1% f.s.	± 0.5% rdg. ± 0.4% f.s.

§Above 20kHz: 200V rms max.

Table 4 6 months at 20°C ± 5°C 1s integration

Nominal Range	Limits of Error 10Hz to 40Hz	40Hz to 10kHz	10kHz to 100kHz
100mV, 1V	± 0.4% rdg. ± 0.08% f.s.	± 0.1% rdg. ± 0.06% f.s.	± 0.5% rdg. ± 0.2% f.s.
10V, 100V	± 0.4% rdg. ± 0.08% f.s.	± 0.1% rdg. ± 0.06% f.s.	± 0.7% rdg. ± 0.2% f.s.
1000V	± 0.4% rdg. ± 0.08% f.s.	± 0.1% rdg. ± 0.1% f.s.	± 0.7% rdg. ± 0.4% f.s.

Table 5 1 year at 20°C ± 5°C 1s integration

Nominal Range	Limits of Error 10Hz to 40Hz	40Hz to 10kHz	10kHz to 100kHz
100mV, 1V	± 0.5% rdg. ± 0.1 f.s.	± 0.15% rdg. ± 0.1% f.s.	± 0.6% rdg. ± 0.2% f.s.
10V, 100V	± 0.5% rdg. ± 0.1% f.s.	± 0.15% rdg. ± 0.1% f.s.	± 1.0% rdg. ± 0.2% f.s.
1000V	± 0.5% rdg. ± 0.2% f.s.	± 0.15% rdg. ± 0.2% f.s.	± 1.0% rdg. ± 0.4% f.s.

Other integration times

Time	Sensitivity	Scale Length	Min. Frequency*	Specification
10s	1μV	139 999	as Tables 3 to 5	as Tables 3 to 5
100ms	1μV	139 999	40Hz	as Tables 3 to 5
20ms	10μV	13 999	100Hz	add ± 0.01% f.s.
1ms	100μV	1 399	400Hz	add ± 0.1% f.s.

*< 40Hz best performance is given by 1s or 10s integration.

Temp. coeff.

Range	<± [% rdg. + % f.s.] per °C	
100mV	0.015	0.004
1V	0.015	0.004
10V	0.015	0.004
100V	0.015	0.004
1000V	0.015	0.004

Overload protection:

100mV & 1V ranges:	350V peak
10V, 100V, 1000V ranges:	1.1kV peak
All ranges, above 20kHz:	200V rms

Crest factor: 5 : 1 at f.s.

Input impedance:

at input socket:	1MΩ//< 150pF
of standard input cable:	< 300pF

Very low frequency measurement:
Useful readings can be made down to 1Hz with <1dB error by employing the 10s integration time.

Temperature corrections:
need be applied only when operating beyond the temperature limits quoted under Limits of Error.

Manufacturers calibration temperature 20°C.

Table 6 GUARANTEED PERFORMANCE 1s integration

Nominal Range	Input Sensitivity	Displayed Full Scale	Limits of Error 24 hrs ± 1°C ±[% rdg. + % f.s.]		6 mnth ± 5°C ±[% rdg. + % f.s.]		1 yr ± 5°C ±[% rdg. + % f.s.]		Measuring Current
10Ω	1mΩ	0.013 999kΩ		0.014		0.014	0.01	0.014	1mA
100Ω	1mΩ	0.139 999kΩ	0.001	0.002	0.003	0.002	0.005	0.002	1mA
1kΩ	1mΩ	1.399 999kΩ	0.002	0.0005	0.003	0.001	0.005	0.0015	1mA
10kΩ	10mΩ	13.999 99 kΩ	0.002	0.0003	0.0025	0.0008	0.004	0.001	1mA
100kΩ	100mΩ	139.999 9 kΩ	0.001	0.0005	0.003	0.001	0.006	0.0015	10μA
1MΩ	1Ω	1 399.999 kΩ	0.001	0.0003	0.003	0.001	0.006	0.0015	10μA
10MΩ	10Ω	13 999.99 kΩ	0.002	0.001	0.006	0.0015	0.008	0.0015	1μA

Maximum dissipation in unknown: 14mW Maximum overload: 250V rms Maximum Voltage, Lo current/Lo sense: 10V peak.

10s integration time: specification as above, but having one additional decade displayed on ranges 10kΩ and above.

Reduced scale lengths

Scale Length	Integration Time	Input Sensitivity	Limits of Error 1 year ± 5°C
5 x 9	100ms	1mΩ	± 0.008% rdg. ± 1 digit ± 1mΩ
4 x 9	20ms	1mΩ	± 1 digit ± 2mΩ
3 x 9	1ms	10mΩ	± 1 digit ± 10mΩ

Open circuit condition:
A source resistance of 1000GΩ ensures full protection to external circuits.

Temp. coeff.

Range	<± [% rdg. + % f.s.] per °C	
10Ω	0.0007	0.0015
100Ω	0.0007	0.0002
1kΩ	0.0007	0.0001
10kΩ	0.0005	0.00007
100kΩ	0.0007	0.0001
1MΩ	0.0007	0.0001
10MΩ	0.0012	0.0001

Zero offset <± 0.2mΩ per °C

Temperature corrections:
need be applied only when operating beyond the temperature limits quoted under Limits of Error.

RATIO FACILITY

Reference Voltage:	2 to 11V
Input Resistance:	Ref Hi to Ref Lo: 2 MΩ
	Ref Hi to Sig Lo: 1.7MΩ
	Ref Lo to Sig Lo: 1.7MΩ
Reference Overload:	100V peak differential
	100V peak either terminal to Sig Lo.
Limits of Error	
1 yr at 20°C ± 5°C:	± [Normal % rdg. + 0.005% rdg. + (Normal % f.s. + 0.005% rdg.) $\frac{10}{V_{Ref}}$]
Temperature Coefficient:	± [Normal % rdg. T.C. + 0.001% rdg. + (Normal % f.s. T.C. + 0.001% rdg.) $\frac{10}{V_{Ref}}$]

Ratio of peak interference to 1 digit reading error.

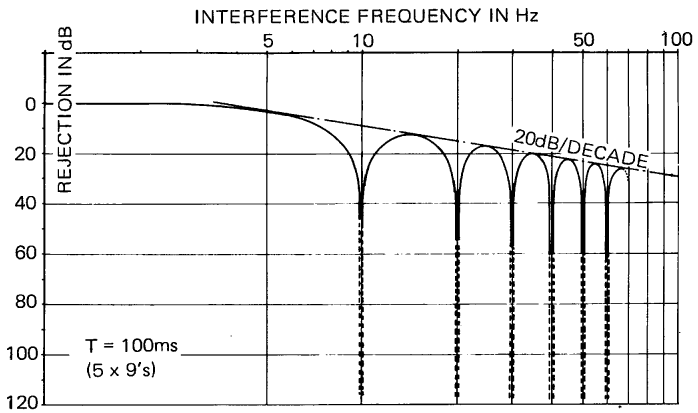
Series mode

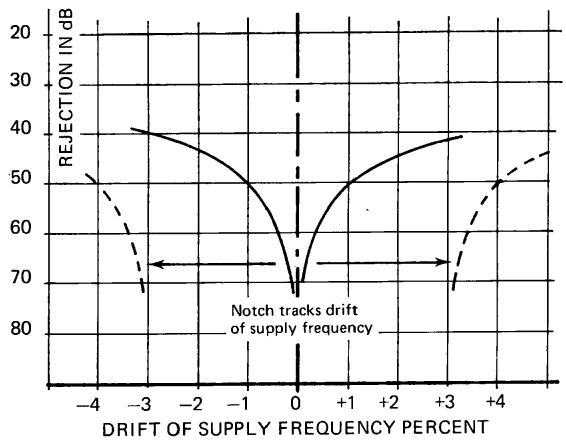
Maximum Series Mode:	Autorange:	1.1kV pk
	Command Range:	1.5 x V_{Range}
DC Measurement:	Rejection of 50 (60) Hz ± 3%	> 70dB
Ratio Measurement:	Rejection of 50 (60) Hz ± 3% at Ref.	> 40dB

Effective common mode

Measured with 1kΩ imbalance in Lo lead.

Maximum Common Mode:		500V dc or peak ac.
DC Measurement:	Rejection of dc:	> 150dB
	Rejection of 50 (60) Hz ± 3%:	> 144dB
AC Measurement:	Rejection of dc:	> 150dB
	Rejection of 50 (60) Hz ± 3%:	> 74dB
Ratio Measurement:	Max. Common Mode Ref. Hi or Lo to Sig Lo:	30V
	Rejection of Common Mode Ref Lo to Sig Lo with up to 80Ω lead imbalance:	> 80dB





In the measurement of dc voltage 7075 gives the mean (average) value of the input during the chosen integration time. Except for 1ms, the times are multiples of the period of the mains supply. Hence the curves for interference rejection exhibit deep notches at discrete frequencies, those for 100ms shown above having a notch every 10Hz. By using the 10s integration the notches become spaced at only 0.1Hz intervals. Furthermore the tangent to the peaks, while retaining the slope of 20dB/decade, is spaced 20dB lower on 1s integration and 40dB lower on 10s integration.

The precise integration time is locked to the period of the mains supply by a digital servo. The notches move to right or left as supply frequency changes thus preserving maximum rejection up to a shift of ± 3%. This is beyond the limit of frequency deviation specified for the national grid.

Environment

Working Temperature Range:	0 to + 50°C.
Storage Temperature Range:	–30 to + 70°C.
Maximum Relative Humidity:	70% at + 40°C.

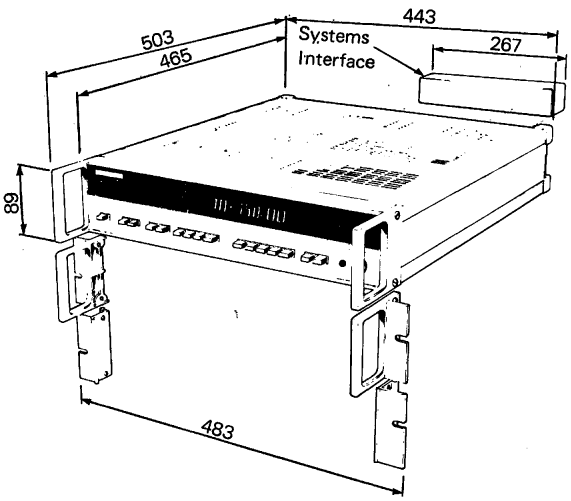
Other specifications to Solartron spec. 50/01/102.

Power supply

Voltage:	100 to 264V (no mains tap).
Frequency:	50(60)Hz ± 3%. Internal switch provides optional 400Hz operation. The instrument is capable of operating up to 2400Hz supply frequency.
Consumption:	Approx. 65VA (35W)
Fuse	800mA Slo Blo

Dimensions

Width:	443mm	(17.4ins)	Rack mounting depth,
Height:	89mm	(3.5ins)	over interface + cable:
Depth:	465mm	(18.3ins)	533mm (21ins).
Weight:	9.1kg	(20lbs)	



Safety

This instrument conforms to IEC 348 recommendations.

Accessories

Included Accessories		Part No.
Input Cable		A2000168
Crocodile Clip (copper)		355901030
Test Probe	Red	351901020
Test Probe	Black	351901010
Spare fuse	800mA	360106310
Mains cable		480140220
Rack mounting handles	(2 off)	429700101
Rack mounting ears	(2 off)	469601201
Operating Manual		70750010
Technical Manual		70750011

Optional Accessories	Part No.
Systems Interface (Parallel BCD)	70754A
Systems Interface (IEC TC66/IEEE 488)	70755A
High Voltage Probe	70757A
3-Terminal input lead	3193
5-Terminal input lead	3183
Telescopic Rack Slides (pair)	70759A
ESI Kelvin clip leads (pair)	70758E
Low thermal lead kit	70758D
Master Series adaptor lead	70758G
Service kit	70759C
Calibration cover	70759D

High voltage probe (70757A)

Extends measurement of dc voltage to 20kV. Complete with fittings and adaptors.

Voltage Range:	1kV to 20kV
Division Ratio:	
at 20kV, 23°C	x 100
Limits of Error:	
1kV to 20kV, 23°C	±5%
Working Temp:	0°C to +50°C
Temp Coeff:	−1500 to −2000ppm/°C
Input Resistance:	1,000MΩ at ±5%
Max. Input Voltage:	20,000 Volts
Lead Length:	1.8m

SECTION 3 Operating Instructions

PRELIMINARIES

Check that the correct fuse is fitted, 800mA SLO-BLO

Connect a suitable plug to the mains lead:-

BROWN	LINE
BLUE	NEUTRAL
GREEN/YELLOW	EARTH

N.B. It is important that this Earth connection is made.

Operation at other than 50Hz supply frequency

The link for 60Hz operation and the switch for 400Hz operation are positioned on board 2, on the right hand side of the instrument. Access to these necessitates partial removal of the cover.

The adjustment procedure for 60Hz operation is given in Section 8 of the 7075 Technical Manual.

The instrument should be disconnected from the mains supply before any attempt is made to remove the cover.

DC VOLTAGE MEASUREMENT

1. Switch POWER on.

2. Select LOCAL, unless Remote operation with optional interface unit is required. (In that instance refer to Section 5).

3. Ensure TEST and RATIO push buttons are released.

4. Select DC.

5. Select INTEGRATION TIME for the resolution, noise rejection and reading rate that are required.

6. Connect input lead to the unknown voltage source - BLACK lead to signal Low, RED to signal High (in that order).

7. Select REP for repetitive display of measurement or press SINGLE for each single reading required. 'V' will now be illuminated.

8. Read the displayed value. The indicated polarity is that of the red lead with respect to the black. (Polarity is positive unless the minus sign is illuminated).

   The user is referred to Section 4 for further information on measurement technique, and the significance of varying Integration Time.

AC VOLTAGE MEASUREMENT (True RMS)

1. Switch POWER on.

2. Select LOCAL, unless Remote operation with interface unit is required. (In that instance refer to Section 5).

3. Ensure TEST and RATIO push buttons are released.

4. Select AC (RMS).

5. Select INTEGRATION TIME for the resolution, noise rejection and reading rate that are required.

Note. A maximum of 5 x 9's reading can be obtained, selection of 1s or 10s resulting in a quieter display at low frequencies, by a process of Digital Filtering (the user is referred to Section 4 for more detailed information on the significance of Integration Time when measuring AC).

6. Connect input lead to the unknown Voltage source.

7. Select REP for repetitive display of measurement or press SINGLE for each single reading required. The ∿ sign will be illuminated.

8. Read the displayed value.

CURRENT MEASUREMENT

Although not a facility directly provided by this instrument, current measurement can be easily effected by measuring the potential difference developed across a known precision resistor, either a resistance Standard or a precision wire wound component. For ac measurement a metal film precision resistor is recommended.

RATIO MEASUREMENT DC/DC and AC/DC (True RMS)

Without RATIO selected, all instrument measurements are made with reference to an internal reference supply.

With RATIO selected an external reference supply (between 2V and 11V dc) must be connected to the rear terminals and all instrument measurements are then referenced to this supply. The relationship between input and the display becomes:-

$$V_{out} = \frac{10V_{in}}{2<V_{ref}<11}$$

where V_{out} is the displayed reading, V_{in} is the applied voltage and V_{ref} is the chosen value of external reference.

After the external reference supply is connected, RATIO measurement operation is as for normal operation. The ratio is,

$$\frac{\text{displayed reading}}{10}$$

RESISTANCE MEASUREMENT

1. Switch POWER on.
2. Select LOCAL, unless remote operation with interface unit is required. (In that instance refer to Section 5).
3. Ensure TEST and RATIO push buttons are released.
4. Select Ω.
5. Select INTEGRATION TIME for the resolution, noise rejection and reading rate that are required.
6. Connect input lead to the unknown resistance.
7. Select REP for repetitive display of measurement or press SINGLE for each single reading required. The kΩ annunciator will be illuminated.
8. Read the displayed value.

   For details of 4 terminal measurement and other refinements of technique the user is referred to Section 4 of this manual.

HIGH VOLTAGE PROBE (70757A)

The H.V. Probe effectively increases the dc voltage range of the 7055/65/66/75 models to a maximum of 20kV. The displayed reading should be multiplied by 100 to obtain the true reading.

Safety Precautions

When using the H.V. Probe, the following safety precautions should be observed:

1. Do not use any of the 7055/65/66/75 instruments in the Autoranging mode as damage is likely to occur.

2. On the 7055/65/66 models, the instrument must be set on the 1000V dc range.

3. On the 7075 model, the 50-way Cannon plug must be inserted in the back of the instrument, to hold the instrument on the 1000V dc range.

4. Know the instrument under test; locate all high voltage points before commencing work.

5. Do not work alone.

6. Do not depend on the insulation of high voltage cables for protection.

7. Remember that high voltage may appear at unexpected points in defective equipment. Furthermore, bleeder resistors may be open and capacitors may retain high voltages even through power is off.

8. High voltages can discharge from point to point or from point to air (corona). Keep hand closed on handle of probe and away from all high voltage points.

9. Keep hands, shoes and test areas absolutely dry.

10. Ensure that the surface of the probe is clean and moisture free.

11. BEFORE MAKING ANY MEASUREMENTS, ENSURE THAT THE GROUND LEAD OF THE PROBE IS CONNECTED TO THE LOW POTENTIAL OR GROUND SIDE OF THE HIGH VOLTAGE SUPPLY BEING MEASURED'

SECTION 4 Measurement Techniques

The following notes are written for those users who wish to know more about the techniques of precision measurement. They also provide the user with a guide as to how he can obtain the optimum performance from the dvm in more unusual applications and avoid some of the pitfalls.

INPUT RESISTANCE

In making a measurement of voltage virtually all instruments take a current from the voltage source. The one exception is the true potentiometer in which, at balance, the current drawn falls to zero. The current drawn by the measuring device causes a voltage drop across the internal resistance of the source such that the voltage measured is less than the true emf of the source. (Fig. 4.1).

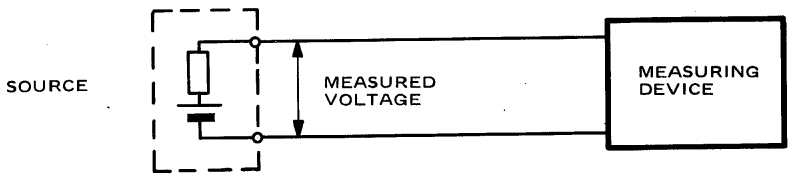


Fig. 4.1 *Current taken by a measuring instrument can cause a voltage drop across source resistance.*

A good moving coil meter will take a current of typically 10μA (100kΩ/V) so that with a source resistance of 1kΩ the voltage drop would be 10mV. This is obviously unacceptable for precision work since an instrument with such a low input resistance would read 1.49V instead of 1.50V.

Fortunately, electronic feedback techniques can give a digital voltmeter such a high input resistance that, for most practical purposes, the effect can be ignored. Thus the 7075 when measuring dc voltages less than 14V, has an input resistance in excess of 10GΩ. This means that the source resistance has to exceed 10kΩ before an error of 1 part per million is produced. If this sounds somewhat vague, it should be understood that defining the input resistance more closely is impossible since a group of voltmeters will have differing gains in their input amplifier. This will of course have no effect on their accuracy, but will make the input resistance different - possibly 20GΩ to 50GΩ, but never as low as 10GΩ.

When measuring voltages greater than 14V it is not possible to apply the unknown input directly to the input amplifier; first it must be attenuated. The attenuator must be very accurate and stable, capable of withstanding high input voltages, hence precision wire wound resistors are used. Since the use of high value resistors would make the attenuator more difficult and expensive to produce, a 10MΩ network is used. Hence, for voltages greater than 14V the input resistance is 10MΩ ± 0.25%, errors arising from source resistance being calculable with reasonable accuracy. For example, a source resistance of 1kΩ will degrade the reading by 0.01%, which is expressed as 1 digit in 10 000.

INPUT CURRENT

All solid state devices have finite input currents and/or leakage currents. A voltmeter will therefore have a current flowing at the input terminals even with zero input signal. The effects of this current are additional to those of input resistance. (Fig. 4.2).

By careful design this current can be reduced such that its effects are almost negligible and in the 7075 it is less than 20pA at room temperature. The input current will flow into or out of the Hi terminal and must therefore, be regarded as lying between + 20pA and – 20pA.

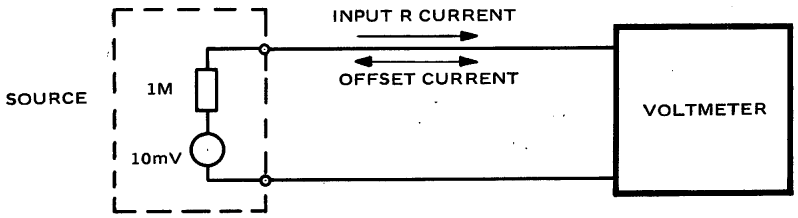


Fig. 4.2 *Current taken by input resistance flows into the voltmeter; offset current may flow either way. Both effects are present together.*

If we take an extreme example of a 10mV source having a resistance of 1MΩ, the input resistance (> 10GΩ) would give a reading that is up to 1μV in error. In addition an input current of 20pA will introduce an error of ± 20μV which will add to or subtract from the input resistance error. The total uncertainty then will be in the range + 19μV to – 21μV.

The condition given in the above example is unlikely to be encountered by the average user because low level signals nearly always have a relatively low source resistance, less than 10kΩ, the effects of which are insignificant.

ASSESSING INPUT RESISTANCE AND CURRENT

1. Input Current:-

Connect a 10MΩ resistor across the input terminals. Select 1s or 10s integration time and DC. (In a "noisy" environment it may be necessary to enclose the resistor in a screening box connected to the Lo terminal). The input current in pA is obtained by dividing the reading in μV by 10.

2. **Input Resistance:-**

Connect the voltmeter to a source of approximately 10V dc. via a 10MΩ resistor and a switch, mounted in a screening box as illustrated in Fig. 4.3.

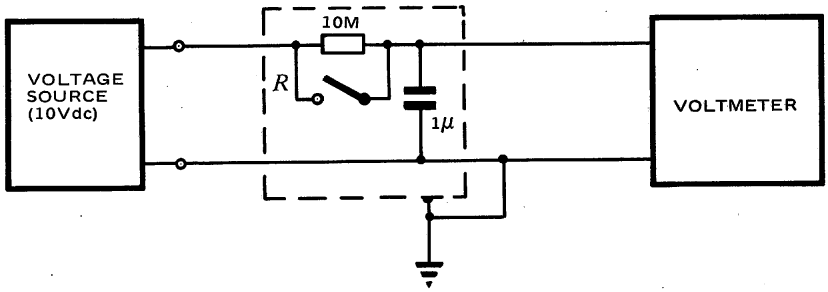


Fig. 4.3 *An assessment of input resistance will include an effect due to offset current.*

Select 1s or 10s integration time and DC.
With switch closed note the reading.
Open the switch and note the fall in reading (ΔV)

The fall is the algebraic sum of the voltage drop across R as a result of the source current and the instrument's input current, I_{in}. Thus:

$$\Delta V = \frac{R}{R_{in}} V_{in} + RI_{in} \qquad \text{(assuming } R_{in} \gg R\text{)}$$

then:
$$\Delta V - RI_{in} = \frac{R}{R_{in}} V_{in}$$

$$R_{in} = \frac{R\,V_{in}}{\Delta V - RI_{in}}$$

Substituting the experimental known values:

$$R_{in} = \frac{(10 \times 10^6) \times 10}{\Delta V - (10 \times 10^6) I_{in}} \ \Omega$$

For convenience this can be simplified and R_{in} expressed in GΩ (1GΩ = 10^9Ω), taking ΔV in μV and I_{in} in pA, thus:

$$R_{in} = \frac{10^5}{\Delta V - 10 I_{in}} \ \text{G}\Omega$$

It was previously noted that I_{in} may flow into or out of the dvm Hi terminal, assisting or opposing the source current. The magnitude of I_{in} is evaluated as in 1. above (Fig. 4.2); its direction and hence its effect on R_{in} can be readily established by reversing the source terminals in the circuit of Fig. 4.3 and again noting the reading with the switch open. A higher reading is obtained when I_{in} opposes the source current, in which case ΔV will be smaller and I_{in} in the final expression will have a negative value.

SPURIOUS VOLTAGES

Although small emf's occur in the voltmeter input circuit, they are compensated for by careful design. Thereafter, when the instrument has warmed-up for about 30 minutes, they are so stable as to be quite insignificant to the user.

The voltmeter will faithfully measure any input that is applied to its terminals; it is the responsibility of the user to ensure that the input contains only the voltage that he wishes to measure. In low level work - with perhaps a few tens of microvolts - this may require some care and thought in the arrangement of the circuit.

As an example, consider measuring the voltage produced by passing a very small current through a wirewound resistor. On the 100mV range the reading is recorded as 126μV. But the resistor is placed - in the sun or near a power transistor - so that one end is a little warmer than the other. Because of the dissimilar materials used in the wire of the resistor and the copper connections, a net thermal emf of possibly 40μV/^{o}C will exist. Thus a differential of 0.5^{o}C across the resistor could mean that the true result should be either 106μV or 146μV. The voltmeter cannot possibly distinguish between the wanted and unwanted parts of the signal that is applied to it. In this example, without altering the conditions of the resistor in any way, a measurement should be made with the small current flowing first in one direction and then in the other. In one case the thermal emf will add and in the other it will subtract. So the mean of the two results will eliminate the error

Metal oxide resistors and reed relays are two other examples in which thermal emf's bring about similar errors, in the reed relay the heat produced by the operating coil being the contributing factor.

When the unwanted emf can be determined and is steady, it can be 'backed-off' by using the μV OFFSET control. This has a range of $\pm$ 10μV. (typically)

In attempting precision measurement of low level signals, effects other than thermal emf's can cause problems. Leakage across an insulator which is degraded by humidity or an industrial atmosphere may produce an unsuspected voltage across a source resistance. Coaxial cables, when flexing under vibration, can generate quite high transient voltages due to the screen scrubbing the pvc insulant; the use of low noise cables will prevent this effect.

SERIES MODE INTERFERENCE

The examples of thermal and other, spurious emf's given above can be regarded as forms of interference because they interfere with the accurate assessment of the unknown signal. They are in series with the signal and voltmeter input and represent a special case of series mode interference because there is nothing that the voltmeter can do about rejecting dc interference while measuring a dc signal.

Series mode ac interference is a different matter. Because of the basic design principle, this voltmeter will ignore all the usual forms of ac and noise that may be intermingled with the dc signal. Hence in all normal measurement work the user will be unaware of ac interference and it will not cause errors.

Nevertheless, it would be possible to introduce such a degree of interference that the voltmeter would be unable to cope, so the keen user may be interested in the mechanism that brings about rejection.

The most common form of ac interference is simple 'hum - i.e. 50Hz superimposed on the dc signal. This can be visualised either as pick-up on the connecting leads, as shown in Fig. 4.4(a), or as a generator that is a part of the source, as in Fig. 4.4(b). In both the result is the same and is shown graphically in Fig. 4.5.

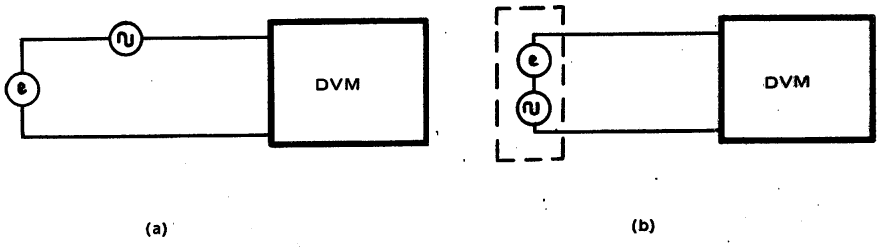


Fig. 4.4 *Interference at 50Hz can arise from pick-up on the leads (a), or may be inherent in the source (b).*

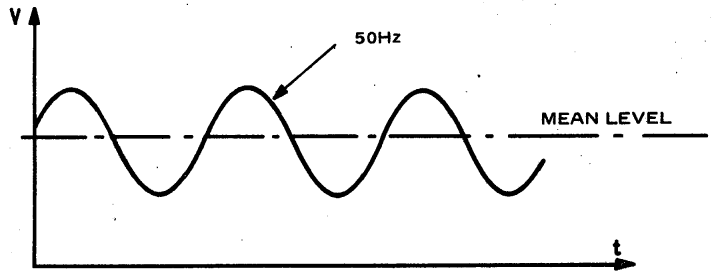


Fig. 4.5 *50Hz superimposed on the dc level that the voltmeter is trying to measure.*

Users of oscilloscopes will be familiar with this sort of picture and will know that the ac component is typically a few milli-volts peak-to-peak. This may be superimposed on a wanted dc signal of a mere 10μV.

The 7075 rejects ac signals by averaging the input voltage over the period of time selected, i.e. the integration time. Since the most common form of interference is attributable to the 50Hz (60Hz) mains, the integration times are chosen to be exact multiples of the mains period (20ms at 50Hz). This is achieved by timing the integration periods using a clock synchronised to the mains supply. Thus over the integration period the average 50Hz (60Hz) interference will be zero, the reading being unaffected.

This total rejection occurs at any frequency with a period equal to an exact fraction of the integration time. Harmonics of the mains frequency will also be totally rejected, while at other frequencies the rejection will be less.

Considering, as an example, the 1s integration time:-

1Hz, 2Hz, 3Hz, 4Hz, 5Hz..... 57Hz, 58Hz..... 83Hz, 84Hz..... 126Hz etc., being whole numbers of Hz their periods are exact fractions of 1s and hence total rejection will occur.

For the 10s integration time there will be 10 times as many totally rejected frequencies, starting at 0.1Hz and spaced 0.1Hz apart. The only practical limitation of frequency rejection is that imposed by clock accuracy and in the 7075 rejection of 50Hz (60Hz) is better than 70dB.

Series mode rejection is defined as:-

$$SMR = 20 \log_{10} \frac{\text{Peak reading error}}{\text{Peak of interference}} \text{ dB.}$$

N.B. The 1ms integration time has of course no rejection at 50Hz.

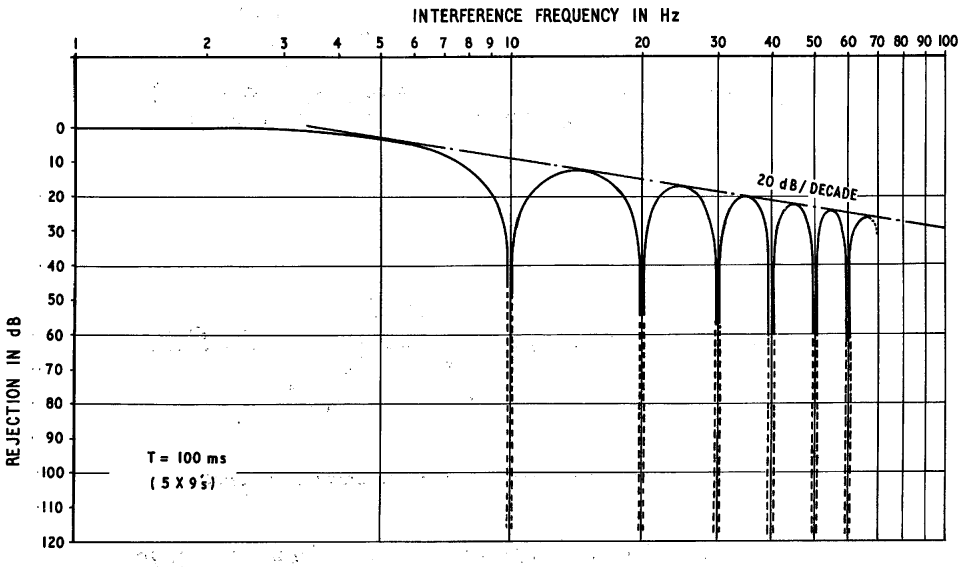


Fig. 4.6 *SERIES MODE REJECTION: These curves show the rejection at the frequencies given whilst measuring dc. The integration time is locked to the mains period so the curves will shift along the frequency axis as the mains supply frequency alters.*

COMMON MODE INTERFERENCE

Interference can also arise from unwanted voltages which are common to both input leads. This is illustrated in Fig. 4.7, where the signal source is earthed locally and the voltmeter input has also been earthed.

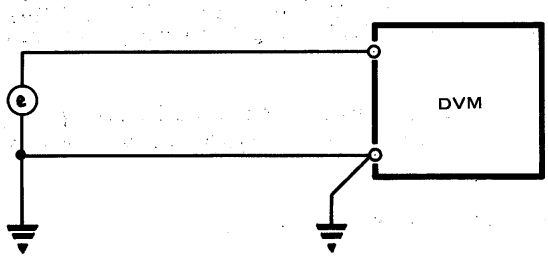


Fig. 4.7 *An 'earth' at both source and voltmeter input may introduce common mode interference. For this reason the voltmeter input is fully isolated.*

There is a distinct possibility that the two 'earths' are not at a common zero potential; in large industrial plants and in some multi-terminal system applications, widely separated earths can have potential differences between them in excess of 10V.

This situation can be represented as in Fig. 4.8, where the source is shown to be at a finite potential with respect to earth.

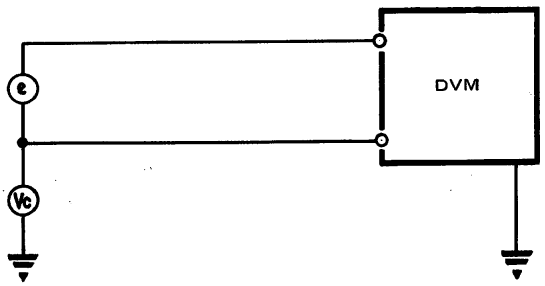


Fig. 4.8 *The source can be at a high potential above earth without causing errors.*

This would happen in practice, for example, where a thermocouple is used to measure the temperature of a furnace element. The signal emf might be millivolts of dc while the element itself is at 240V ac with respect to earth. Obviously earthing the voltmeter input would not be possible, although the case and many of the instrument's circuits are earthed via the mains lead.

The 7075 has been engineered so that the input circuits are extremely well isolated from the case, which itself is connected to mains earth. In all normal measurement the small current which does flow as a result of a large common mode voltage, will not cause any error. However, purely for the safety of equipment and operator, this voltage should not exceed 500V.

The lead supplied with the dvm is shown in Fig. 4.9. Within the instrument the cable screen is connected to the guard "box" (a screening compartment which encloses the input circuits) and at the free end the screen is strapped to signal Lo (Black). Hence the guard is preserved right up to the signal source and measurements cannot be affected by common mode current flowing in the screen and via leakage to earth.

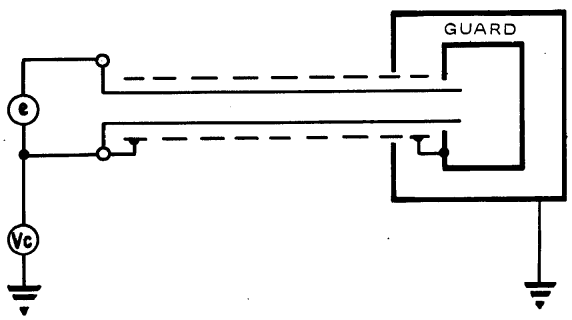


Fig. 4.9 *In the lead provided with the voltmeter Guard is strapped to Lo (BLACK) within the free end of the cable.*

In some measurement situations common mode voltage can have an affect on the reading. Most users will never meet the problem, but those who do can still eliminate errors by using the voltmeter correctly. When there is resistance associated with the source - perhaps inherent in the source, or in the connecting leads - common mode current can flow through this resistance. Examples are: the resistance of strain gauges, long compensating leads from a thermocouple. This is illustrated by Fig. 4.10 where it will be seen that current flowing from V_c to earth through the screen will pass through the resistance. If the guard-earth leakage is assumed to be the specified minimum of $10^{10}\Omega$ and V_c = 100V dc the common mode current will be 10^{-8}A. Taking a lead resistance of 1kΩ, 10^{-8}A will develop a voltage drop of 10μV. Since the voltmeter cannot reject dc interference the worst error will be 10μV.

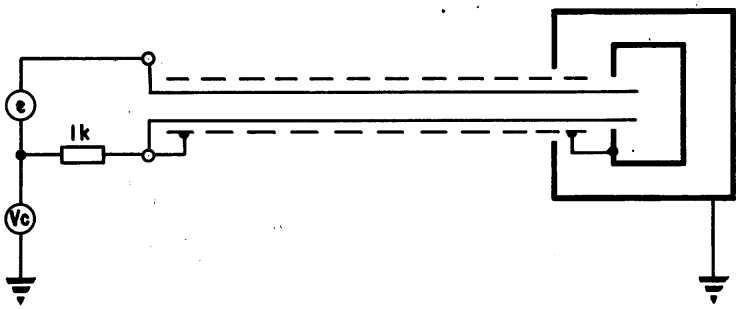


Fig. 4.10 *A rare, but more difficult, situation is where common mode current flows through lead resistance. This is entirely overcome by the arrangement of Fig. 4.11.*

If the source of common mode is ac, the stray capacitance from guard to earth is more important. The figure specified is 500pF which exhibits a reactance of about 6MΩ at 50Hz. With V_c now 100V rms the drop across 1kΩ is approximately 17mV rms or 24mV peak. This appears at the input terminals and the inherent rejection of series mode will be effective in reducing reading error to much less than 24mV. At worst the final reading error will not exceed 1μV.

In these examples a 1kΩ resistance has been assumed in one lead. Obviously the magnitude of the errors is proportional to this resistance and it is accepted practice to specify common mode rejection with 1kΩ unbalance in the leads using the configuration of Fig. 4.10. Even in these exceptionally adverse circumstances the error can be overcome by using a different input arrangement as in Fig. 4.11.

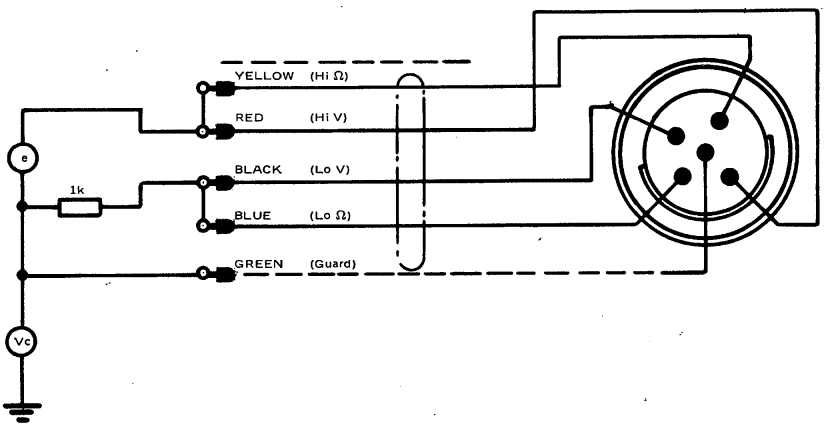


Fig. 4.11 *A special lead (EX 3183) is obtainable from Solartron which enables the Guard to be driven directly by the common mode voltage.*

Here use has been made of a special 5 way lead from which 4 cores and the screen are brought out at separate terminations.

The four cores are required for 4-terminal resistance measurement as described later. For voltage measurement with guard, however, only 3-terminals are required - signal Hi, signal Lo and screen (guard). When measuring voltage the YELLOW and BLUE cores are internally linked to RED and BLACK by the selection circuits. To prevent inadvertent contact of these plugs with earth, other terminals or each other, the user should plug YELLOW into RED and BLUE into BLACK. GREEN is connected directly to the source of interference thus isolating common mode current from the input leads.

Using this arrangement, even though the interference were the permitted maximum (500V dc or peak ac), it is most unlikely that there would be any discernable error - even on the most sensitive range.

For a more complete treatment of interference in digital voltmeter measurement the reader is referred to the following monographs:-

(1) Digital Voltmeters and Interference.

(2) Principles of Interference Rejection.

both of which are available free on request to Solartron.

NOISE

The foregoing explanation of interference dealt specifically with 50Hz because by far the most common source of interference is the mains supply or fields radiating from mains wiring and mains energised equipment. It has been shown in earlier pages of this Section that, at harmonics of 50Hz, rejection is improved so that 100Hz ripple from power supplies or 400Hz/1600Hz aircraft and ship supplies are unlikely to cause difficulty. When considering noise of no specific frequency (e.g. white noise) the integration process still applies and the resultant noise component over the integration period will tend to zero.

INTEGRATION TIME

When considering immunity to series mode interference, reference was made to the integration time. This time, which is capable of selection by the user, is the period over which the instrument takes an *average* measurement of the input level. The conversion technique continuously integrates (i.e. averages) the input signal, results being obtained which in principle, increase the accuracy of the conversion in direct proportion to the integration time. Averages over periods greater than 10s may be achieved in practice by recording successive 10s measurements and calculating the average over the time required. The result would be a true average of the input signal. For example an input of 10.00001V measured with an integration time of 100ms (full scale 14.0000) will be displayed as 10.0000 with the least significant digit changing to a 1 once every ten readings. This indicates that the true reading (the average over a large number of readings) is in fact 10.00001.

Integration time determines the resolution, maximum sensitivity, noise rejection and, of course, the number of readings presented per second.

The maximum displayed sensitivity is limited to 1μV but achieved in the instrument and present in the Interface output data is a sensitivity to 10nV.

All integration times are available in DC AC and Ω but the display on AC is limited to 5 × 9's (full scale 140000). This is discussed more fully in the following paragraphs.

AC MEASUREMENT

In its simplest form a dvm is able to measure dc voltage only. It can be adapted to measure ac by including an ac - dc converter before the dc input circuits. This is the case in the 7075, which employs a sophisticated circuit which converts the input into a dc proportional to its true rms value. This is an obvious advantage over previous, mean sensing, instruments, since alternating voltages are conventionally specified by rms value. In order to appreciate the difference between rms and mean, the reader is reminded of the precise relationship between the three ways of specifying the magnitude of a sinusoidal waveform:-

$$\text{Mean} = \frac{2}{\pi} \text{ peak} \qquad \text{i.e. } 0.637\ V_p$$

RMS (i.e. the *root* of the *mean* of the *square* of the input).

$$= \frac{1}{\sqrt{2}} \text{ peak} \qquad \text{i.e. } 0.707\ V_p$$

Two other relationships are important when evaluating alternating quantities. They are *form factor* and *crest factor*, derived as follows:-

$$\text{Form factor} = \frac{\text{rms}}{\text{mean}} = 1.1 \quad \text{for a sine wave.}$$

$$\text{Crest factor} = \frac{\text{Peak}}{\text{rms}} = 1.414 \text{ for a sine wave.}$$

Maximum crest factor for the 7075 is specified as 5:1.

COMPUTING TECHNIQUE FOR DERIVING RMS

A circuit for deriving true rms value of an alternating quantity is, in its simplest form, a circuit which:

a. squares the input V^2

b. obtains a mean $\overline{V^2}$

c. takes the square root $\sqrt{\overline{V^2}}$

That used in the 7075 is one of many configurations based on the simplified illustration in Fig. 4.12.. It has the advantage of being, to a large extent, unaffected by waveform shape.

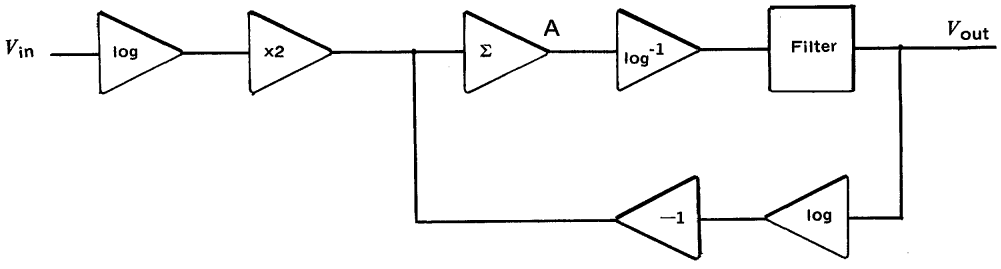


Fig. 4.12 *Typical computing technique for deriving true rms value.*

Expressed mathematically, the output of the summation amplifier, Point A, is

$$2 \log V_{in} - \log V_{out}$$

while the circuit output, V_{out}, is:

$$V_{out} = \overline{\text{Antilog}\,(2 \log V_{in} - \log V_{out})}$$

$$\therefore \quad V_{out} = \overline{\frac{V_{in}^2}{V_{out}}}$$

$$\therefore \quad V_{out}^2 = \overline{V_{in}^2}$$

$$\therefore \quad V_{out} = \sqrt{\overline{V_{in}^2}}$$

It has been said that with a circuit of this type the possibility of errors due to waveform distortion are virtually eliminated. However, when the 7075 is used on pulse waveforms, care may be necessary to ensure that it is operating within the specified limits. An approximate Crest Factor value for a pulsed waveform can be calculated from the formula:

$$\text{C.F.} = \sqrt{\text{Mark/space ratio}}$$

Elsewhere in this Section it was noted that when measuring dc voltages the dvm cannot reject thermal or other dc interference. Similarly there cannot possibly be rejection of series mode ac interference when measuring ac voltages. Common mode rejection is, however, still preserved and the input circuits on ac are still fully isolated from the instrument case and from earth.

For those who are interested in pursuing the subject in greater depth, a monograph 'AC Voltage Measurement', with particular reference to waveform errors, is available free on request to Solartron.

INTEGRATION TIME

In an earlier note reference was made to the limitation of scale length imposed on the ac mode of measurement. All integration times are available on AC but selection of the two longer periods is not accompanied by the increased resolution obtained in dc measurement. Selection of 1s or 10s integration time introduces Digital Filtering, enabling more stable, less noisy readings to be achieved with low frequency ac inputs. It is recommended that, in a noisy environment, users wishing to measure low frequency ac voltages make use of the significant advantages to be gained, by selecting one of the two longer integration times.

RESISTANCE

The 7075 measures the value of a resistor by passing a defined current through it and measuring the resulting potential difference. The current is small so that the power dissipated in the resistor is negligible.

Resistance Value measured	Current used
$< 14k\Omega$	1mA
$> 14k\Omega < 1.4M\Omega$	$10\mu A$
$> 1.4M\Omega \leqslant 14M\Omega$	$1\mu A$

The $1m\Omega$ sensitivity is satisfactory for most low value measurements. Should there be a requirement for increased sensitivity on low values the voltmeter can be used on a dc voltage range to measure the potential difference across the resistor with the current provided from an external source (Fig. 4.13).

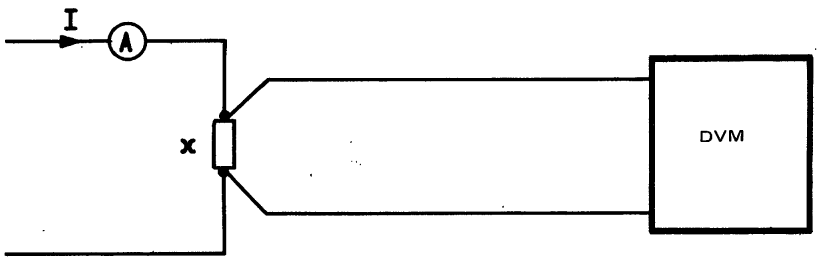


Fig. 4.13 *A very low value resistance may be measured by measuring the voltage developed across it. The voltage leads should be connected close to the ends of the resistor.*

If I is 10mA, a reading of 0.101245V means that X is 10.1245Ω. Obviously other appropriate currents could be used. The first point to observe is that, in this example, the sensitivity is $0.1m\Omega$ per digit. Hence the voltmeter connections must be made right at the ends of the resistor and must not embrace any significant length of the current carrying leads (1cm of 22swg copper wire is approximately $0.4m\Omega$).

A second point is that the accuracy is affected directly by the precision of the current setting. There would be little point in using a moving coil multimeter to set the current and then record a reading of 12.631Ω.

An improved technique is shown in Fig. 4.14.

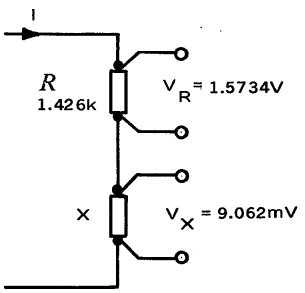


Fig. 4.14 *A ratio measurement avoids having to set a precise value of current.*

Here a resistor R, whose value is known, is connected in series with the low value unknown X. R can be a much higher value than X. If R is not already known it can be measured on one of the ohms ranges.

The voltmeter is connected across R and the current supply adjusted to give a reading. The precise value of V_R is not important; neither is the value of the current I. In this example I could be simply provided by a 1.5V cell. The reading V_R is recorded. The voltmeter is transferred to X and the reading V_X is noted. The value of X is then given by:-

$$X = R \frac{V_x}{V_R} \text{ ohms}$$

Using the values shown in Fig. 4.14:-

$$= \frac{1.426 \times 10^3 \times 9.062 \times 10^{-3}}{1.5734} = 8.213\Omega$$

If X is being set to different values it may be necessary to measure V_R each time because, unless I comes from a constant current supply, changes of X may significantly alter I.

Should it be necessary to measure resistance at a distance from the voltmeter which is beyond the reach of the standard lead, a special lead may be obtained from Solartron. In this the four cores and screen are terminated separately as shown in Fig. 4.15.

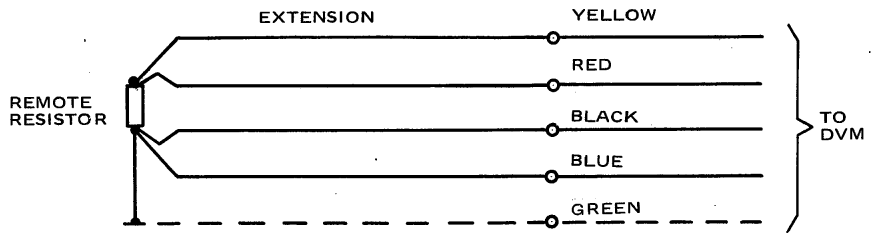


Fig. 4.15 *In measuring a remote resistor, lead compensation can be preserved by using the special input cable (obtainable from Solartron) and extending it by a 4 core screened cable.*

This cable should be extended to reach the point of measurement by means of a similar 4 core screened cable and connected to the remote resistor as shown.

This arrangement will preserve the compensation for lead resistance up to a maximum of 1Ω per wire, on any ohms range. Using an extension of 7/.0076 wires a length of 100m can be safely used. (The Yellow and Red leads may have resistances as high as 1kΩ).

The user is reminded that, should separate extension wires be used for this purpose, the connector run should be identical for each lead - preferably by employing twisted pairs. In this way the effects of interference emf's, induced in the leads as a result of local electromagnetic fields, will be minimised.

RATIO MEASUREMENT

Ratio is a relationship, of one quantity relative to another. When considering ratio measurement one intends that measurement is to be made relative to a reference source. It is essential, therefore, when making precision ratio measurements with the 7075, that the integrity of the reference matches the stability and accuracy of the dvm. If that cannot be guaranteed, it is suggested that reference and signal inputs are derived from the same voltage source. Thus any variation in the source, providing it is within both input limits, will not affect the readings.

DC/DC RATIO

Example 1. Comparing the performance of one device against another, standard, device.

Two transducers, A and B are in the same environmental enclosure and fed from a common power source, to ensure that variations in the supply and of temperature, vibration etc., affect both devices equally (Fig. 4.16).

The output of A, the standard, is taken to the dvm reference terminals while that of B - the transducer under test - is taken to the dvm signal input.

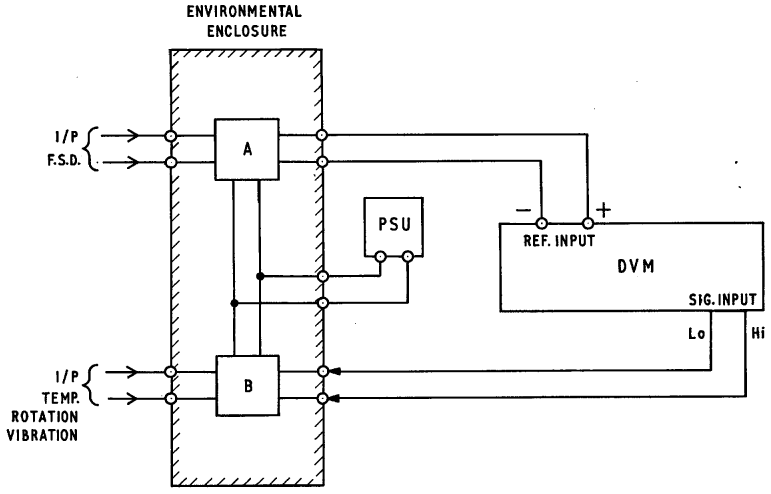


Fig. 4.16.

As was stated in Section 3 of this manual, the relationship between the dvm reading (V_{out}) and its input (V_{in}) when RATIO is selected is:-

$$V_{out} = \frac{10V_{in}}{V_{ref}}$$

Thus the ratio $V_{in} : V_{ref} = \frac{\text{displayed reading}}{10}$

which in the example is the ration of the output of transducer B to that of A. Thus a true comparison can be made.

Example 2. Determining the actual value of a number of 0.1Ω precision resistors, given a standard resistor of known value 10.0002Ω (± 0.005%) rated at 1A.

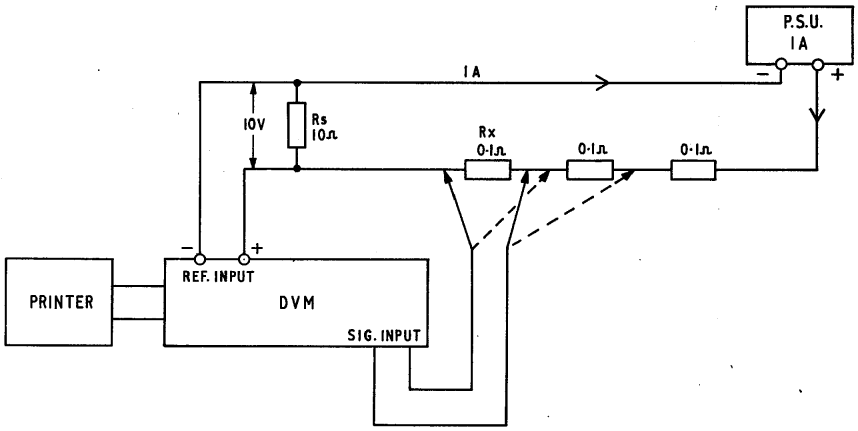


Fig. 4.17.

The constant current psu delivers 10V nominal at 1A. With the dvm operating on the 100mV range:

$$\frac{R_x}{R_s} = \text{Ratio} = \frac{\text{displayed reading}}{10 \times 10^3}$$

$$R_x = \frac{\text{displayed reading}}{10^4} \times R_s$$

If the dvm reading is 100.050mV

$$\text{then } R_x = \frac{100.050}{10^4} \times 10.0002$$

$$= 0.100053\Omega$$

Note that the resolution of the result is 1μΩ and the total uncertainty is the sum of the limits of error of the dvm on the selected range and the tolerance of the standard resistor.

This technique should be compared with that shown in Fig. 4.14 and the two important differences noted:

(i) the actual voltage across R_s does not have to be measured

(ii) provided V_{ref} does not fall below 10V (for minimum uncertainty) the source current need not be stable.

CONCLUSION

Use of the Ratio facility is not intended to, nor does it, give more accurate measurements than those possible using the instrument's internal reference. It does, however, simplify many otherwise time consuming measurement tasks. The reader will no doubt discover many more applications than the examples given.

Rear Panel showing Interface Unit 70754.

SECTION 5 Parallel BCD Interface Unit 70754

SYSTEMS USE

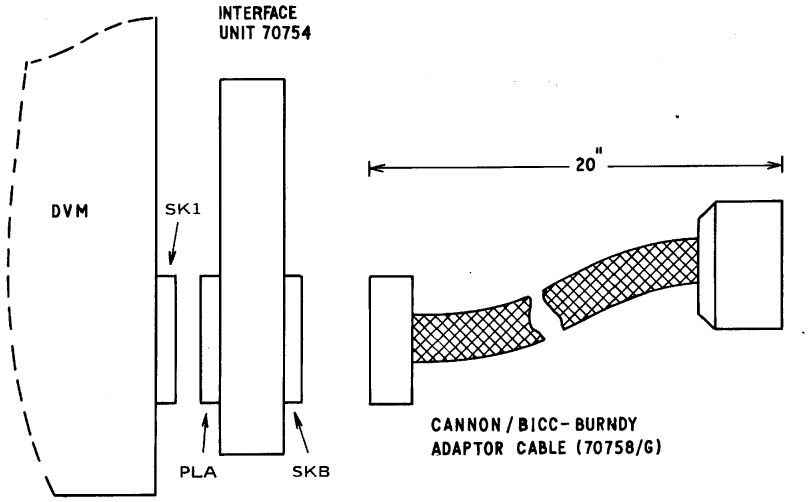
The addition of a Parallel BCD Interface Unit (70754) permits the use of the dvm in a data logging or automatic test system. Full remote control of the front panel controls (except POWER) is possible and the interface provides display information and the various control signals necessary in such systems.

The interface can be considered as a two-part unit. One section enables the external system to command all measurement decisions, obviating the need for manual selection. The other section, primarily concerned with the output of measurement data, also generates gating and steering signals to control the use of the data within the external system.

CONNECTION

The Parallel BCD Interface Unit mates directly with the dvm rear Cannon socket, being secured by two captive screws (see illustrations on facing page). In the ensuing notes all pin designations refer to the Interface Unit **SKB**. For those users with systems based on the Solartron Master Series of instruments, a Cannon/BICC Burndy adaptor cable (70758G) is available as an optional accessory. Connection details for **SKB** and for the adaptor cable, are given in the table at the end of this Section.

Note: If a Parallel BCD Interface Unit is fitted but not connected to an external system, front panel selection of REMOTE will cause the instrument to revert to 10s integration, dc volts operation (100ms if 70758G is fitted).



LOGIC LEVELS

All signals unless otherwise stated conform to the following logic levels:

Input:

High	(Logic '1')	= + 2.4V < '1' < + 5V at 100μA
Lo	(Logic '0')	= −0.5V < '0' < + 0.5V at 5mA 'sink'

Output:

High	(Logic 1)	+ 2.4V < '1' < + 6V from 6kΩ source
Low	(Logic 0)	−0.5V < '0' < + 0.5V at 10mA sink.

INPUT INFORMATION

The following input commands can be accepted from the external system. Command signals enter the instrument via the 50 way rear panel connector while either front or rear input socket may be used for the measurement leads.

CONTROL

External commands are effective only when the instrument is in REMOTE operation, either as a result of selection of the REMOTE push button or on receipt of FRONT PANEL LOCKOUT command from the external system - the latter overriding any selection made with the push-button. FRONT PANEL LOCKOUT is effected as follows:-

Pin 38	FRONT PANEL LOCKOUT
0	Yes
1	No

When FRONT PANEL LOCKOUT is commanded all front panel controls (except POWER) are disabled.

FUNCTION

The measurement mode is commanded on pins 42, 43 as follows:-

Pin 43	Pin 42	FUNCTION
1	1	DC
1	0	AC (RMS)
0	1	Ω
0	0	CHECK

RATIO OPERATION

Ratio measurement in DC or AC (RMS) mode (not available on Ω) is programmed on pin 41. (An external reference must be applied to the rear input terminals as normal).

Pin 41	RATIO COMMANDED
0	Yes
1	No

INTEGRATION TIME

The pins employed for Command Integration Time are 44, 45 and 46, selection being made with a 1 2 4 BCD code as follows:

(4) Pin 44	(2) Pin 45	(1) Pin 46	COMMANDED INTEGRATION TIME
0	1	1	1ms (3 x 9's)
1	0	0	20ms (4 x 9's)
1	0	1	100ms (5 x 9's)
1	1	0	1s (6 x 9's)
1	1	1	10s (7 x 9's)

Other codes will give 1ms integration time.

On AC (RMS) codes 110, 111 give the stated integration time but resolution remains at 5 x 9's as for code 101.

RANGING

Autorange can be inhibited by setting pin 47 High, while Command Range signals, in 1 2 4 BCD form, are applied to pins 48, 49 and 50 as shown in the table.

It should be noted that when operating on command range overload protection is as stated in the tables in Section 2, the instrument's ability to autorange out of trouble being inhibited.

INPUT RANGE COMMAND CODES

Pin 47	(4) Pin 50	(2) Pin 49	(1) Pin 48,	V DC	V AC	OHMS
1	0	0	0	1000V	1000V	10MΩ
1	0	0	1	100V	100V	1MΩ
1	0	1	0	10V	10V	100kΩ
1	0	1	1	1V	1V	10kΩ
1	1	0	0	100mV	100mV	1kΩ
1	1	0	1	10mV	100V	100Ω
1	1	1	0	AUTORANGE		10Ω
1	1	1	1	AUTORANGE		

If a Low is applied to pin 47, Autorange is enabled and Command Range signals will have no effect. A SAMPLE Command is, however, necessary to initiate an Autorange sequence.

SAMPLE

A measurement is initiated by one of two SAMPLE commands originating in the external system. These are:-

CONTACT SAMPLE	Contact closure between pins 39 and 37 (0V) with < 2ms contact bounce.
PULSE SAMPLE	A positive pulse applied to pin 40, of amplitude between +3V and +8V and duration $> 10\mu$s.

SAMPLE occuring during a measurement cycle will have no effect.

Note: If FRONT PANEL LOCKOUT command has not been received but the instrument is in Remote operation as a result of selection of the REMOTE push button, the SAMPLE push buttons are still effective. Selection of REP in this instance will inhibit any remote SAMPLE commands.

At the end of scan the channel lines are usually open circuit. Depending on the last operating range, either Commanded or Autorange, the display at this time may 'flash'. This is not necessarily an indication of instrument overload but merely warns the user that the displayed reading (i.e. the last digitised measurement) is no longer representative of the signal present at the input terminals. This should not cause any concern, the next SAMPLE Command automatically updating the display but the effect can be prevented by connecting a 10MΩ resistor across the input terminals. However if measurements of resistance or of voltages having a high source impedance are being made, the effect of this extra resistance must be taken into account.

OUTPUT INFORMATION

DISPLAY DATA

The numerical display data, 6½ decades in BCD form, is available for use at the 50 way output socket. For details of pin connections reference should be made to the throw-clear connection table at the end of this Section. Output data full scale is normally 1400000 but this can be reduced to 999999, if required, by means of a link in the Interface Unit. When operating on the shorter integration times unused decades are presented as zeroes.

POLARITY

The polarity of a reading is coded on pins 26 and 27 of the connector, with the following significance:-

Pin 26	Pin 27	Polarity
0	1	Negative (–)
1	0	Positive (+)
0	0	AC/Ω (Polarity not applicable)

RANGE

There are two possible types of Range Output codes, one of which is related to the range input code:

RANGE OUTPUT CODE

(4) Pin 30	(2) Pin 31	(1) Pin 32	V DC	V AC	OHMS
0	0	0	1000V	1000V	10MΩ
0	0	1	100V	100V	1MΩ
0	1	0	10V	10V	100kΩ
0	1	1	1V	1V	10kΩ
1	0	0	100mV	100mV	1kΩ
1	0	1	10mV	*	100Ω
1	1	0	*	*	10Ω
1	1	1	*	*	*

* Code not applicable

The other type is arranged such that the integer value of the displayed data (6½ decades) is related to the measurement as in the following, where N is the output code decimal value:-

Measurement = Reading (as an integer) x 10^{-n}V or kΩ.

The 6½ decade range output BCD is given in the following table:-

(4) Pin 30	(2) Pin 31	(1) Pin 32	Voltage Range	Resistance Range	N
0	1	0		10 000kΩ	2
0	1	1	1000V	1 000kΩ	3
1	0	0	100V	100kΩ	4
1	0	1	10V	10kΩ	5
1	1	0	1V	1kΩ	6
1	1	1	100mV	100Ω	7
0	0	0	10mV	10Ω	(8)

If a full scale of 5½ decades has been selected, the value of N can be reduced by 1, maintaining the above relationship, by means of a link in the Interface Unit.

This is illustrated in the modified (5½ decade) table:-

(4) Pin 30	(2) Pin 31	(1) Pin 32	Voltage Range	Resistance Range	N
0	0	1		10 000kΩ	1
0	1	0	1000V	1 000kΩ	2
0	1	1	100V	100kΩ	3
1	0	0	10V	10kΩ	4
1	0	1	1V	1kΩ	5
1	1	0	100mV	100Ω	6
1	1	1	10mV	10Ω	7

FUNCTION

The Output mode code is identical to that for Command mode, the relevant pins being 28 and 29.

Pin 28	Pin 29	FUNCTION
1	1	DC
0	1	AC (RMS)
1	0	Ω
0	0	CHECK

PRINT COMMAND PULSE (Pin 33)

At the end of a measurement pin 33 goes High for between 10 and 30μs, providing an alternative PRINT command for those systems requiring a pulse input.

Both PRINT command pins are held at logic level '0' when REP is selected.

PRINT COMMAND LEVEL (Pin 34)

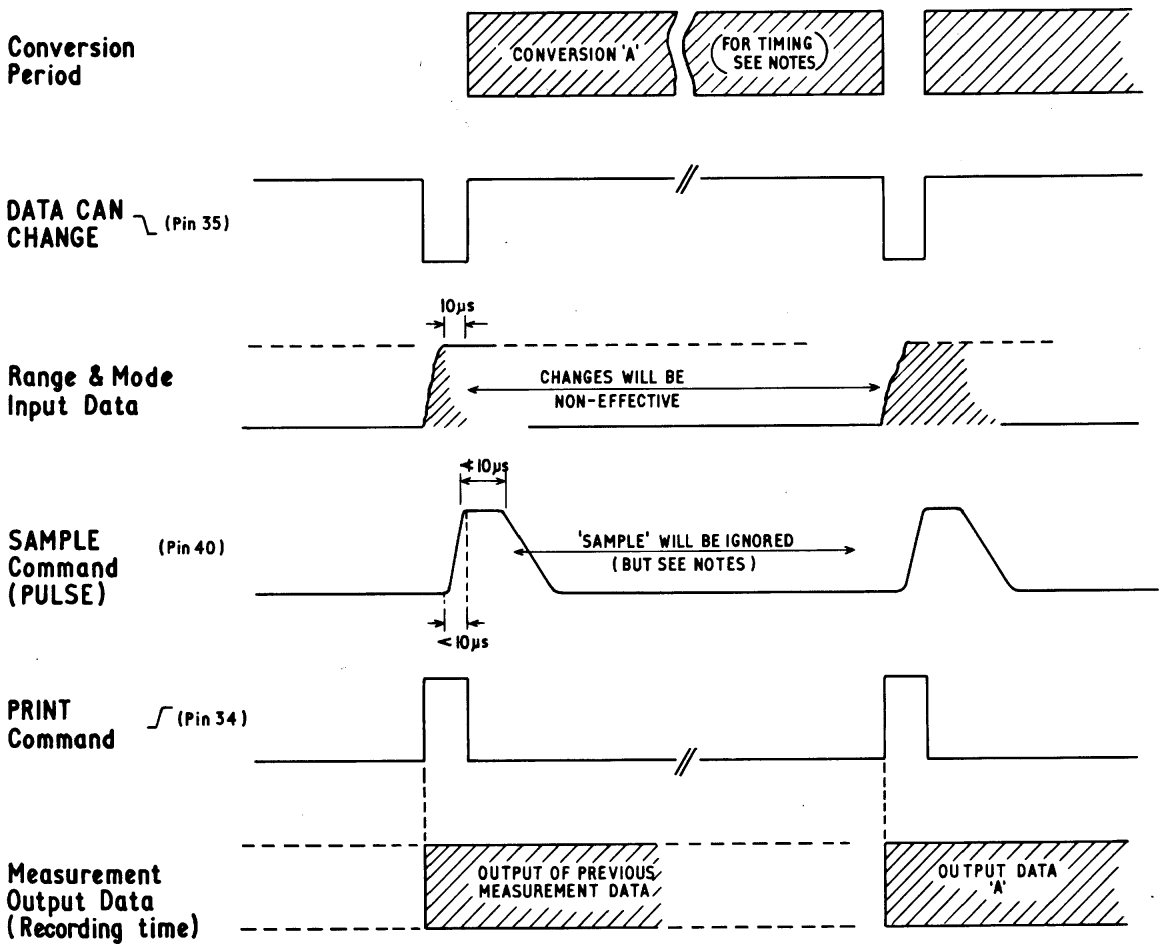
During a measurement pin 34 is Low, having been set to '0' after SAMPLE command. After the measurement is complete and the output information is updated pin 34 is set High as PRINT command to the external system.

The logic inverse on pin 35 is used as DATA CAN CHANGE, a logic '0' informing the external system that a change in command data can be accepted.

NOTE: No separate DATA IS CHANGED input command is required, comparison being carried out by circuits within the voltmeter.

Timing Information

Analogue and digital information can be applied simultaneously with SAMPLE command, all necessary settling delays being provided automatically by the instrument.



CONVERSION TIMING

1. Basic delay = Integration time + 4ms (DC, Ω)
   + 800ms (AC)

2. Mode change* = 20ms

3. Range change* = 21ms range-up (or down) per range (3 × 9's DC, Ω)

   21ms range-up
   40ms range-down
   } per range (4 × 9's to 7 × 9's; DC, Ω)

   = 800ms per range (AC)

*These delays are additive if on Autorange operation, parallel if operating on Commanded range.

NOTES

1. To avoid the slowing down effect of range hunting when Autorange is remotely commanded, receipt of a SAMPLE Command is necessary for autorange to occur. When in LOCAL operation however, detection of an overload causes an immediate Autorange upwards, independent of the receipt of SAMPLE Command.
2. Should a SAMPLE Command occur during a self-protecting autorange sequence it will be stored, to be obeyed once the overload condition no longer exists. With the foregoing exception SAMPLE Command occuring at any time other than after a PRINT Command output, will be ignored.

CONNECTION TABLE 1.

SKB Pin No.	FUNCTION	
1	1×10^6	Staticised BCD output data
2	8×10^5	
3	4×10^5	
4	2×10^5	
5	1×10^5	
6	8×10^4	
7	4×10^4	
8	2×10^4	
9	1×10^4	
10	8×10^3	
11	4×10^3	
12	2×10^3	
13	1×10^3	
14	8×10^2	
15	4×10^2	
16	2×10^2	
17	1×10^2	
18	8×10^1	
19	4×10^1	
20	2×10^1	
21	1×10^1	
22	8×10^0	Not available when using Adaptor Cable.
23	4×10^0	
24	2×10^0	
25	1×10^0	

SKB Pin No.	FUNCTION
26	+ ve POLARITY
27	− ve Output code
28	FUNCTION output code 0 for A.C. } Both 0 for CHECK
29	0 for Ω } Both 0 for CHECK
30	(4) RANGE Output
31	(2) RANGE Output
32	(1) RANGE Output
33	PULSE PRINT Command
34	LEVEL (Output signal)
35	DATA CAN CHANGE Output
36	OVERLOAD (Output signal)
37	EARTH/Logic '0' level
38	FRONT PANEL LOCKOUT
39	SAMPLE Command - CONTACT
40	SAMPLE Command - Pulse
41	RATIO Command
42	FUNCTION Command 0 for AC } Both 0 for CHECK
43	(DC, AC (RMS or Ω) 0 for Ω } Both 0 for CHECK
44	(4) INTEGRATION TIME Command
45	(2) INTEGRATION TIME Command
46	(1) INTEGRATION TIME Command
47	AUTORANGE Command
48	(1) RANGE Command
49	(2) RANGE Command
50	(4) RANGE Command

Systems Interface 50-way Cannon Socket Connections.

CONNECTION TABLE 2.

BICC - BURNDY Pin designation	CANNON (SK.B) Pin Number
A	21
B	20
C	19
D	18
E	17
F	16
H	15
J	14
K	13
L	12
M	11
N	10
P	9
R	8
S	7
T	6
U	5
V	4
W	3
X	2
Y	1
Z, a, b	(Note 1.)
c	41

BICC - BURNDY Pin designation	CANNON (SK.B) Pin Number
d	26
e	27
f	32
h	31
j	30
k	– (Note 2)
m	48
n	49
p	50
r	38
s	39
t	40
u	33
v	34
w	– (Note 2)
x	35
y	47
z	– (Note 2)
AA	42
BB	43
CC, DD	28, 29 (Note 4)
EE	46
FF	44
HH	45 (Note 3)

Notes:

1. Pins Z, a, b are connected to Earth at Pin HH.
2. Pins k, w, z are not used.
3. Pin HH is connected to Earth holding Cannon pin 45 Low.
4. The outputs on CC and DD are the complement of Master Series DVM outputs.

Bicc - Burndy Extension Connector Pin Connections. (70758G)

(Master Series Compatible).

Servicing

INTRODUCTION

Sections 6-8 contain Technical Information and are written primarily to meet the needs of the Service engineer. A detailed treatment of the principles of operation is not included but the descriptive text accompanying each circuit diagram is sufficient to enable the reader to understand the purpose of the circuit and its effect on its input(s). To facilitate fault diagnosis attention is drawn to special features of circuits, together with any precautions necessary when carrying out checks.

PRESENTATION OF INFORMATION

The circuit diagrams (Section 6) are arranged to fold out clear to the right, the functional description appearing on the facing left hand page. Similarly the pcb layout and notation diagrams will fold out clear to the left, where possible arranged to immediately precede the relevant text. Hence immediate cross reference can be made between the circuit and the component layout diagram.

Signal paths are indicated by bold lines, arrows being used where necessary to indicate the direction of functional flow. In general this is from left to right, feedback paths flowing from right to left. To prevent ambiguity however and where space is limited, this convention has not been followed rigidly.

COMPONENT IDENTIFICATION

In addition to the pcb layout diagrams, line drawings and/or clear photographs are reproduced in the manual to facilitate rapid identification of components during diagnostic checks.

The component numbers on each diagram are particular to that pcb only – thus each board will have, for example, an R1. Identification is by reference to the Parts List in Section 7.

On two major circuit boards the component numbering has been coded, a prefix digit being used to differentiate between components of the several functions carried on those boards. Thus R201 indicates R1 in the circuit coded '2'.
(This is explained in greater detail in the circuit descriptions.)

POWER RAILS

These are represented by short, detached bars annotated to show the nominal voltage. Several separate bars, annotated with the same voltage, may appear on a diagram. These of course are electrically connected to a common rail derived from the Power Supply circuits.

Zero volts may be either Supply 0V or one of six separate Signal 0V lines. Signal 'earth' rails are annotated Sig 0V1 to Sig 0V6, these being commoned at a star point. They should not be joined at any time during servicing.

Note that voltages specified on the circuit diagrams are in all cases **nominal** values, the actual value being dependent upon the load offered to the supply by the specific circuit. Inconsistencies between actual measured values and those quoted should not, therefore, be regarded with suspicion without considering other symptoms of possible unserviceability.

ELECTRICAL CONNECTIONS

Scotchflex ribbon connectors are generally used for pcb interconnections, though in some instances Berg - type pins/sockets have been used where pcb's are mounted in the same vertical plane. The latter are marked 'B', followed by a number.

It is important to ensure correct mating of all inter-board connections after any servicing operation.

SPLIT PADS

These are used to provide a means of isolating various parts of the circuit for fault diagnosis and, in some instances, to permit alteration of circuit parameters for a particular operating need. They are simply bridged with solder, open circuit being effected by removing the solder. It should be noted that excessive heat applied during this operation could damage the solder track – a small, low wattage iron should be used.

TEST POINTS

A further aid to rapid circuit check-out is the provision of test pins. These are indicated on the circuit diagrams and clearly marked on the pcb's.

TEST KIT 70759C

To provide access to certain circuit areas when servicing the instrument 'live', extension connectors have been assembled into a kit which can be ordered as an Optional Accessory.

CAUTION Ohms Guard

Before commencing any Servicing the instrument should be inspected to determine whether an Ohms Guard modification has been embodied. Serious permanent damage can be caused by an inadvertent short circuit of the Ohms Guard line to earth/signal low.

FLOATING CIRCUITS

As much of the instrument's electronic circuitry is floating with respect to Supply Earth, it is recommended that an isolating transformer is used for all servicing work within this voltmeter.

PRINCIPLES OF OPERATION

The 7075 dvm employs an A/D converter which converts the input voltage to a time analogue, which in turn is split into discrete, equal-length time units. These are counted and the result displayed as a numerical indication of the measured quantity.

The V to t converter produces a pulse train, the pulse width being variable and proportional to the magnitude of the input signal. The pulses gate the output of a fixed frequency clock into a counter, over a time period which can be chosen by the user. At the end of the time period the total accumulated in the counter is a measure of the input during that time. An averaging (integrating) technique is used whereby the total count is divided by the number of gating-pulses used. The average thus obtained is displayed as a direct reading of the measured quantity.

Statistically, the larger the sample the truer will be the average. This reasoning has been applied in the 7075, in that the integration time (the measurement period) can be varied by the user. At a fast reading rate the measurement period is very short and the average obtained is correct to, say, 2 decimal places. Increasing the measurement period provides a much truer average – the resolution is increased to much smaller sub-divisions.

Since the total count is much larger when operating at the longer integration times, the counter requires more capacity. This results in an increase in scale length and it follows that the display sensitivity is improved hand-in-hand with the increased measurement resolution.

FUNCTIONAL DESCRIPTION

7075 can conveniently be regarded as consisting of four major functional sub-divisions. Reference to the Block Diagram opposite will identify those as:

1. the SIGNAL CONDITIONING section.

2. the A/D CONVERTER.

3. the DIGITAL section.

4. the POWER SUPPLY.

Considering the overall functioning of the instrument, an input is processed by the Signal Conditioning circuits which change all measured functions into a dc voltage, scaled to a level suitable for further processing. Input protection, reference and guard circuits are included in this sub-division.

The correctly scaled dc signal is converted to a train of digital pulses by the A/D Converter, these pulses being used to gate the output of a Clock circuit.

Control of the measurement conversion and timing of the control sequences are two important parts of the Digital section. It also contains the counters which accumulate the gated clock-pulses, the multiplexer and memory circuits and the display drivers. The decoded counter output ultimately provides drive currents to light the appropriate Display elements.

All necessary operating power for the analogue circuits and logic levels for the digital circuits are provided by the Power Supply. Also derived from this section of circuitry is the synchronising waveform for the mains-locked clock.

Regardless of what measurement is being made the Voltmeter is only capable of measuring dc volts, hence all other quantities require to be converted into a dc level. Once converted, the input signal is applied to an amplifier, the gain of which is determined by the range on which the instrument is operating. It is the output of this amplifier which is compared with the instrument's reference, both being applied to the A/D Converter.

A/D CONVERTER

The analogue input, changed to a dc voltage level and correctly scaled, is converted to digital form by a circuit which produces a pulse train, the width of the pulses being proportional to the magnitude of the input. This conversion technique is known as Voltage-to-time conversion – the method employed being a variant in which the "time" is in fact the difference between two distinct time periods. It is this time-differential which is used to control the number of clock pulses finally accumulated in an up/down counter in the Digital circuits.

DIGITAL SECTION

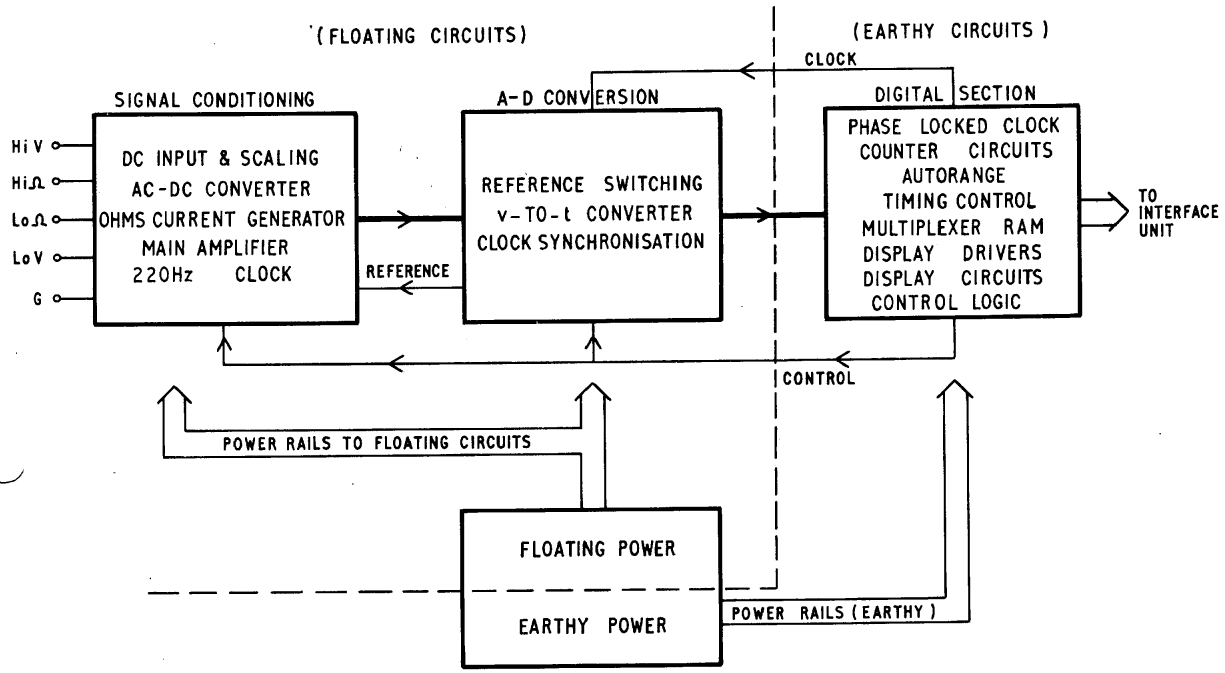
The heart of this section is the clock which produces the pulses which will be counted to digitally measure the applied signal. The clock pulses are gated into a counter stage by the V-to-t converter output pulse train. Two counters are used, the main one being concerned with the measurement function proper while a small, 3 × 9's counter gives a fast indication of range overload and initiates an autorange action. A further, timing counter determines the counting (or integrating) period.

The up/down (7 × 9's) counter output is multiplexed into the random-access memory (RAM) via a zero blanking circuit. Under the control of the sequence timing circuit the RAM is accessed, outputs being applied to the display interface to generate display drive signals.

POWER SUPPLY

The power supply consists of a switching regulator driving a 25kHz invertor to provide the main supply rails. Thus no mains transformer is used and voltage tappings are not required. A small transformer is included to provide the reference frequency for the mains locked clock.

It should be noted that parts of the power supply are floating with respect to supply earth. The use of an isolating transformer is essential when carrying out checks on the floating circuits.


(FLOATING CIRCUITS)
(EARTHY CIRCUITS)
CLOCK
SIGNAL CONDITIONING
A-D CONVERSION
DIGITAL SECTION
Hi V
Hi Ω
Lo Ω
Lo V
G
DC INPUT & SCALING
AC-DC CONVERTER
OHMS CURRENT GENERATOR
MAIN AMPLIFIER
220Hz CLOCK
REFERENCE
REFERENCE SWITCHING
v-TO-t CONVERTER
CLOCK SYNCHRONISATION
PHASE LOCKED CLOCK
COUNTER CIRCUITS
AUTORANGE
TIMING CONTROL
MULTIPLEXER RAM
DISPLAY DRIVERS
DISPLAY CIRCUITS
CONTROL LOGIC
TO INTERFACE UNIT
CONTROL
POWER RAILS TO FLOATING CIRCUITS
FLOATING POWER
EARTHY POWER
POWER RAILS (EARTHY)

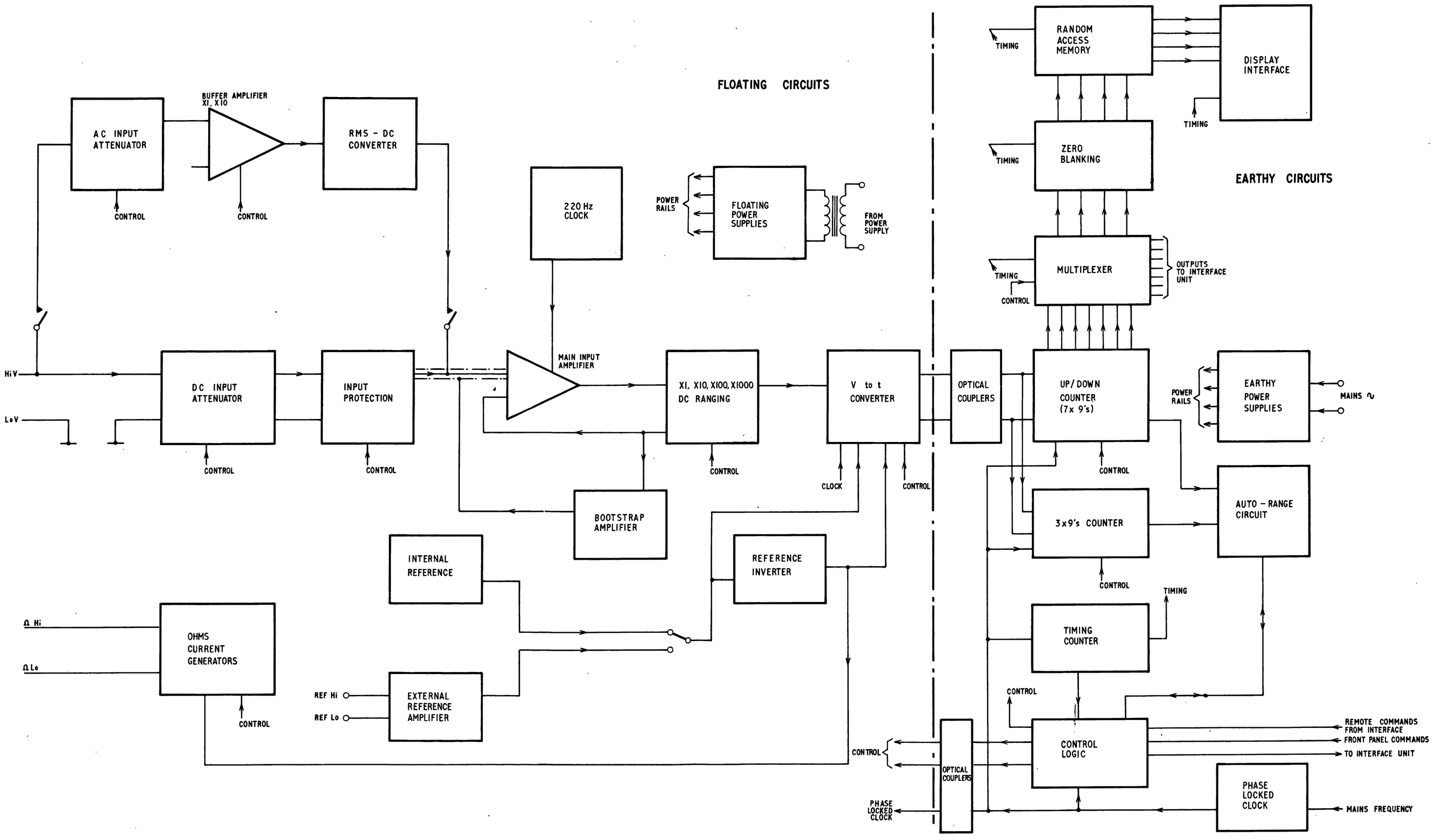
SECTION 7 Circuit Descriptions

This section provides the Servicing engineer with information concerning the function of the instrument's circuits, the treatment being one of defining the *effect* of each circuit on the input(s) applied to it. In the main the descriptions follow a signal path through the circuit board, diversions from the flow being examined as they become relevant to the signal. When considering the digital circuits, however, the descriptive text is concerned more with sequences and parallel logic activities. In these instances a flow treatment is inappropriate.

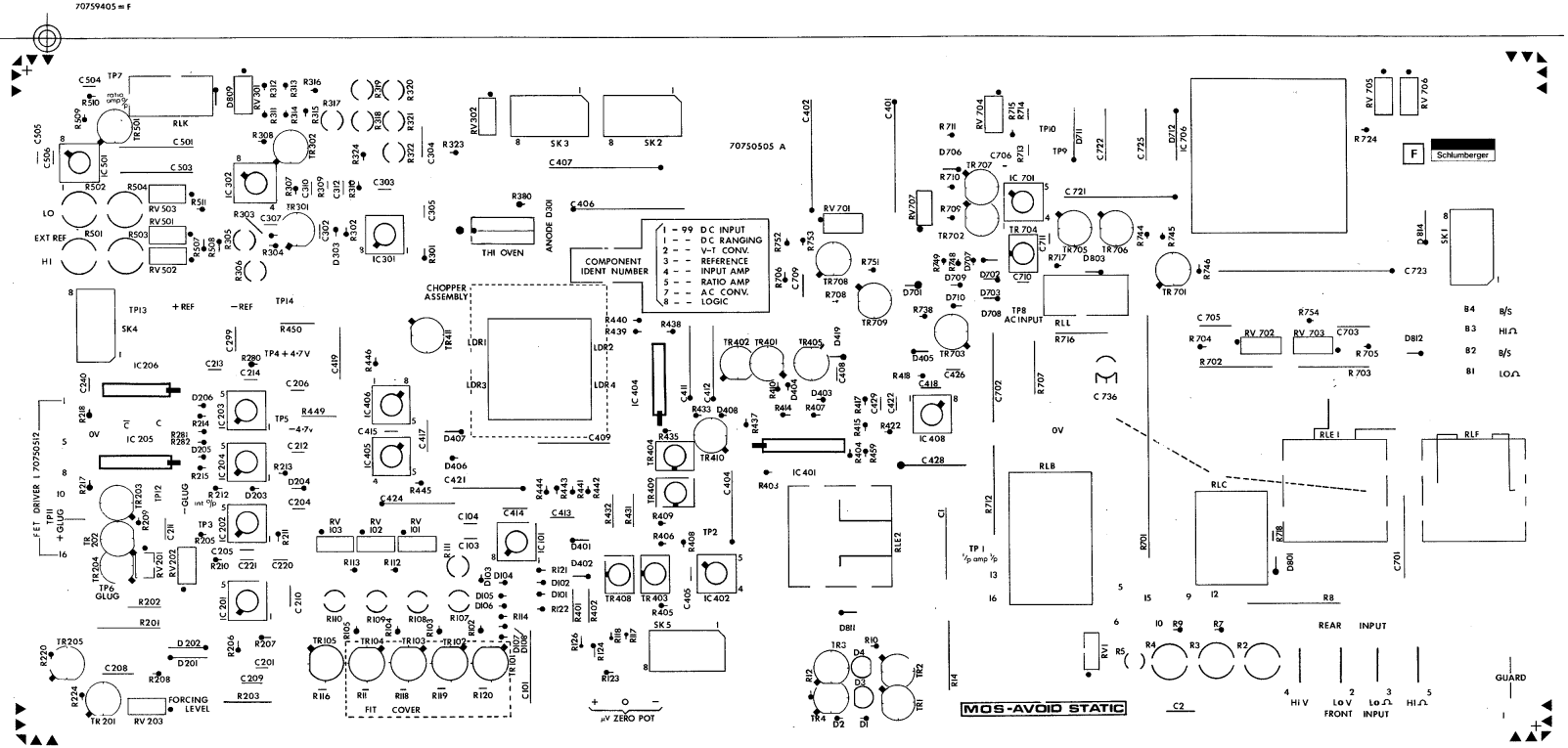
INTRODUCTION

The Block Schematic Diagram (Diag 7.1) illustrates the functional layout of the instrument. The diagram can be seen to be an expansion of that on page 6.5 and while it's primary function is that of affording an overall appreciation of the instrument, it also provides the reader with a pictorial index to the ensuing circuit descriptions

Block Schematic Diag. 7.1 ⟶



Block Schematic Diag. 7.1



THIS BOARD MUST BE SILK SCREENED
WITH YELLOW PAINT.

PCB 5 Notations

DC INPUT (Diag 7.2)

The purpose of these circuits is to provide initial conditioning of the input signal and to protect the Input Amplifier (Diag 7.3) against voltage overloads.

INPUT ATTENUATOR

The instrument can accept inputs up to 14V without attenuation, this circuit providing the necessary attenuation on the top two ranges. For inputs below 14V RLB is energised, relay drive being derived from pcb 6. The signal path is thus via R8 only. Above 14V RLB is de-energised providing 1:100 attenuation of the input signal, adjusted by RV1.
C2, R7 and R9 are spark suppression components.
The output from this stage can be monitored at Test Point 1.

INPUT PROTECTION

Despite the use of an Input Attenuator, large input swings could still occur, sufficient to overdrive the Input Amplifier. The Input Protection circuit provides an extra safeguard, limiting the signal line excursions to approximately 17V on the 10V and 1000V ranges.

On all other ranges the output from this circuit is limited to approximately 1.7V, Zeners D1, D2 being shunted by TR3, TR4.

LED's D3, D4 are used as normal diodes in this circuit. However they can provide a useful clue to an engineer if a persistent overload indication is being investigated.

AC AND Ω

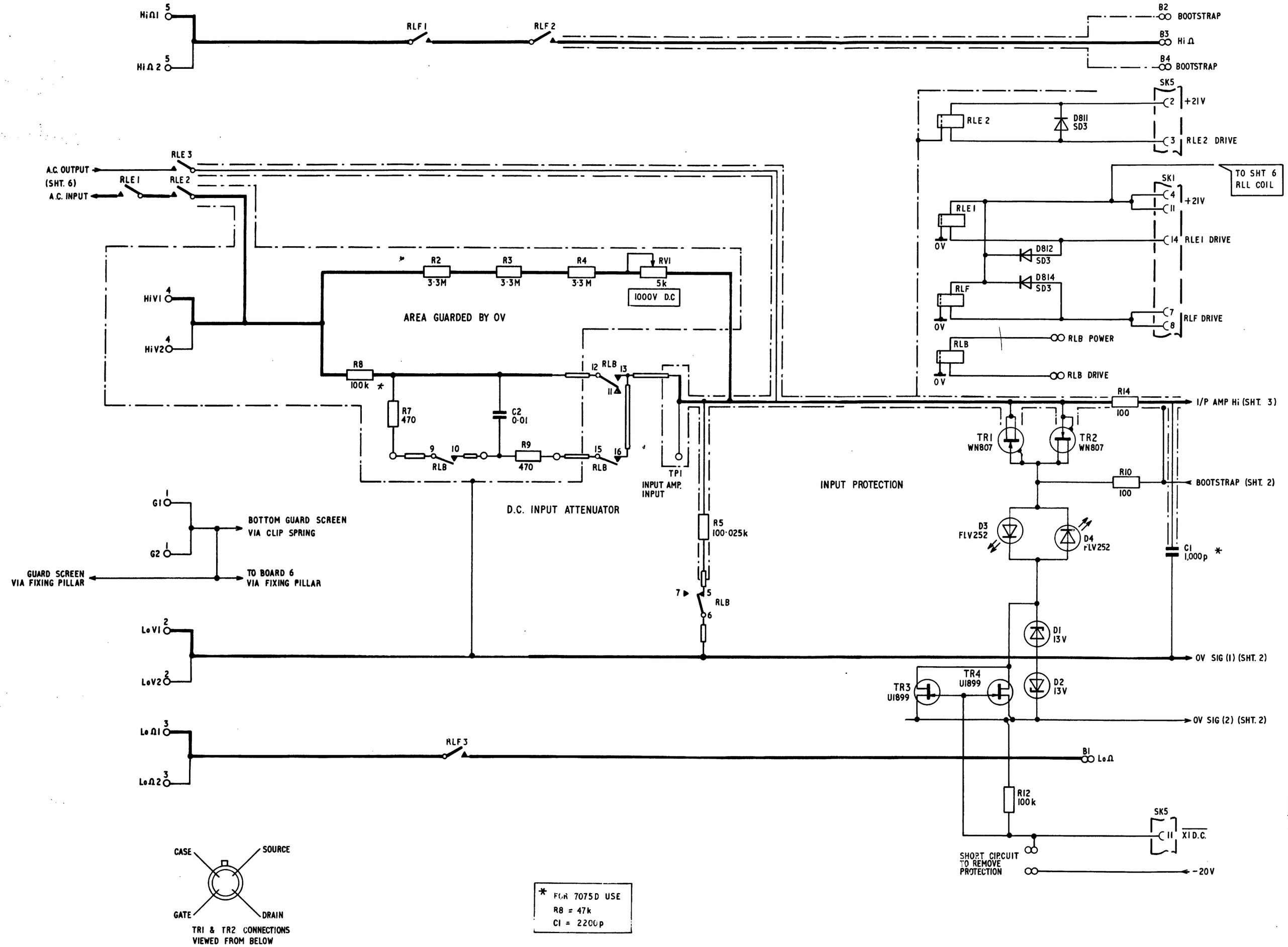
This circuit provides partial conditioning for the output from the AC/DC Converter, via RLE contacts, Input Protection being identical to that described above.

The Ohms Converter inputs are also to be found within this section of circuit, RLF providing the necessary switching.

BOOTSTRAP

Note the guard afforded to much of this circuit by the Bootstrap line. The output of a voltage follower (BOOTSTRAP AMPLIFIER, Diag 7.4) provides local voltage 'guard', supplementing the effect of the main instrument Guard. Bootstrap potential is always that of the input to the main Input Amplifier.

← PCB 5 Notations



DC Input Diag. 7.2 pcb 5 (sheet 1)

INPUT AMPLIFIER (Diag 7.3)

All input signals, however derived, are applied to this circuit, the last in the signal conditioning chain. In conjunction with the DC RANGING circuit (Diag 7.4) the signals are scaled to a level suitable for processing by the A/D converter. The circuit is "area" coded 4.

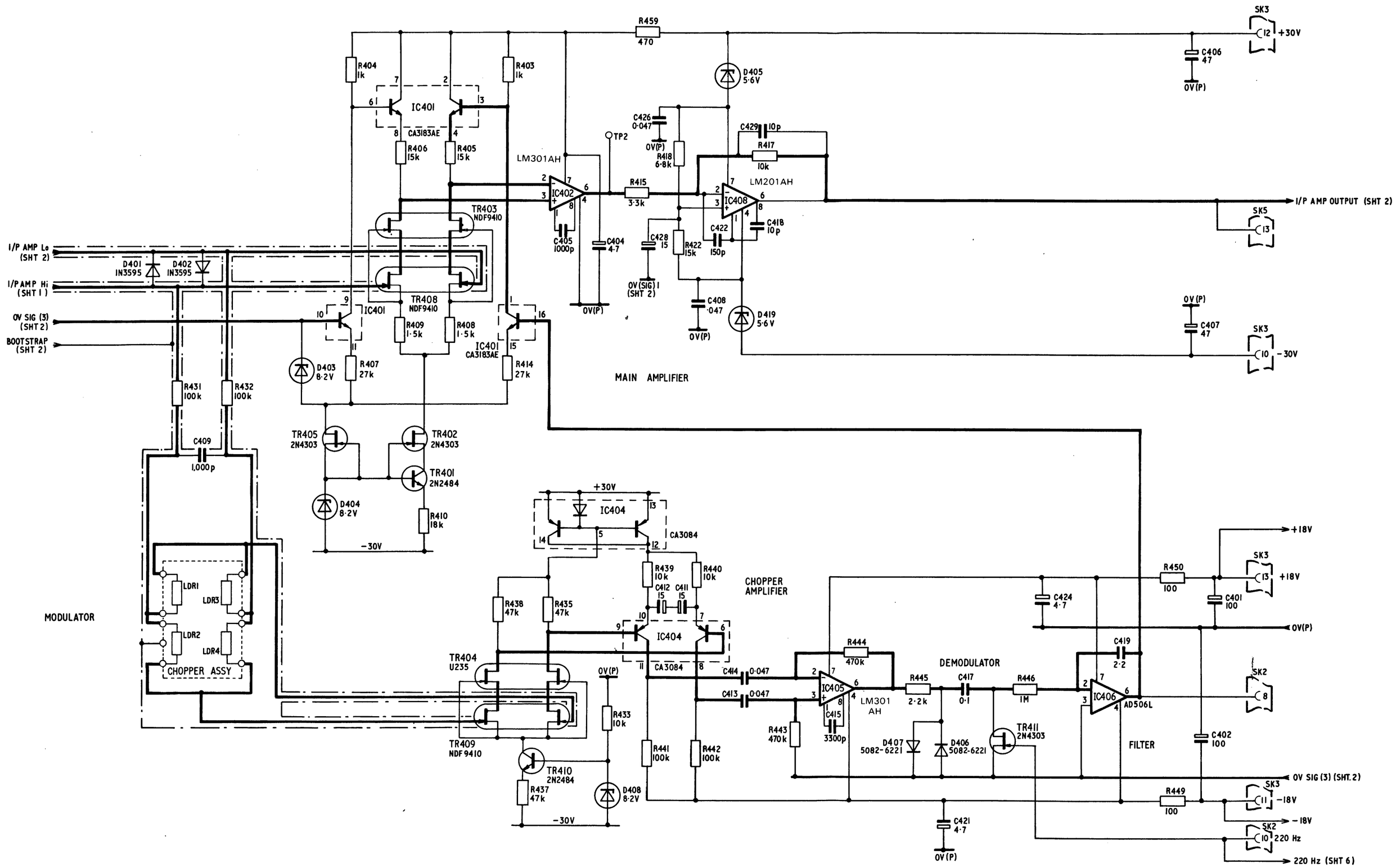
MAIN AMPLIFIER

This is the amplifying element proper, the output from the circuits on Diag 7.2 being applied to a differential amplifier, which in turn feeds the operational amplifiers, IC's 402 and 408.

The gain of this operational amplifier is determined by the range resistors shown on Diag 7.4 .

DRIFT CORRECTION

The function of the remaining circuits illustrated is that of correcting differential amplifier drift caused by temperature variations. The drift errors, being no more than a few μ volts, are amplified in a Chopper Amplifier stage, the chopping being performed opto-electronically at 220Hz. LDR's 1 to 4 are light dependent resistors forming the Modulator. The amplified error is demodulated, the same 220Hz waveform (derived from pcb 6) driving the Demodulator. After passing through the Filter the drift correction potential is applied to one side of the differential amplifier output (IC 401).



Input Amplifier Diag. 7.3 / pcb 5 (sheet 3)

DC RANGING (Diag 7.4)

The gain of the main Input Amplifier (Diag 7.3) is controlled by the scaling resistor network in this circuit, which also provides an additional measure of Input Amplifier protection, relative to Bootstrap. The circuit is "area" coded 1.

DC RANGING

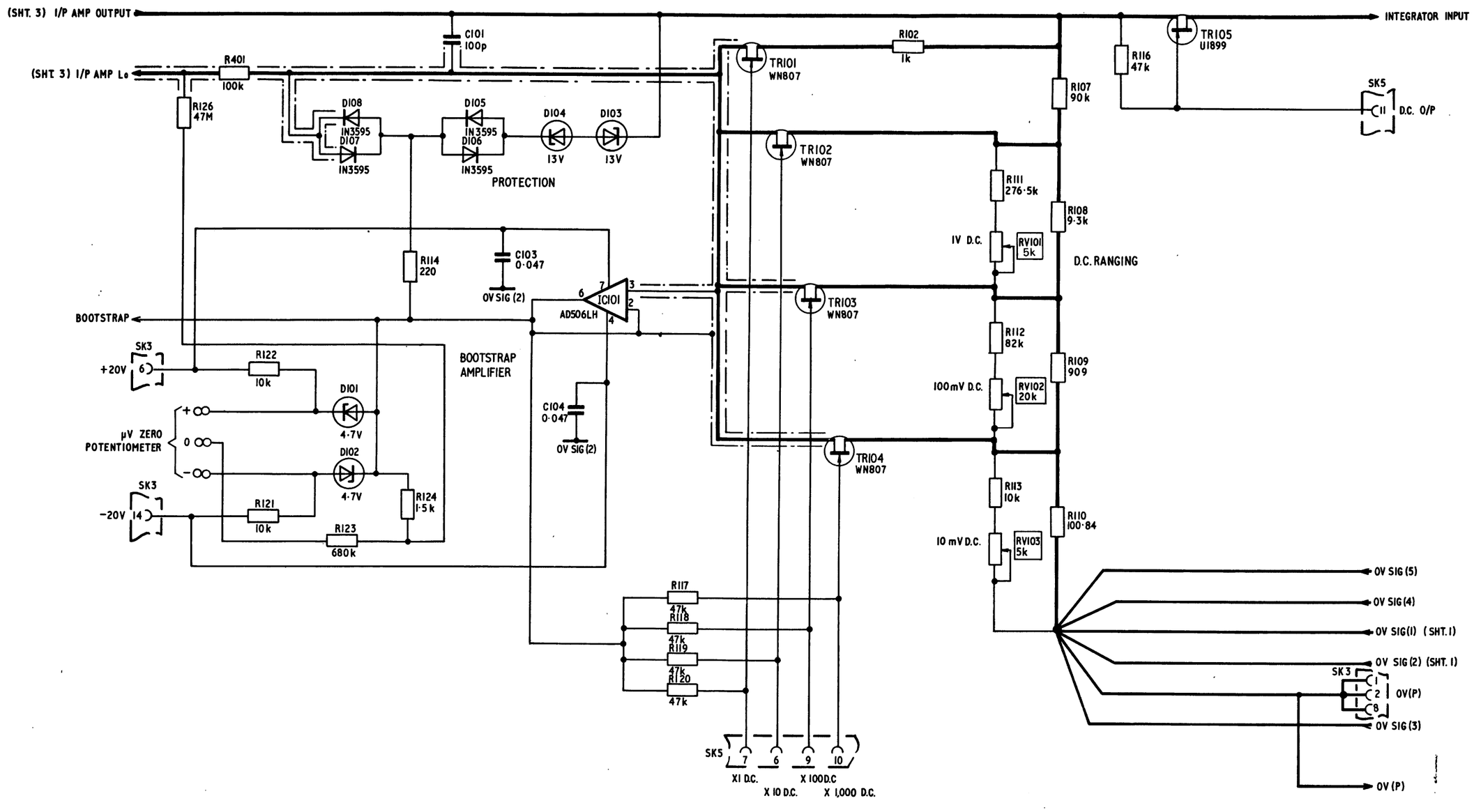
The FET switches TR's 101 to 104 are switched on by ranging signals derived from the DC Decoder on pcb 6. Thus the amplifier gain is determined by one of the matched set of 4 resistors R107 to R110. (Note that R111 completes the matched set).

BOOTSTRAP AMPLIFIER

IC101 is a low output impedance unity gain voltage follower producing an output which faithfully follows the input to the Input Amplifier. Its function in this circuit is to provide a rapid means of switching off FET's TR101 to 104. As mentioned earlier, Bootstrap also affords additional input guarding throughout the Input circuits.

PROTECTION

The Input Protection circuit shown in Diag 7.2 was concerned with protection relative to Signal 0V. The circuit shown here provides protection relative to the Bootstrap line.



DC Ranging Diag. 7.4 pcb 5 (sheet 2)

V to t CONVERTER (Diag 7.5)

This circuit performs Analogue to Digital conversion, the applied voltage being converted to time periods which are used to gate the output of a Clock circuit. The circuit is clock synchronised to ensure that the pulses in the "pulse train" start and finish exactly on a clock edge. This section of pcb 5 is "area" coded 1.

INTEGRATOR

A continuously running Dynamic Integrator is driven between preset limits by a 1kHz forcing waveform, to produce a symmetrical triangular waveform output.

LEVEL DETECTOR

Compares the excursions of the Integrator output with reference levels, switching Integrator reference potentials which maintain the closed loop action of the Integrator. This system can be regarded as having pulse-width modulated feedback — the pulse width varying in proportion to the input signal applied to the instrument.

REF. SWITCHES

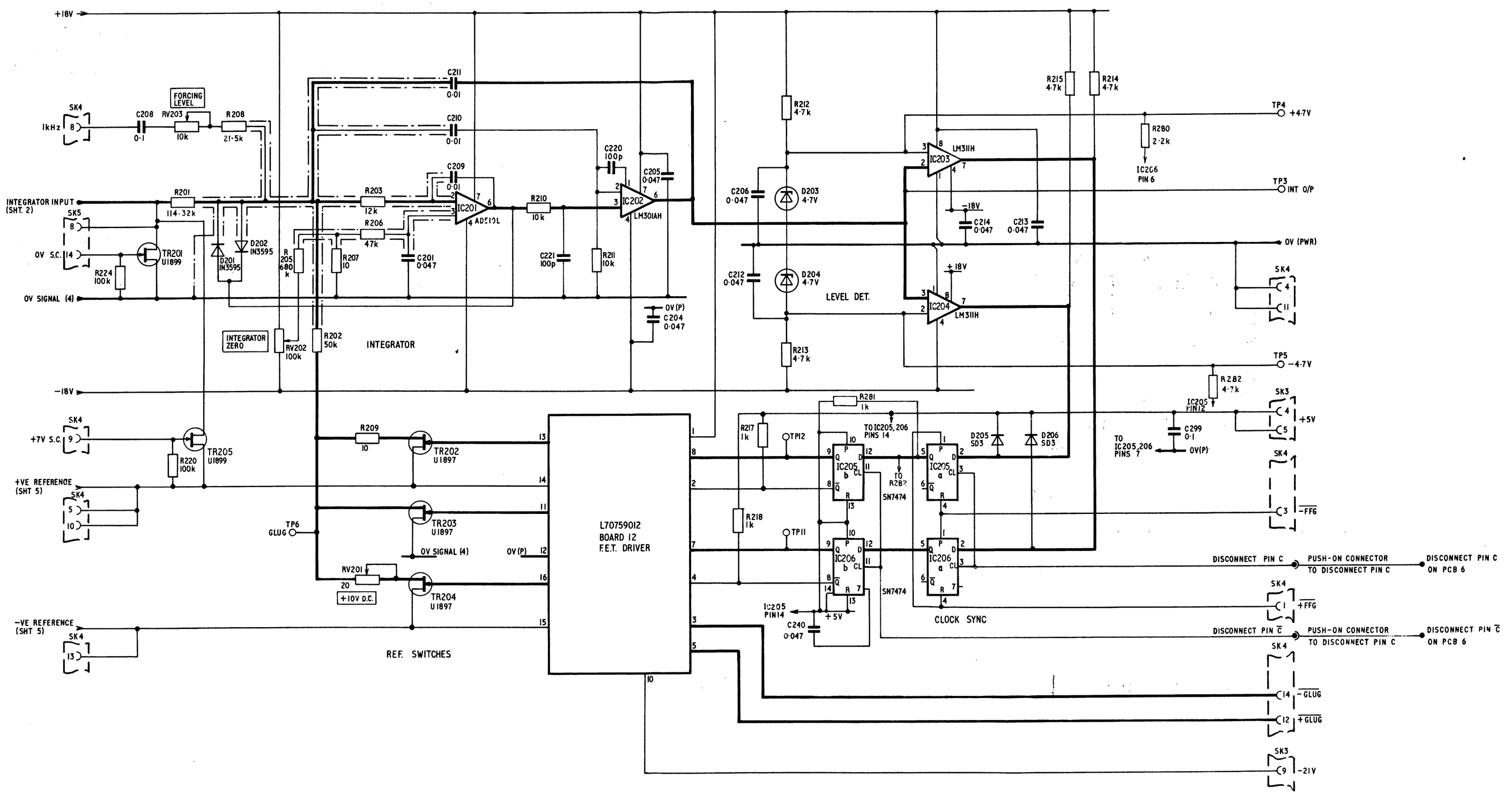
Controlled by the Level Detector via the FET Driver, these switches apply one of two reference potentials, or Sig. 0V to the "virtual earth" of the Integrator. The cut-on/cut-off of the FET switches is determined by the polarity of the input (dc) and its magnitude. The voltage across R202 can be represented by a train of positive and negative pulses, running at 1kHz, the pulse width being variable with voltmeter input.

CLOCK SYNC.

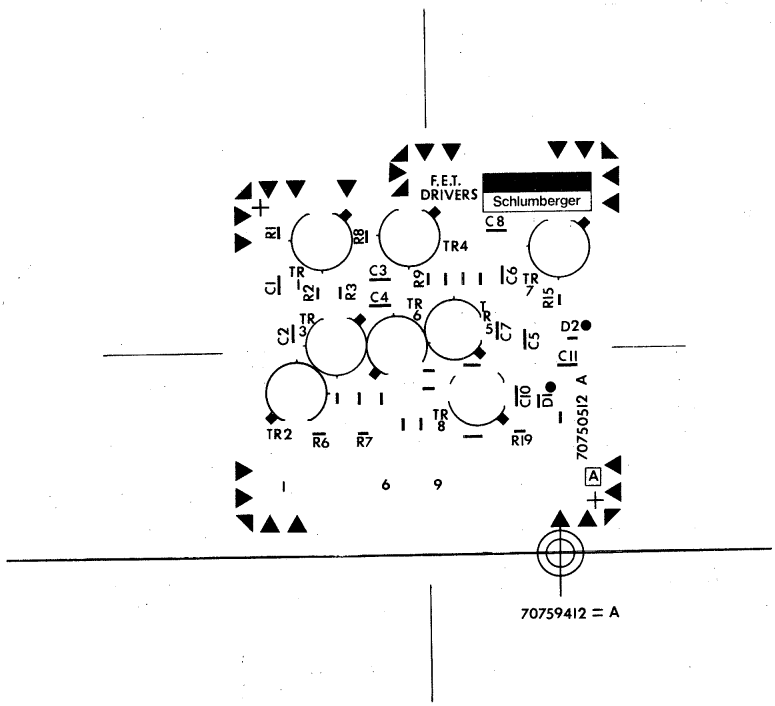
Synchronisation of the feedback waveform with the Clock is achieved by this section of the circuit.

FET DRIVER

The circuit carried on pcb 12 is described overleaf.



V to t Convertor Diag. 7.5 | pcb 5 (sheet 4)



PCB 12 Notations

FET DRIVERS (Diag 7.6)

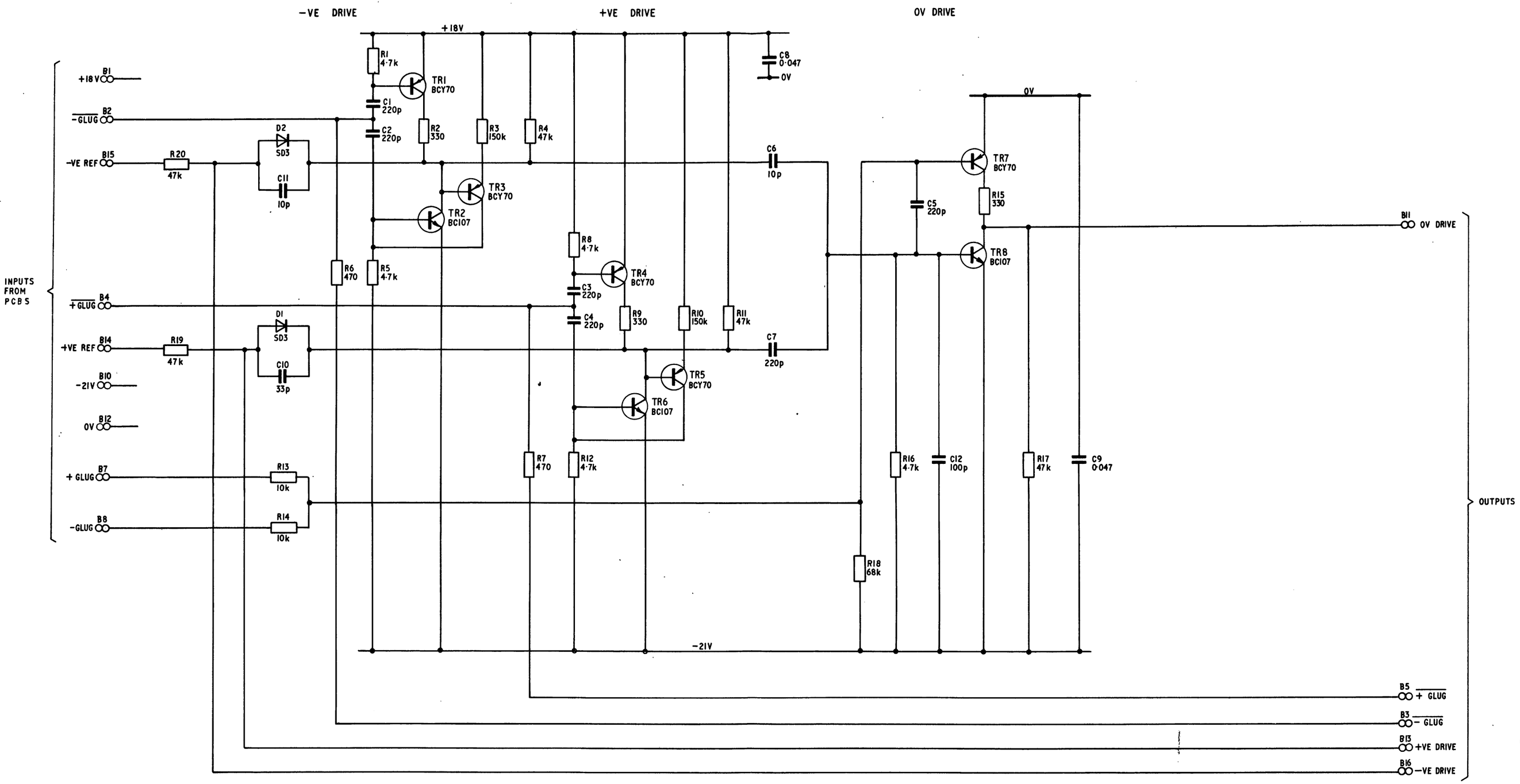
The circuit illustrated, though forming part of the reference switching arrangement on Diag 7.5, is carried on a separate plug-in card, pcb 12. Interconnection with board 5 is via Berg-type horizontal sockets, the mating pins being mounted vertically on board 5.

The FET Drivers provide fast switching of the reference potentials and 0V, the circuit configuration ensuring rapid transition from one switch state to the other. TR3, TR5 perform a 'latching' function for the ON state of their associate switches. In the case of the 0V switch both ON and OFF states are latched by the inputs on pins B7, B8. Pins B6, B9 are not used.

GLUG

Within this manual the reader will find many signal annotations which include the word "Glug". The word may be abbreviated to the letter 'G', as in FG (*forced* glug), FFG (*forced forced* glug) etc. The term is used as a convenient alternative to the cumbersome title "Quantum of Charge" (i.e. V × t) and should be treated merely as an identifier label, facilitating circuit tracing.

◄—— **PCB 12 Notations**



Fet Drivers Diag. 7.6 pcb 12

AC CONVERSION (Diag 7.7)

Diag. 7.7 illustrates the circuits concerned with processing an alternating input to produce an equivalent dc level. The dc thus obtained is further conditioned as described in earlier pages under "DC". This circuit is "area" coded 7 on pcb 5.

AC ATTENUATOR

Three alternative signal paths provide attenuation as follows:

On the 1000V range	1 : 1000 via R701, R702, RLL
On the 10V, 100V ranges	1 : 100 via R701, TR701
Other ranges	no attenuation via RLC

The output from this stage is thereby scaled to a maximum of 1V. Relay drive for RLC and RLL is derived from the AC DECODER circuit (FLOATING LOGIC pcb 6), as is the signal AC ATTEN. Potentiometers RV702, RV703 provide attenuator adjustment for the 10V and 1000V ranges while C736 is adjusted to balance the attenuator for 100V at input frequencies above 10kHz.

BUFFER

The Buffer Amplifier has a dual role, that of isolating the input from the low input impedance of the Converter and of providing amplification of small input signals from the attenuator. Buffer gain is switched between unity and X10 by TR's 705, 706, R704 controlling the gain at 100mV.

AC SCALING SUMMARY

Nominal Range	Attenuation			Buffer gain	
	1 : 1000	1 : 100	1 : 1	X1	X10
100mV	–	–	√	–	√
1V	–	–	√	√	–
10V	–	√	–	–	√
100V	–	√	–	√	–
1000V	√	–	–	√	–

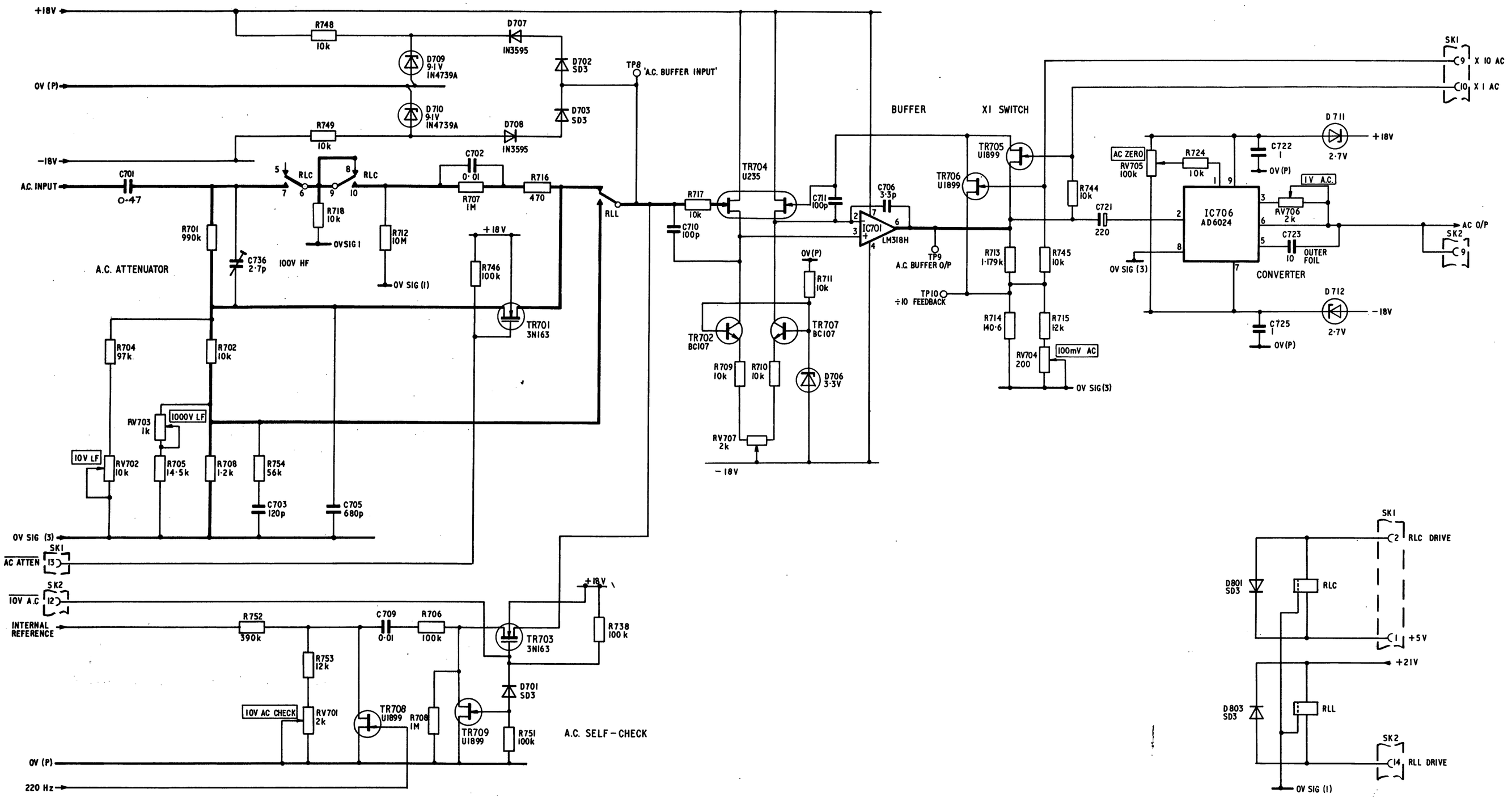
CONVERTER

IC706 with its associated components performs the conversion of the rms of the ac to a dc level.

Zero adjustment is provided by RV705, the 1V output potentiometer being RV706.

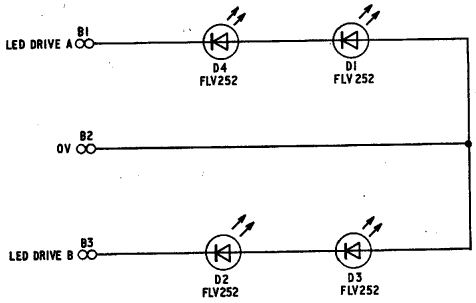
SELF CHECK

The voltmeter internal reference is chopped at 220Hz and applied as a 100mV ac "reference" to the Buffer, via the switch TR709, TR703. The 1V signal thus obtained is scaled to give a Self Check display of 10V.

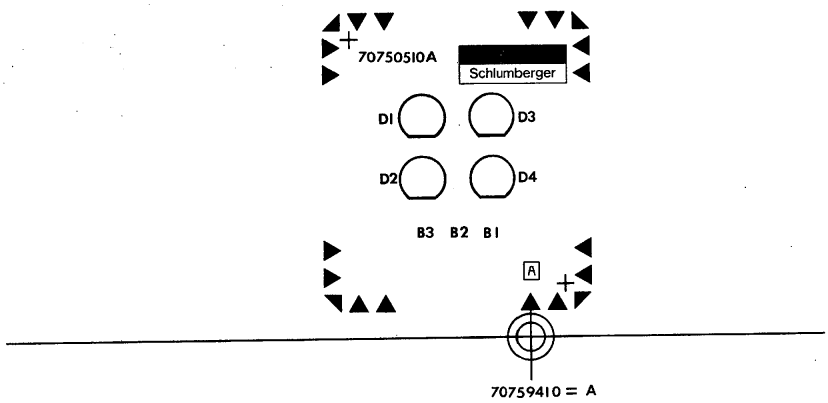


AVOID STATIC M.O.S.

AC Conversion Diag. 7.7 pcb 5 (sheet 6)



PCB 10 Circuit Diagram



PCB 10 Notations

RESISTANCE (Diag 7.8)

Resistance measurement with the 7075 is accomplished by measuring the voltage developed across the unknown resistor by virtue of a known current passing through it. The major function of the section of Board 6 illustrated is that of generating the necessary current. The circuit is "area" coded 6.

CURRENT GENERATORS

The instrument's negative reference is utilised to determine a current which, in it's turn, produces a reference potential relative to the +30V rail — divided down across R602, R604 (a matched set). This potential defines the Hi Current, the value of which depends on the position of reed switches as follows:

RLH 1 closed	1mA	(10Ω to 10kΩ)
RLG 1 closed	10μA	(100kΩ to 1MΩ)
Both reeds open	1μA	(10MΩ)

The Lo Current generator provides the necessary current sink to give effective 4 - terminal measurement, potentials arising from lead resistances being nullified. The second contacts of reeds RLG, RLH perform a similar function to those outlined for RLG1, H1 above.

Link A across R603 is set as required during factory calibration. IC's 601 to 603, unity gain amplifiers are used in this configuration as voltage followers. High voltage (up to 300V) protection is given by D606, R610 and TR's 605 and 606.

Note that the Hi Current circuits are guarded relative to the potential developed across R604, Bootstrap providing the remaining guard potential.

SELF CHECK

The 1mA current through R608 in parallel with the input resistance of the Integrator produces 10V for the nominal Self Check 10kΩ display. Control is via RLD.

CHOPPER DRIVE

Also illustrated in Diag 7.8 is the 220Hz Generator (area code 4) which produces the chopping waveform used in the Input Amplifier circuit (Diag 7.3). Outputs are taken via Berg pins 5 and 7 to the LED's forming part of the opto-electronic Chopper Modulator (Diag 7.3). A further output feeds the Demodulator in the same circuit area of pcb 5. A link is provided across R454 to permit a small adjustment of the nominal 220Hz, if the oscillator frequency is found to be a harmonic of the supply frequency.

PCB 10 Notations and Circuit Diagram

Resistance Diag. 7.8 pcb 6 (sheet 1)

REFERENCE (Diag 7.9)

The voltmeter's reference potentials are generated in the circuits illustrated, which are "area" coded 3 on Board 5. The other circuit, coded 5, processes the External Reference associated with RATIO operation.

INTERNAL REFERENCE

Zener D301 defines the +ve Reference at +9V above the potential of the inverting input of IC301. The zener current is that through R301 derived from the Inverter. The junction of the matched pair R321 R322 is at −2V, regulated by the action of IC301, TR301. Thus the emitter of TR301 is held at +7V, which is used as the +ve Reference.

The network R311 through R320, with RV301, is used during calibration to take out zener tolerances and thus accurately define the +7V.

REFERENCE INVERTER

The system is stabilised by using an inverted version of the +ve reference as the current source for D301. A closed loop is thus formed, producing −7V at TR302 emitter for use as the −ve Reference.

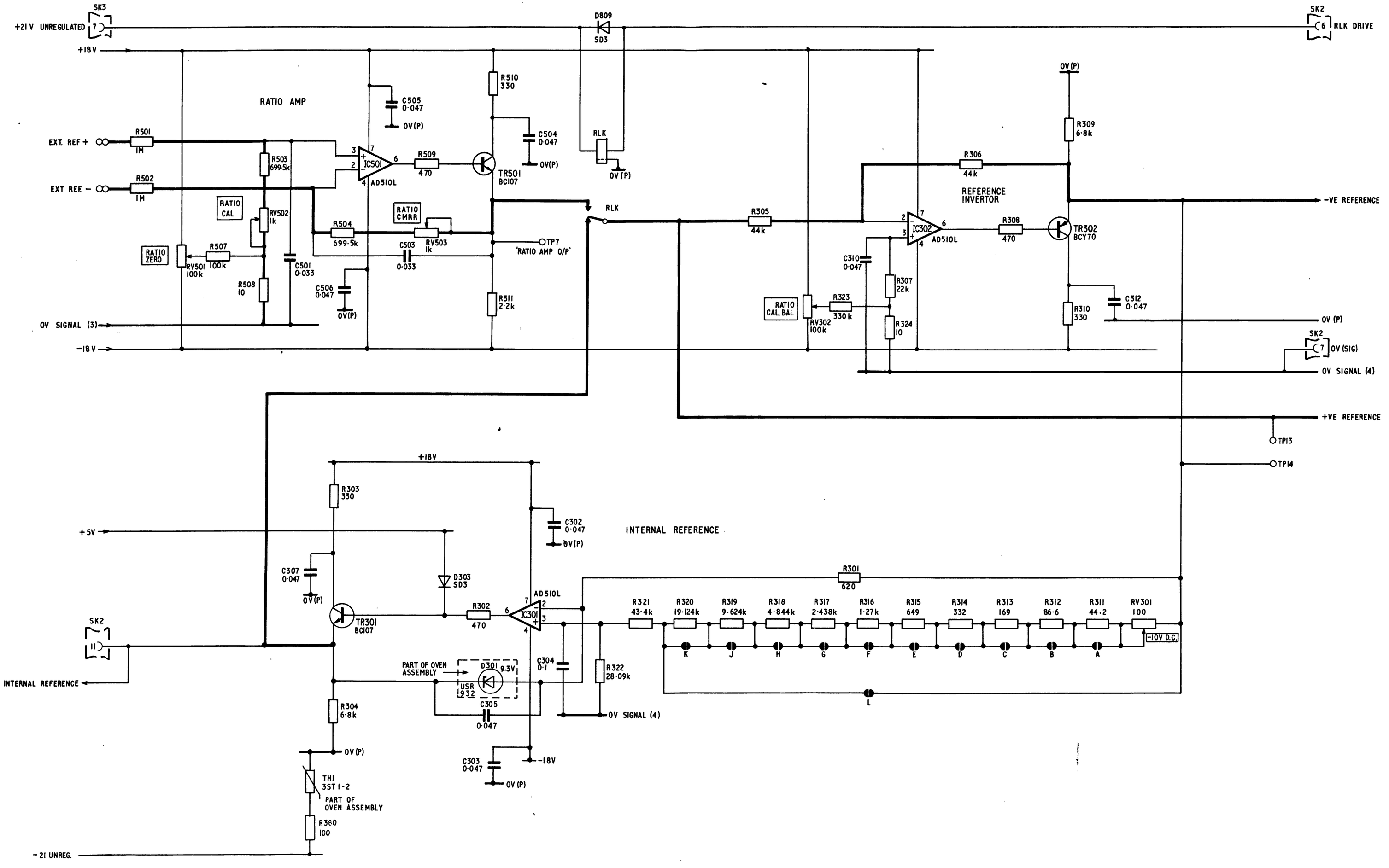
The circuits described, once set up, are very stable and independent of variations of the 18V rails. However under certain circumstances it would be possible for latching to occur in the wrong direction. D303 prevents this by holding TR301 base above +5V.

RATIO AMP

An external reference is fed to the Inverter via IC501, TR501 and the changeover relay RLK. This replaces the Internal Reference with the user's choice of reference potential for RATIO measurement.

RV503 corrects for Common Mode errors between Ratio Hi and Ratio Lo, RV502 setting the output of IC501/TR501. Offsets in the IC are taken out by RV501.

Offsets in the amplifier IC302 are taken out by adjusting RV302, **such adjustment forming part of the RATIO calibration procedure.**



Reference Diag. 7.9 pcb 5 (sheet 5)

FLOATING LOGIC (Diag 7.10)

The main function of the area of Board 6 coded 8 is that of decoding Front Panel (and Systems Interface*) Commands associated with measurement Mode (Function) and Range. The circuits are floating with respect to supply 0V, data transfer being accomplished by means of optical couplers. The circuit coded 2 forms parts of the V - to - t Converter (Diag 7.5).

SERIAL DECODER

Data is sent at the beginning of each reading to determine the Function and the measurement Range. The state of the Serial Data lines is fed as an 8 - bit serial word to the Serial Decoder, strobed by an 8 - pulse clocking signal, Serial Strobe (Test Point 12). The resulting data is set on lines A to H of the 8 - bit shift register IC819.

NOISE REJECTOR

This binary counter circuit only produces a strobe output if the 8 - pulse clocking signal is complete. Thus spurious noise peaks are not detected as Clock pulses.

The strobe thus produced clocks the output lines of the Shift Register into a pair of 4 - bit buffer stores, IC's 814 and 815, the decoded Mode and Range data being held for the duration of the current reading.

SK8 is a test socket for use with an ATE device such as Membrain.

MODE DECODER

Apart from RATIO, which is processed directly into a drive for RLK (Diag 7.9) the binary Mode code and that for Self Check are decoded in a 4 to 16 line decoder IC802. For each of the possible input codes one of the 16 output lines is set Lo. All 16 outputs are connected, those corresponding to each measurement mode being commoned in 4 - way wired OR networks. The remaining 4 outputs specify the measurement tests of the Self Check function — shown in tabular form overleaf.

AC DECODER

IC's 803, 804 and 805 (excluding pins 5, 11 and 2, 14) provide the necessary decoding and current drive for the control of the AC signal conditioning circuits (Diag 7.7). The input on pin 12 of IC803 is the $\overline{AC}$ decode from the Mode Decoder, the other inputs being binary coded Range data from IC815.

OHMS DECODER

Control for the Ohms Converter (Diag 7.8) is derived from this circuit, the input being $\overline{\Omega}$ from the Mode Decoder and Range data in binary code from IC815.

DC DECODER

Together with part of IC805 (pins 5 and 11), this section of the circuit generates the control and drive signals for the DC Signal Conditioning circuits (Diags 7.2, 7.3, 7.4). $\overline{DC}$ and binary coded Range data are the inputs, derived from IC802 and IC815 respectively.

*see Section 10 of this manual.

SELF TEST (Diag 7.10)

Test	IC802 Pin No.	Decoded/Processed by	Range/Mode Selection	Control Signal Output	Effective on Diagram
7V dc	5	IC813(b), IC805		7V SC	7.5
			D804, IC808	DC O/P	7.4
0V	1	IC811(d), IC808		0V SC	7.5
			D813, IC808	DC O/P	7.4
10V ac	14	IC805		10V AC	7.7
			IC811(b), IC812(e).	RLE/2 DRIVE	7.2
			IC809(b), IC811(c), IC808, IC807.	X10 DC (Note 1).	7.7
10kΩ	9	IC810(c)		RLD DRIVE	7.8
			D805, IC808	DC O/P	7.4
			IC810(c), D815	RLH DRIVE (Note 2)	7.8
Display	— (Note 3)	—	—	—	—

Notes

1. This control signal selects the correct scaling factor for the test ac.
2. RLH is energised to provide a measurement current of 1mA.
3. Self Check Test No. 5 is not decoded on this board. The Control Signal LAMP TEST, derived from the Self Check logic on pcb 3, is connected directly to pcb 2. The decode is equivalent to Test 1 (code 00).

INTEGRATOR CONTROL (Diag. 7.10)

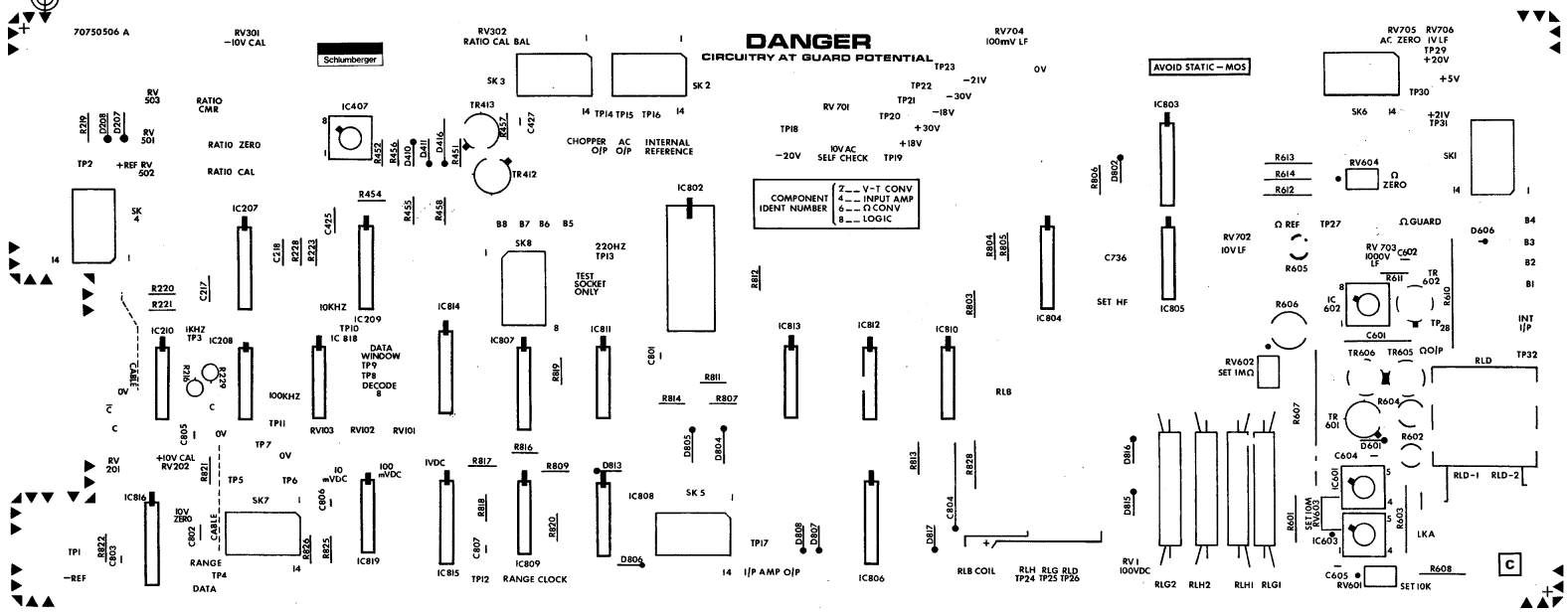
The Integrator Control logic, "area" coded 2, provides controlling waveforms for the dynamic integrator described earlier (V - to - t CONVERTER, Diag 7.5). A floating circuit, the inputs to it are made via optical couplers.

INTEGRATOR CONTROL

Clock pulses are processed by IC209, the three sections of which provide ÷ 16, ÷ 10, ÷ 10 to the input 1.6MHz. The resulting square wave at 1kHz is the Forcing Waveform (FW) controlling the ramp up and down of the Integrator (Diag 7.5). D207 limits the positive excursions of FW to +10V.

The 1kHz signal is further processed by IC207(a) and (b) to produce two pulses, each coincident with an edge of FW. The pulses, $+\overline{FFG}$ AND $-\overline{FFG}$, are utilised in the Clock Sync circuit of the V - to - t Converter (Diag 7.5).

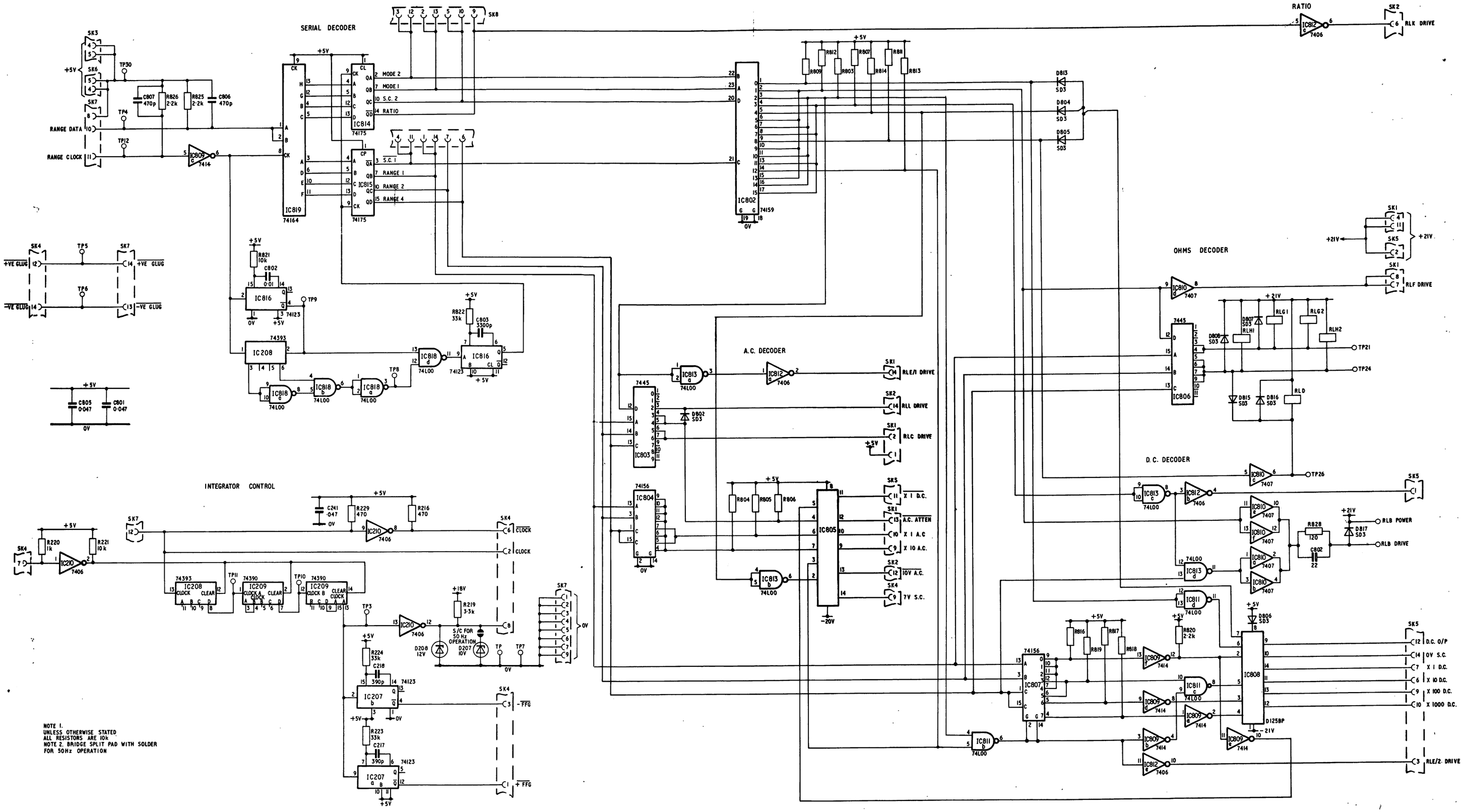
PCB 6 Notations ⟶



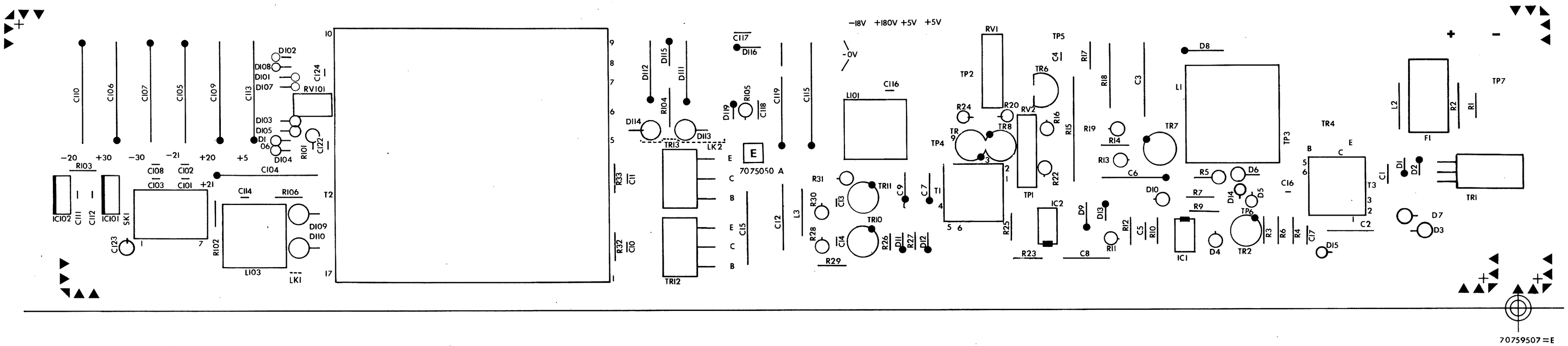
THIS BOARD MUST BE SILK SCREENED WITH YELLOW PAINT.

PCB 6 Notations

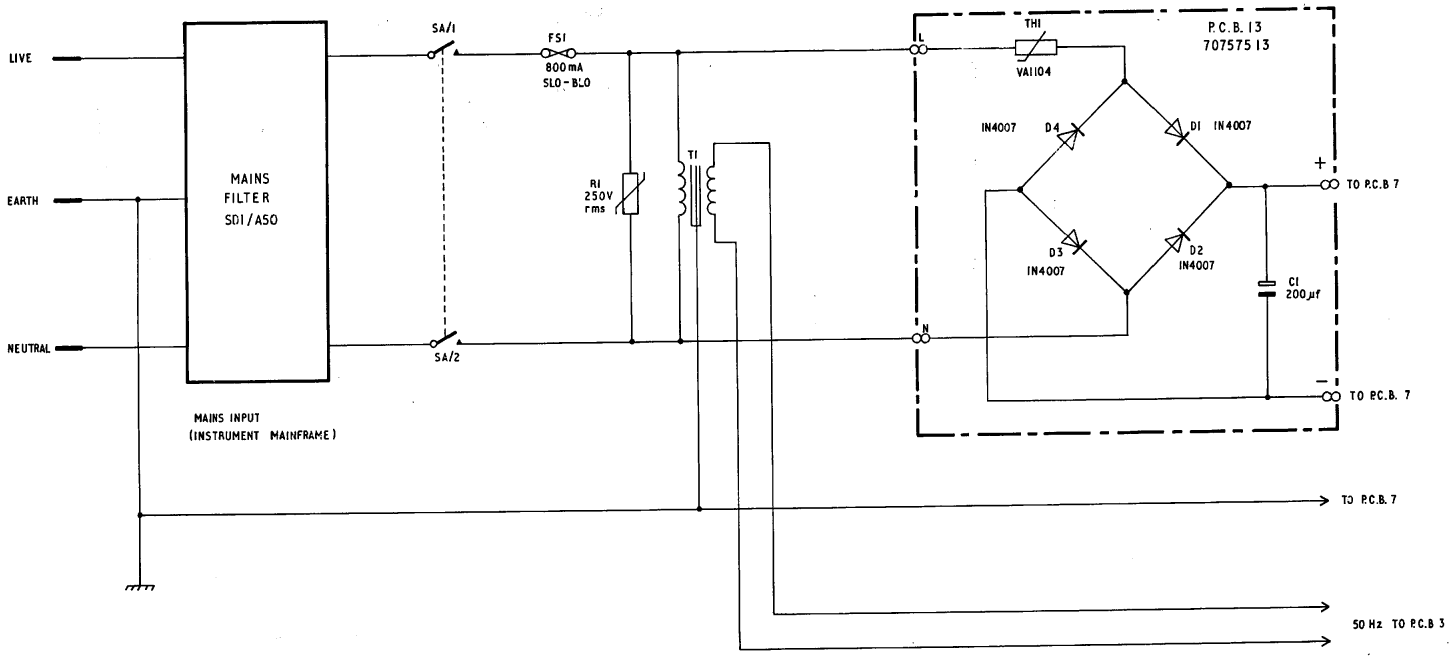
JWW/7075/5



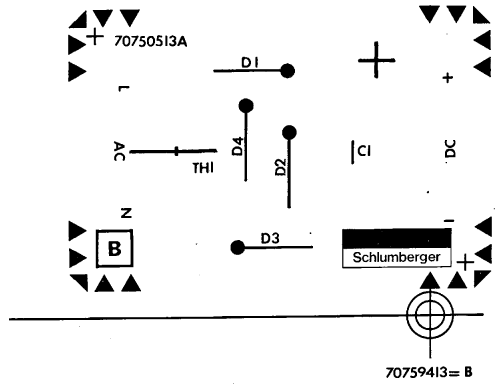
Floating Logic Diag 7.10 pcb 6 (sheet 2)



PCB 7 Notations



Mainframe Diag. 7.11



PCB 13 Notations

POWER SUPPLY (Diag 7.12)

PCB7 contains a dc-dc converter which uses the rectified mains input from pcb13 (Diag 7.11), applied directly without the use of a mains transformer, to produce all the regulated dc supplies for the instrument. A switching regulator circuit is employed to maintain a very stable supply to the inverter. A start-up circuit, and voltage and current overload protection circuits are also employed.

The start-up, switching regulator and inverter circuits are shown in Diag 7.12, while the rectification and regulaton circuits are shown on Diag 7.13.

WARNING

Floating supplies are output from this instrument, for safety, always use an isolating transformer.

START UP

TR1 and associated components form a start-up circuit. The function of this circuit is to supply current to the switching regulator IC1 when the instrument is first switched on. In this condition, TR1 is biased on, the 30V rail is at a nominal 27 volts and the switching regulator (IC1) starts to oscillate. As the voltage on the 65V rail (TP5) builds up, current for the 30V rail (TP1) is supplied from the 65V rail via R17 and R15. The 30V rail rises to 30V when it is caught by D3 and D7, causing TR1 to be biased off. The higher, normal operating current for the 30V rail is now supplied only from the 65V rail. This is a more efficient arrangement as less power is dissipated in the dropping resistors.

SWITCHING REGULATOR

IC1 and associated components from a switching regulator which is designed to convert the dc input supply to a regulated mean level of 65V.

When the instrument is switched on, the reference voltage at IC1 pin 3, slowly builds up to a level of 5.6V, due to the action of D10 and C6. If the voltage at IC1 pin 2 is less than the reference voltage, IC1 pin 6 will be at 28V, causing C5 to charge up via D14 and R7, dependent on supply voltage. When this feedback voltage at IC1 pin 2 crosses the reference level, the output of IC1 (pin 6) goes low, causing C5 to discharge via R11 and R1. This starts the oscillatory condition in IC1. A sawtooth waveform, mean value 5.6V, is produced at IC1 pin 2 and a pulse train is produced at the output, IC1 pin 6. This pulse train output from IC1 is used to switch TR4, via TR2, T3 and associated components. TR2 and its associated compoments ensure that the T3 primary current is switched hard off when the IC1 output is low. They also ensure that the mean dc level at T3 primary is zero over a full cycle (mark-space) of IC1 output. T3 itself provides a current magnification of 10 and also isolates the high voltage input from the switching circuitry. The dc input voltage is switched by TR4 to produce a mean level of 65V (at TP2). This 65V is routed to the centre-tap of T2 primary, and provides a very stable supply for the inverter.

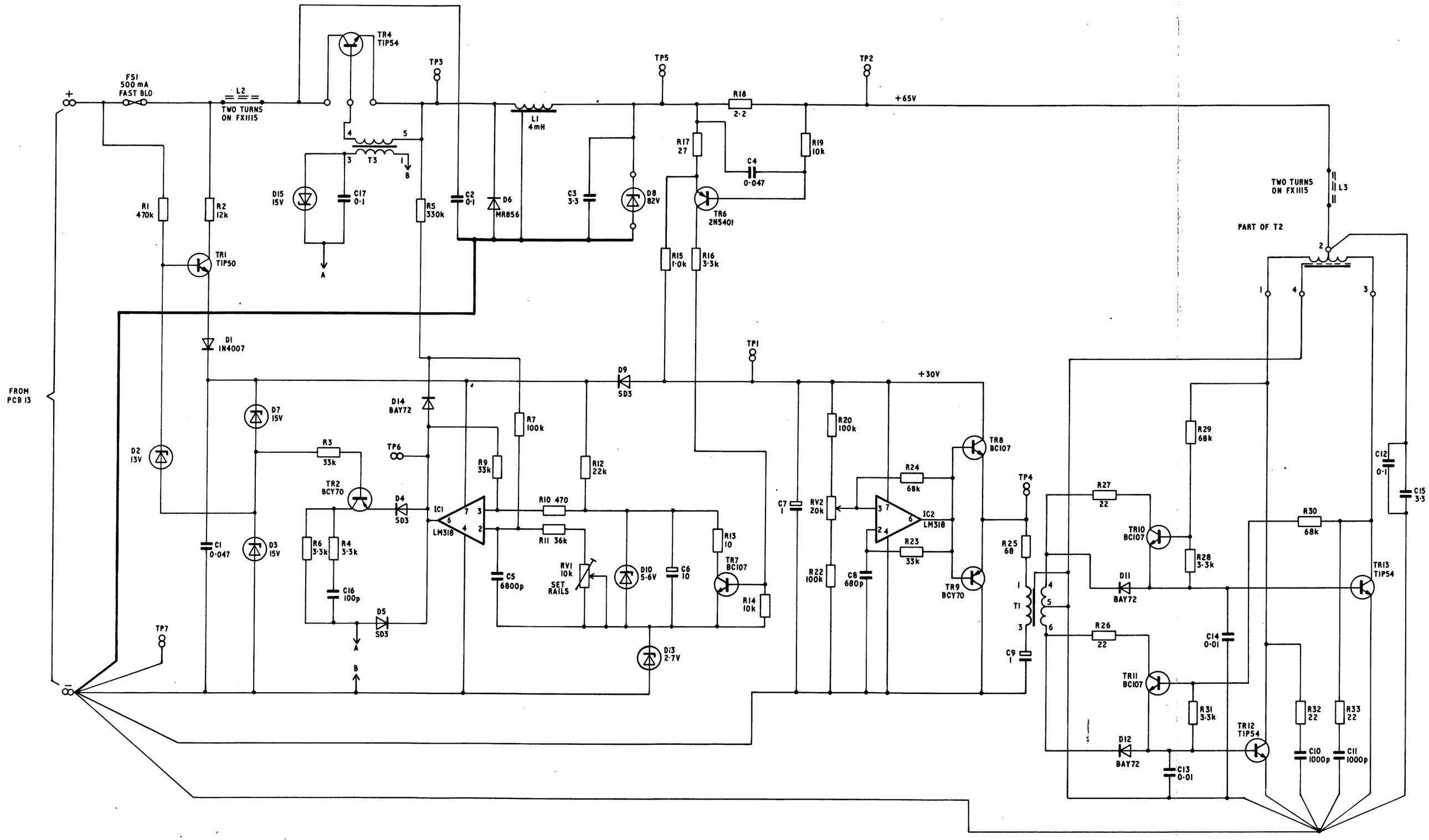
The level of the 65V will always be approximately ten times that of the reference input at IC1 pin 3.

When the voltages on the 65V and 30V rails have settled, IC1 will output a pulse train having a mark-space ratio which is dependent on the input supply voltage.

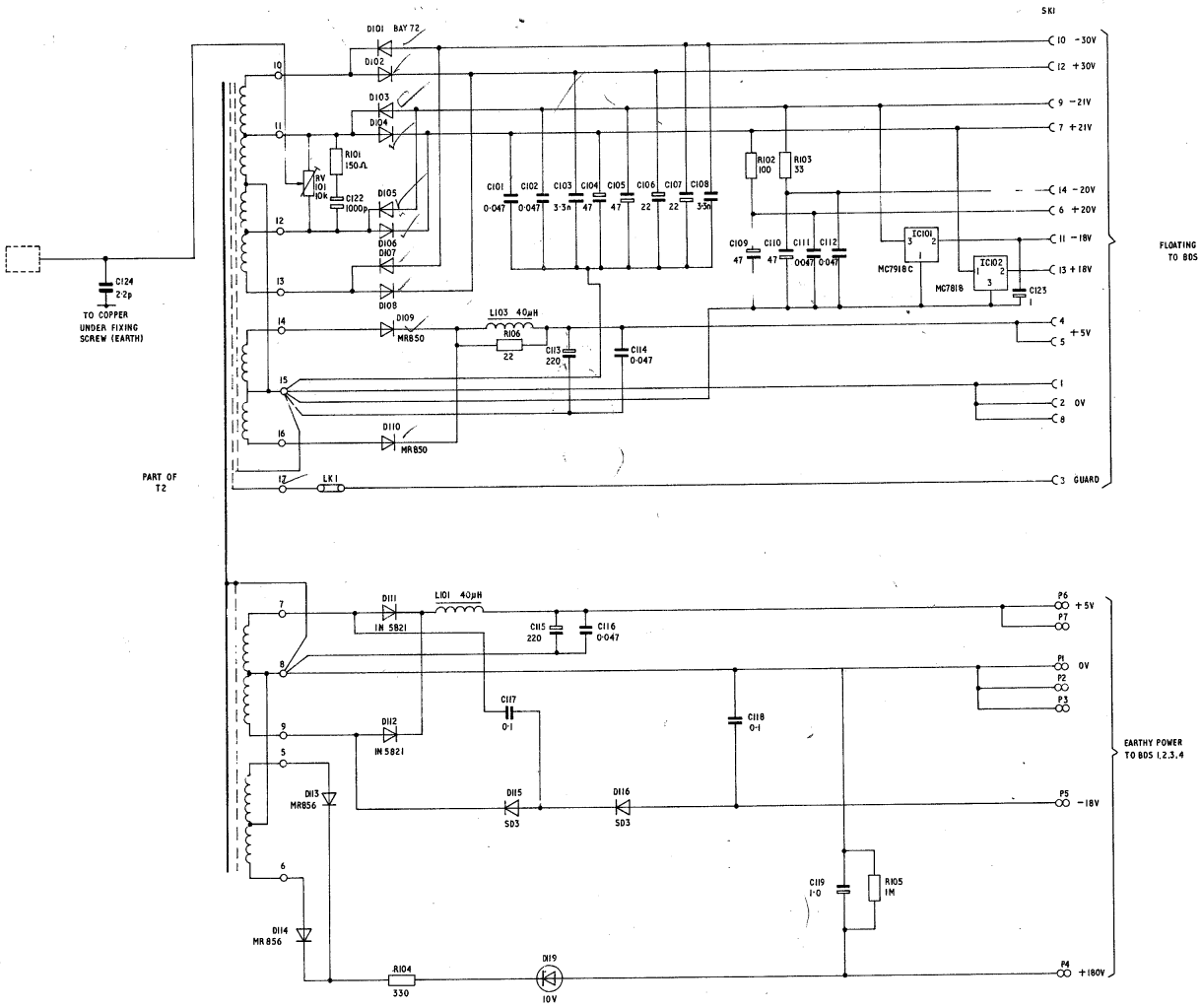
For a 240V mains operation, the input will be approximately 350V dc and the IC1 mark-space ratio will be approximately 1:4.

For 120V mains operation, the input will be approximately 140V dc and the IC1 mark-space ratio will be approximately 1:1.

← **Diag. 7.11. PCB 7 and PCB 13 Notations**



Power Supply Diag. 7.12 pcb 7 (sheet 1)



Rectification Diag. 7.13 pcb 7 (sheet 2)

INVERTER

IC2, TR8, TR9 and their associated components form a 25kHz square wave oscillator. RV2 sets the mark-space ratio, and should be set to give an even ripple at TP2, produced from a nominal 1:1 mark-space ratio at TP4. The output from TR8 and TR9 is coupled to the output drivers TR12 and TR13 via T1, TR10 and TR11. TR10 and TR11 ensure that TR12 and TR13 cannot conduct at the same instant, thereby preventing excessive current in the T2 primary. Only when TR12 has turned off can TR10 turn on, and thus switch on the drive to TR13 via R27. When TR13 switches on, TR11 is held off, and no drive can be supplied to TR12 (via R26), until TR13 is switched off in the anti-phase cycle of operation.

VOLTAGE OVERLOAD PROTECTION

D8 is a special 'fail-short' zener which provides protection in the event of voltage overload on the 65V rail. If this situation arose, i.e. if TR4 became short-circuited, D8 would fail short-circuit and cause fuse FS1 to blow. As the short circuit condition is irreversible, D8 must then be replaced, and the cause of the fault rectified before the instrument is switch on again.

CURRENT SENSING

The current drawn from the 65V rail is sensed by TR6, R18 and their associated components. If excessive current ($>0.75A$) is drawn, the voltage drop across R18 increases and TR6 starts to conduct. This causes TR7 to conduct and thereby lowers the reference voltage at IC1 pin 3. The switching regulator produces an output having a lower mark-space ration, which lower the output voltage at TP3. The current sensing circuit produces a 'current foldback' effect whereby the current through R18 required to cause TR6 to conduct, becomes less as the voltage at TP6 decreases. This effect causes the circuit to respond very quickly. When a current overload occurs the switching regulator will be switched down to produce an output waveform with a very low mark-space ratio.

RECTIFICATION AND REGULATION

The various dc supply rails, floating and earthy, (Diag. 7.13) are derived from the conventional rectifiaction and smoothing circuits. IC101 and IC102 are voltage stabilisers for the +18V and the −18V rails. RV101, whose wiper is connected via C124 to mains earth, provides adjustment for minimum spike feedback at the 7075 HI and LO input terminals.

SETTING RV101

1. Connect the HI and LO terminals of the 7075 together.
2. Connect an oscilloscope probe to the shorted HI/LO terminals.
3. Connect a 10kΩ resistor between the probe and the oscilloscope screen.
4. Adjust RV101 for minimum spikes on the oscilloscope display.

The earthy −18V rail which supplies the display tube 'keep alive' electrodes (Diag 7.20) is derived from the voltage trebler network.

The earthy +180V provides the HT supply for the display tubes.

← Diag. 7.13 Diag. 7.14 →

DIGITAL

This part of section 6 covers those circuits which convert the pulses generated in the A/D converter into a digital count, which after further processing is used to drive the display.

The Block Schematic Diagram (Diag 7.14) illustrates the functional layout of the digital section, which for convenience, can be considered as having 3 sub-sections:

1) **Counters and Memory (Diag 7.15, 7.16)**
2) **The Control Logic (Diag 7.17, 7.18)**
3) **The Display, Display Drive and Phase Locked clock (Diag 7.19, 7.20).**

COUNTERS AND MEMORY

This sub-section is illustrated on two sheets, Diag 7.15 and 7.16, and comprises the counter chain with its associated input circuits, the data transfer Multiplexer and the Random Access Memory (RAM) including the necessary Read/Write logic. The Timing Counter, together with the organisational logic associated with the formatting of the geographical display is shown on Diag 7.16.

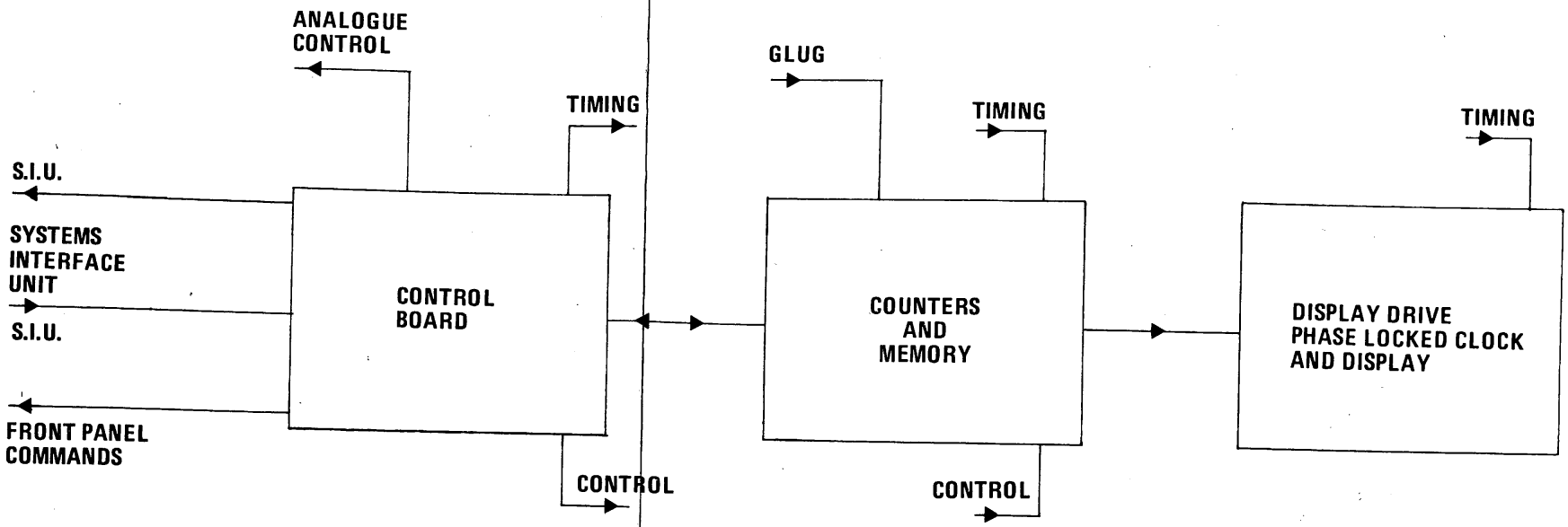
THE CONTROL LOGIC

This board controls the other logic boards and the floating circuitry. Shown on Diag 7.17 are the Main Control, the Range Control logic and Self Control logic circuits, the "State" Counter and its decoder.

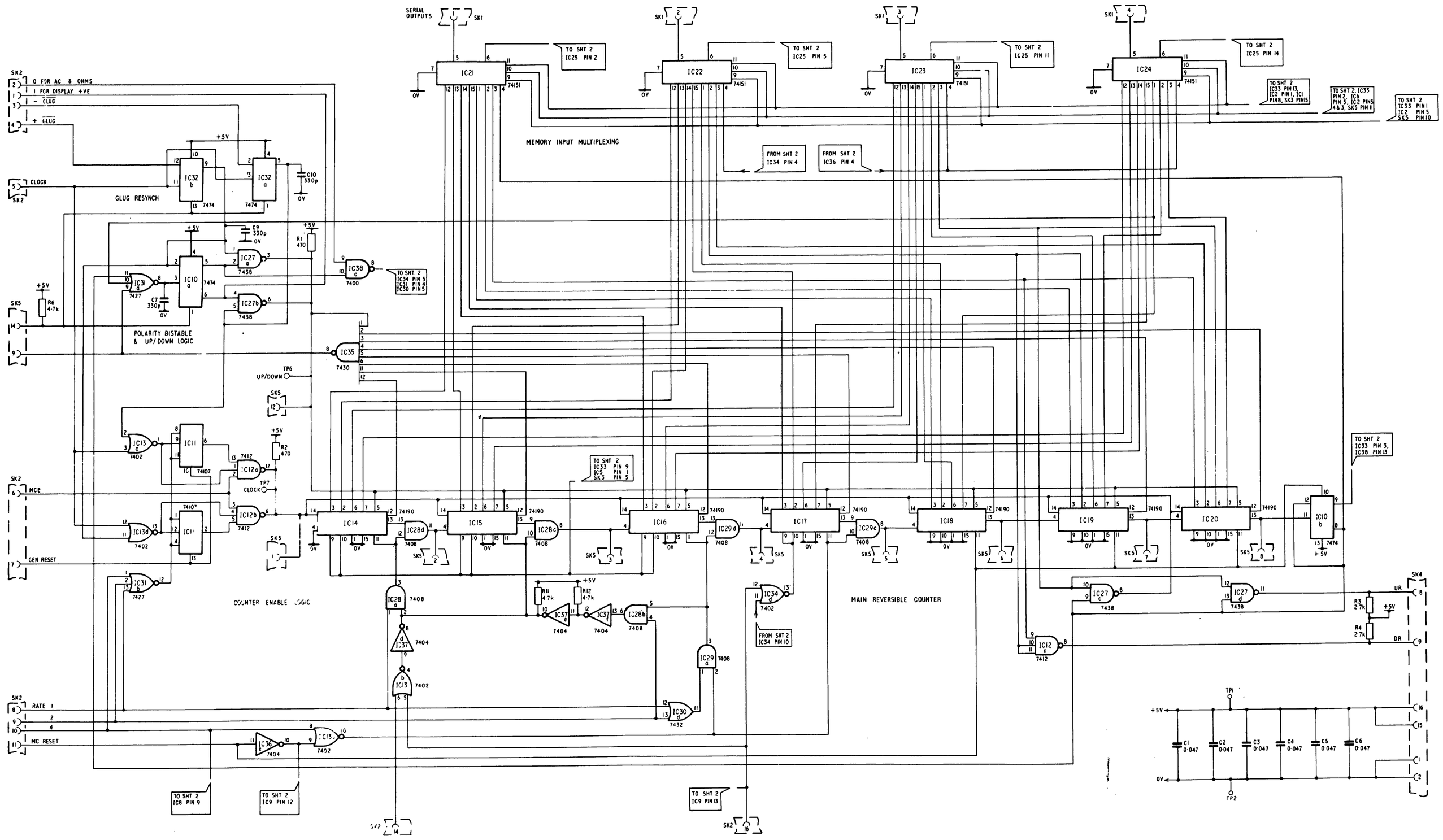
On Diag 7.18 are the Opto-Couplers, Autorange circuits and Display Flashing logic.

THE DISPLAY, DISPLAY DRIVE AND PHASE LOCKED CLOCK

The Display Drive and Phase Locked Clock are illustrated on Diag 7.19. In this sub-section the BCD information is decoded and presented to the display, which has 12 decade windows to enable the visual information to be positioned correctly relative to the fixed decimal point Diag 7.20.



Block Schematic Diag. 7.14



Counters and Memory Diag. 7.15 pcb 4 (sheet 2)

COUNTERS AND MEMORY

GLUG RESYNCH (Diag 7.15)

The output from the A/D converter is a pulse train pair. The pulse trains are labelled + GLUG and – GLUG, and are transferred from the floating circuits via optical couplers. To restore synchronization the signals are gated with Clock in the dual flip-flop IC32. The input to pins 1 and 13 is for test purposes only.

COUNTER ENABLE LOGIC

Provided Main Counter Enable (MCE) SK2 pin 6 is present the resynchronized $\overline{+GLUG}$, $\overline{-GLUG}$ signals are permitted to gate Clock pulses through IC13, IC12 into the counter chain. The indirect path for each half of IC13, via IC11, provides the ÷ 2 function necessary when the instrument is operating at 20ms (4 x 9's) integration time. IC31b inputs all low.

POLARITY BISTABLE & UP/DOWN LOGIC

The direction of count is governed by two factors. Essentially $\overline{+GLUG}$ will drive the counter in one direction, – $\overline{GLUG}$ causing the count to reverse. However, if at any time the counter content is being decremented through zero, gate IC35 will detect underflow and force a reversal via IC31a and IC10a. Thus the effect of the GLUG-lines on pin 5 of each counter element is reversed. The labelled polarity of the inputs at SK2 Pins 3 and 4 is not in itself significant to the direction of count, the counter content at all times being the modulus of the input value irrespective of sign. The need for a minus sign is detected by IC38 Pin 10, and depends on the final state of IC10a. The gate is inhibited in the AC or OHMS mode. The input on SK2 pin 14 blanks decades 6 and 7 (see Fig. 7.1) during STAT period when AC is selected. (Maximum AC mode displayed scale length is 5 x 9's).

MAIN REVERSIBLE COUNTER

IC14 to IC20 plus IC10b form the 7½ decade counter chain, IC20 being the most significant "9" while IC10b can only assume a 1 or 0. The counter operates in BCD, pin 13 of each element providing the "ripple" enable to the next decade. Elements IC17, 16, 15 and 14 are capable of being held at zero by the Rate lines (SK2 Pins 8, 9 and 10) when low, so that unwanted decades are inhibited for the shorter scale lengths. Main Counter Reset ($\overline{MCR}$) generated by the Process Control circuits, provides the zero resetting on pin 11 of the counter elements at the end of each conversion.

SCALE LENGTH

For operation as a 7 x 9's instrument the complete counter is used. The coded inputs on SK2 pins 8, 9 and 10 are decoded to provide progressive inhibition of the least significant decades as the Integration time is changed. (Pin 11 set low on each IC in turn). This is illustrated in the following table:-

RATE	SCALE LENGTH	COUNTER ELEMENTS INHIBITED
10s	7 x 9's	–
1s	6 x 9's	IC14
100ms	5 x 9's	IC14, IC15
20ms	4 x 9's	IC14, IC15, IC16
1ms	3 x 9's	IC14, IC15, IC16, IC17

◄——— **Diag. 7.15**

MEMORY INPUT MULTIPLEXING

Parallel to Serial Conversion is performed by IC's 21 to 24 inclusive. The outputs on Pin 6 of each being determined by the state of the select lines feeding pins 9, 10 and 11 of each converter element. The counter content is fed in serial BCD form to the data selector (IC25) on Diag 7.16

DATA SELECTOR (Diag 7.16)

IC25 a 4 x 2 line-to-1 line data selector completes the multiplexing of the Counter data into the Random Access Memory (RAM).

Control of the selector is the clock ÷ 128 output from IC2 which when low selects the counter data and when high selects the organisational data. Memory load addresses are generated by the range counter code from pcb3, fed in on SK3 pins 9, 10, 11 and 12 via IC5 when STAT is high (SK3 pin 5). The output from IC33 pin 8 determines the operation of the "RAM". When low, memory load occurs. When high, Read is selected. The 16 load pulses (during STAT) are derived from the timing counter and phased with the 16 selected input words.

DISPLAY SECONDARY ORGANISATION

The function of these elements (IC's 29, 30, 31, 33, 34, 36 and 38) is to test for certain conditions which determine what type of secondary display is necessary.

The conditions tested are:-

1) Address of word to be loaded - display digit.
2) The presence or absence of a 1 as the most significant measurement digit.
3) The operation on 3 x 9's scale length (10mΩ range) – trailing zero restoration.
4) The need for a minus sign.
5) The need for extra leading zeros in certain cases – low ranges.
6) Autorange mode – affects leading zero blanking and minus sign.

The display calls for the generation of 16 words of data, of which 12 are actually visible display information. The words are presented in two groups of 8, the first group being derived from the counter chain BCD data. The second, being generated from the Display Secondary Organisation, fills in the gaps, as it were generating all the necessary blanks and extra zero's required and in some instances, a minus sign. For convenience in the explanatory text which follows, the display windows are identified by the numbers 0 to 11, reading from left to right.

DISPLAY WINDOWS

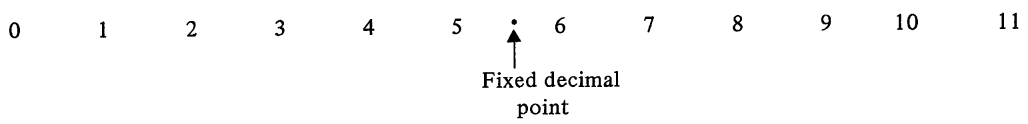


Fig 7.1

MINUS SIGN

The need for a minus sign is detected in the Polarity Bistable on Diag 7.15. This is applied as a low on pin 5 of IC34 (Diag 7.16). The second input to IC34 will be low if IC33b inputs are all high, i.e. Autorange is true, the msd of the measurement data is a zero and the word being scanned is not that for display windows 5, 6 or 7. This would normally generate a 'blank required' signal on IC36 pin 4, but the presence of a 'minus sign required' signal on IC34 pin 4 will override the blank. This also determines whether a zero, blank or –ve sign is displayed before the most significant 9.

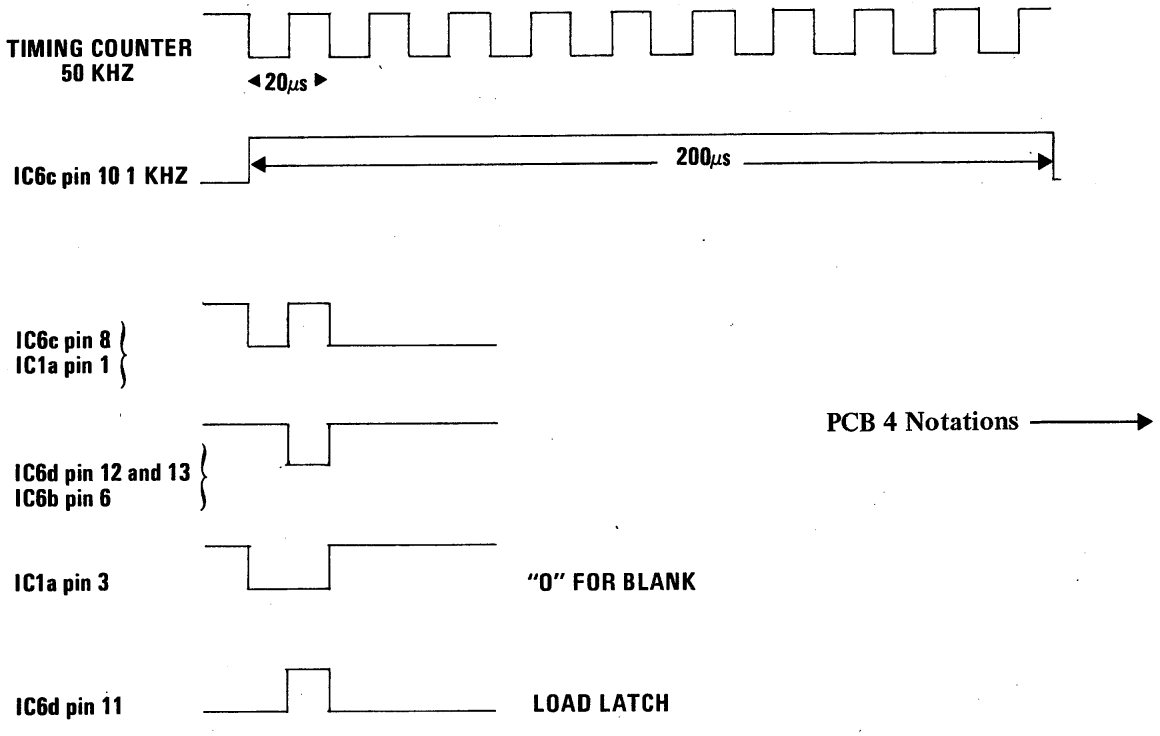
If the m.s.d. of the measurement data is not zero but 1, the minus sign for a negative quantity is normally needed one place further left than the previously described case. The element involved is IC29b whose output will be high. Additionally the memory address being loaded is address 7 i.e. the last to be loaded of secondary organisation. The high on pin 6 of IC29b will set IC25 output pins all low, which will cause the memory to output 1.1.1.1., which is the minus sign code.

There is a further special case requiring a secondary organisation minus sign, necessitated by the convention of preceding a fractional number with a zero before the decimal point. The display organisation normally inserts a minus sign before the m.s.d. of the displayed value, which for the 100mV and 10mV ranges would be position 5 or 6. Since this would result in, for example, (on the 100mV range), a display of "−.414", it is necessary to force a zero into position 5 and re-insert the minus sign in position 4. IC38 pin 3 goes low when position 4 word is being scanned enabling IC30 pin 4 to allow a minus sign if required, to force IC25 pin 6 to a low. Similar logic determines the position of Blanks in the display entered by the inverted codes on IC25 pins 13 and 10.

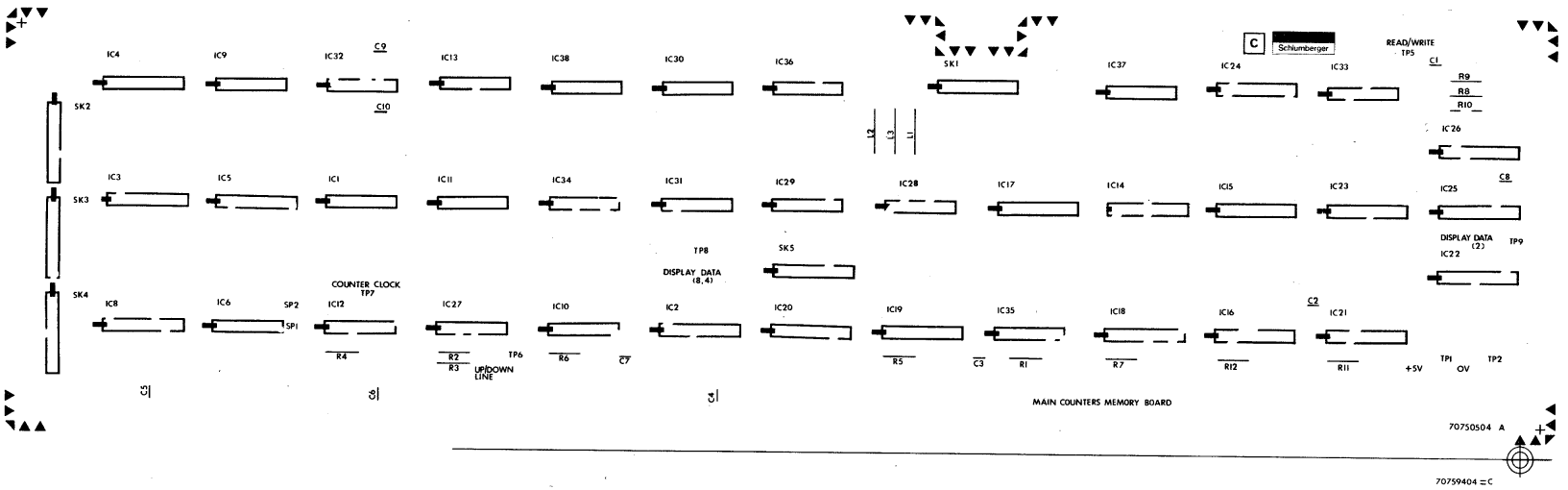
When the instrument is operating on the 10MΩ range at the 3 x 9's scale length, the input on IC34d pin 11 in conjunction with STAT from pcb 3 forces IC17 to register a zero for display in the decade window immediately preceding the decimal point i.e. position 5.

MEMORY DISPLAY MODE

The data previously loaded into memory are output to the display circuits under the control of the display scanner (IC1). The timing counter 50kHz output is gated via IC6b (pin 6) with a 1kHz pulse train, both pulse trains derived from the timing counter divider stages, the resulting gate pulse on IC6c pin 8 is used to enable the scanner (the address lines being pins 3, 4, 5, 6) accessing the two "words" needed for the digit pair to be displayed. The scan is such that no two digit pairs are ever addressed in sequence (bits 8 and 2 being transposed for this purpose) IC6d pin 11, the inverse of IC6b pin 6 is used as a load latch for the righthand digits in the display drive circuit. When they are being latched, the selected display element pair is blanked by the low on IC1a pin 3 via SK3 pin 8.

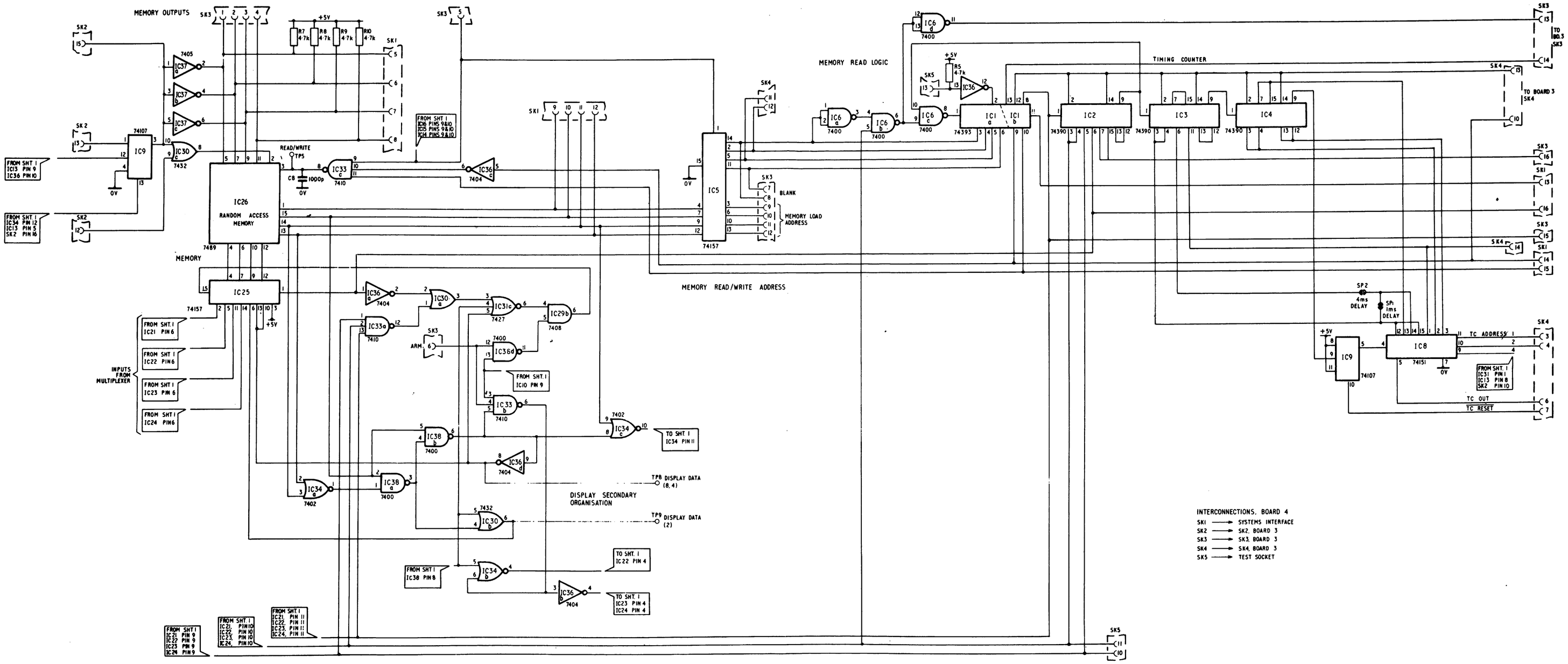


MEMORY DISPLAY MODE

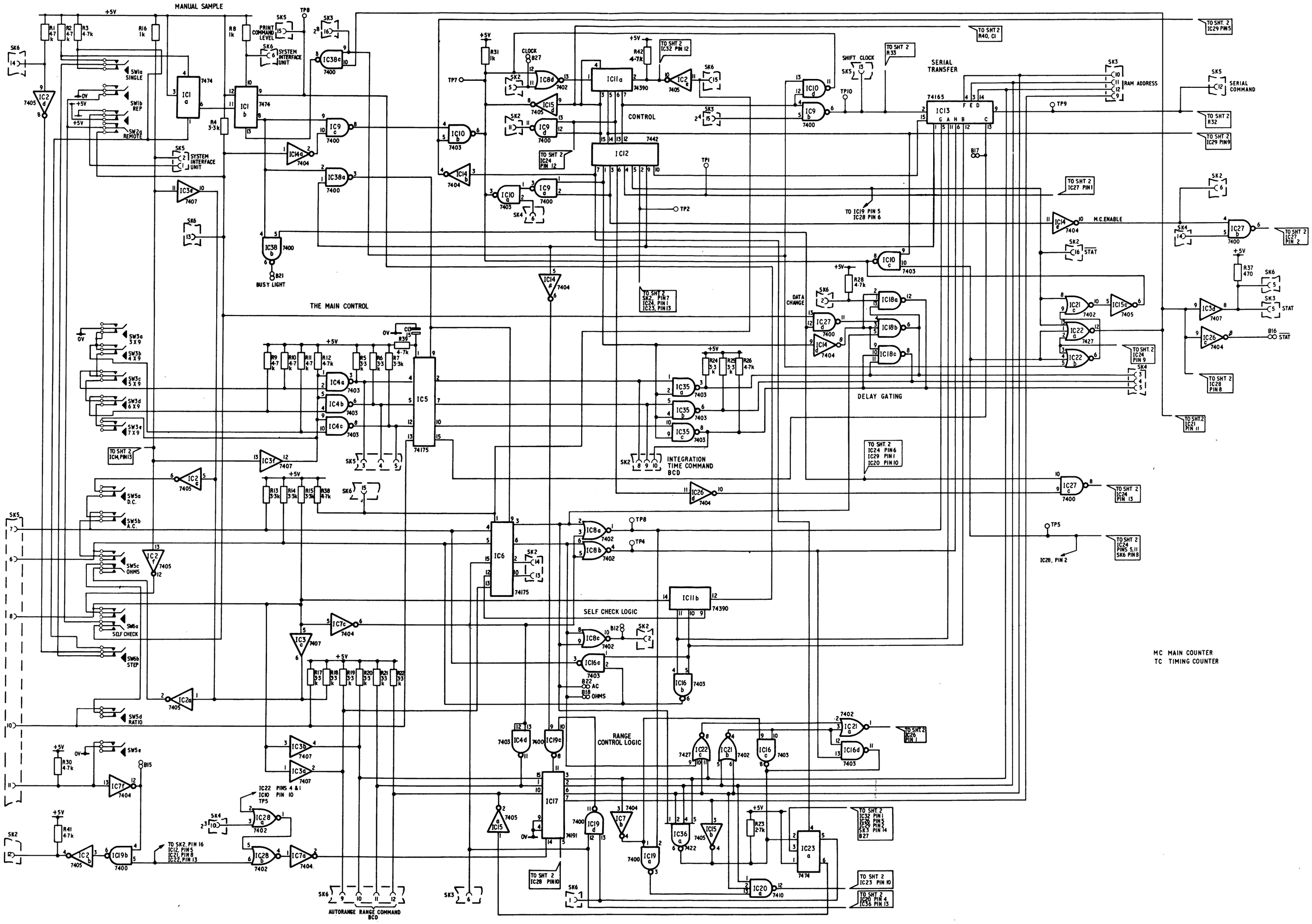


PCB 4 Notations

JWW/7075/4



Counters and Memory Diag. 7.16 pcb 4 (sheet 1)



Control Board Diag. 7.17 pcb 3 (sheet 1)

CONTROL LOGIC (Diag. 7.17, 7.18)

IC11a is the "state" counter, decoded into the 10 states by IC12. At anytime one of the10 outputs of IC12 will be low.

The states, advanced by a low at TP7 synchronously with the 1.6MHz clock are tabulated below, and described in sequence, starting at state ⑤ , the state that accepts a digitise command.

7075 CONTROL SEQUENCE

CODE		ACTION	IC12 PIN No.	TERMINATED BY
6	0110	HOLD – waits for Dig Command unless "not-in-Remote", overload or in Rep.	7	(i) CLOCK (in Rep) (ii) Overload (on Autorange) (iii) Dig Command
7	0111	LOAD – Integration & Mode latches. Range counter if not in Autorange serial transfer Shift Register	9	CLOCK
8	1000	SERIAL TRANSFER (Floating & Fan-out)	10	TIMING COUNTER
9	1001	(Not Used)	11	CLOCK
0	0000	DELAY PERIOD before Measurement Start	1	TIMING COUNTER
1	0001	RESET Autorange ccts & ÷ 2 bistable on Bd. 4	2	CLOCK
2	0010	MEASUREMENT PERIOD	3	TIMING COUNTER
3	0011	PULSE BEFORE STAT – Samples down-range system	4	CLOCK
4	0100	STAT – Memory Write Sequence Resets Dig Command & Print Command Autorange counter reset	5	TIMING COUNTER OR CLOCK (if autoranging)
5	0101	PULSE AFTER STAT – resets Main Counter resets "O/L during HOLD" bistable	6	CLOCK

OPERATION

State ⑤

State ⑥ enables IC10b pin 5. IC10b pin 4 will go high, putting a low on TP7 to advance control for a low on either IC9d pin 9 or 10. If in "REP" IC14a pin 1 will be high making IC9c pin 10 low and control will advance to state ⑦ on next clock. If in "SINGLE" sample IC14a pin 1 will be low. The system is therefore waiting for a low on IC1b pin 8 from either a remotely commanded digitise command on IC1b pin 10 or a front panel command via the anti-bounce latch IC1a from the single sample switch.

State ⑥ can also be advanced by an overload signal via IC10c – see autorange system.
State ⑥ resets range error bistable IC23a.

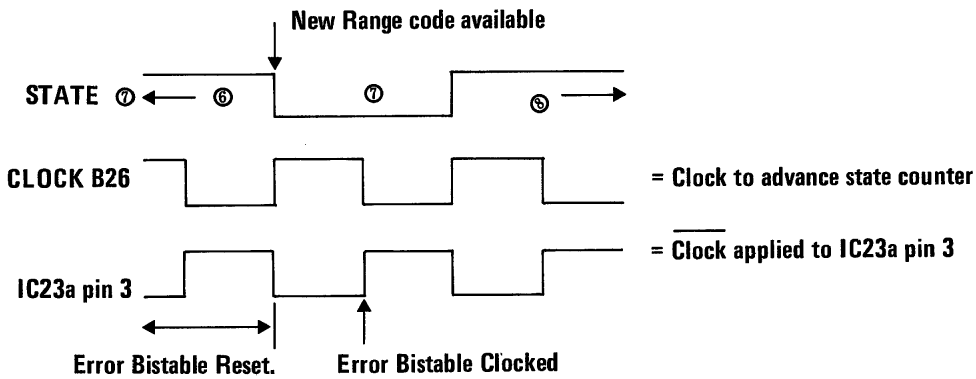
◀——— Diag. 7.17

State ⑦

Integration and Mode latches (IC5 and IC6) are loaded. If in remote these latches are already loaded via IC38a pin 2.

IC17 the range counter is loaded via IC19c pin 9 if IC19d pin 12 or IC19d pin 13 is low. IC19d pin 12 will be low if not in Autorange. IC19d pin 13 will be low if the error bistable detects an incorrect range code, putting a low on IC23a pin 5 when clocked, which corrects and resets the range counter.

When state ⑦ ends the shift register IC13 will be loaded (IC13 pin 1) with the final range and mode information. As it is an odd state (IC11a pin 3 = high) it is terminated by clock via IC15d holding TP7 low. Also it will have reset the Timing Counter via IC7d, e, and the measurement counter via IC9d.

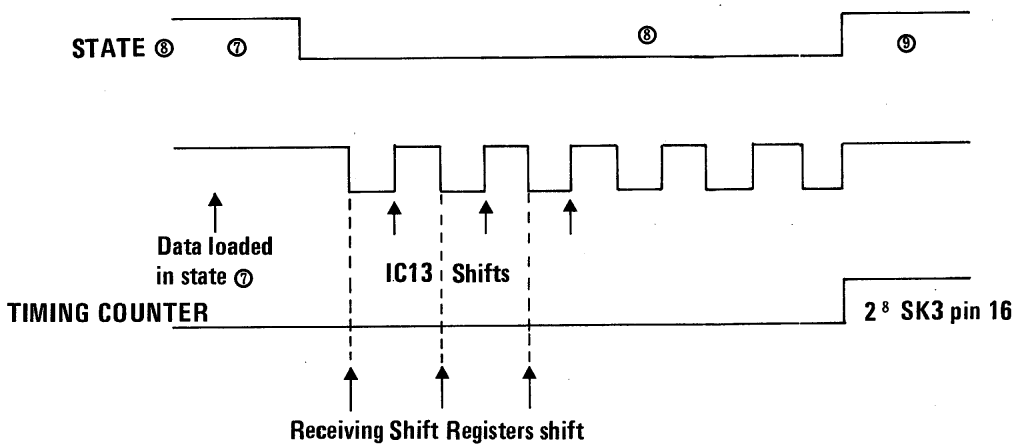


State ⑧

IC13 is now ready to transfer its information to the floating logic on board 6 via the opto-couplers IC30 and IC31 and to the systems interface unit (S.I.U.) if fitted.

IC11 pin 7 is high enabling IC9b to pass strobe pulses on SK3 pin 15 (from the 4TH output) down the timing counter chain (2^4) to the clock input; to the shift registers IC13; via SK5 pin 13 to the receiving shift register in the S.I.U. and via opto-coupler IC31 to the floating logic. IC13 pin 2 is enabled by IC12 pin 10 being at a low, and shifts on the positive edges. The receiving shift registers are arranged to shift on the negative edges to allow for data settling time.

This state is terminated by a high from the 8th output of the timing counter arriving at SK3 pin 16 enabling gate IC10d, (already enabled by IC11a pin 7), putting a low on TP7 to advance IC11a on the next clock edge.



CONTROL BOARD WAVEFORMS

State ⑨

State ⑨ is not used, clocked to state ⓪ as it is an odd state.

State ⓪

This state lasts for the time needed for analogue settling before a measurement starts. The required delays are normally 20ms unless:-

1) SIU determines no command changes since the last measurement, in which case it puts a low on IC18a pin 1 requesting a 4ms delay only.

2) AC mode and Single measurements or Autorange change – 800ms delay.

Operation 2) has priority over 1).

IC35a, b and c is disabled by state ⑧ (IC12 pin 1 low). Codes set up on SK4 pins 3, 4 and 5 by IC18a, b and c and IC27a address the output of the Timing Counter, which will go high after the required delay. This is applied to SK4 pin 6 which enables gate IC10a already set up by state ⑤ to put a low on TP7 to advance IC11a.

Codes to Timing Counter:-

	SK4/ 3	4	5
20ms	1	1	0
800ms	0	1	1
4ms	1	0	1

State ①

Resets autorange bistables IC24a, IC23b
Resets ÷ 2 bistable for 4 x 9's rate.
Resets Timing Counter via IC7d and e.
Terminated by clock as odd state.

State ②

This is the measurement period. The code for the required integration time is held in IC5 and applied to the timing counter via IC35a, b, c and SK4 pins 3, 4 and 5.

The Codes are:-

	SK4/ 3	4	5
1ms (3 x 9's)	1	1	1
20ms (4 x 9's)	1	1	0
100ms (5 x 9's)	0	1	0
1s (6 x 9's)	1	0	0
10s (7 x 9's)	0	0	0

Similar codes on SK2 pins 8, 9 and 10 select the required measurement counter length. The codes are either encoded from the front panel switches SW3a to SW3e or from the S.I.U. via SK5 pins 3, 4 and 5. In the latter case IC4 a. b. and c. are disabled by SK5 pin 2 via IC3f.

This state will be terminated by either:-

1) The "time-up" signal on SK4 pin 6 from the timing counter. IC10a enabled by state ② via IC9a
or
2) By an autorange decision via IC10c enabled by state ② or ⑥ by IC11a pin 5. (See Autoranging).

State ③

This is an odd state and so if resets the timing counter ready for state ④ . It also samples the autoranging system for a "slow-down" range decision in case this has not already been made during state ② (see autoranging).

State ④

Memory is loaded with display data measurement and status information during state ④ and the same data is sent to the S.I.U. via SK1 pins 5, 6, 7 and 8. It is normally terminated by the timing counter 8th output on SK3 pin 16 via IC22b, IC21c and IC15c, putting a low on TP7 to advance IC11a on the next clock edge.

It may be by-passed by the autoranging system placing a high on IC22b pin 4 which will inhibit STAT on IC22a pin 12 and advance IC11a immediately on the next clock pulse.

STAT normally lasts for 80μs during which time there are 16 pulses on SK4 pin 10, the 2nd output of the timing counter. These, clock the binary counter through its 16 states, starting and finishing on the same range code. The range counter is reversible and the direction is determined by IC17 pin 5. This is held low (count up) by IC28c pin 10 since IC28c pin 8, is high (STAT).

If state ④ is being by-passed by the autoranging system, IC28c pin 8 is held low by IC22a pin 1 at a high. Instead of 16 pulses there is now only one. IC28b pin 6 is low (IC12 pin 5 low in state ④). IC28a pin 2 is high and blocked, so as state ④ passes there is one pulse on IC28b pin 4 which is delivered to IC17 pin 14. This changes the range code. Clock input to IC17 while high during state ④ ensures correct direction of count.

State ⑤

Resets measurement latch via IC9d.
Resets timing counter via IC7d and e.
Resets latch in autoranging system.
Terminated by clock (odd state).

State ⑥

As before.

AUTORANGING SYSTEM

IC32a, 33a and 33b are the autorange counters. Should the presence of either GLUG (IC38 pin 13 or 12 low) occur during state ② and state ⑥ IC11a pin 5 gates IC29c pin 9 enabling the autorange counters. They are reset at all other times.

During a GLUG there will be at least one transition of output (IC33a pin 9) if the GLUG is larger than the size of GLUG corresponding to the down range point.

For a steady DC input voltage to the analogue system there will be at least one GLUG larger than the critical size if the input value is greater than the down range value. This incident will clock IC23b and prevent a down range decision (see later).

Similarly for an input greater than the up range value, there will be at least one transition of output IC33b pin 11 with IC33a pin 9. This will pass through IC35d, IC26 pins 3 and 4 and IC36b pin 12 to clock IC24a, the main autorange bistable. In both cases the information is OR-ed with information from the measurement counter on board 4. Should the measurement count exceed the up range value SK4 pin 8 will go low at least once. Should the measurement count exceed the down range value SK4 pin 9 will go low at least once.

The system will therefore up-range if:-

1) Any GLUG exceeds the size equivalent to that obtained with a steady input equal to the up range value.

2) The top range for the mode has not been reached.

3) Autorange is enabled.

The system will down-range if:-

1) During the measurement or the first 20ms there are no GLUGS greater than those obtained by a steady input at the down-range point.

2) It is not already on the bottom range.

3) It is in the autorange mode.

IC24a and IC23b (the autorange and down range bistables) are reset before a measurement starts on state ① . If during a measurement, the main reversible counter output or a GLUG greater than the down range value occurs, IC15e pin 10 will go low. This will clock IC23b to prevent down ranging on the next clock IC29a pin 2, if IC24a is not already set (IC29c pin 9). If on the bottom range IC23b will be set anyway (IC23b pin 10).

The down-range bistable will be sampled by either the 20ms output from the timing counter IC26b pin 6, or state ③ (IC27a pin 1), by IC20b pin 3 to set the main bistable IC24a if autorange is true (IC20b pin 4) to start an autoranging sequence. IC24a will terminate state ② or state ⑤ if not already finished, inhibit state ④ , and increment the range counter by one during the passing of state ④ in the direction determined by IC28c pin 10. As STAT is inhibited (IC28c pin 8) the direction will be determined by whether IC23b had been clocked or not (i.e. if not clocked – down range).

An overload signal from the GLUG counter or the main counter will clock IC24a directly (providing IC23b had already been clocked up-range). State ② and ⑥ will be terminated immediately. To do this Autorange must be true (IC36b pin 13) and the top range must not have been reached (IC26a pin 1).

If an overload occurs while in state ⑥ and the system is not in remote, the main autorange bistable (IC24a) will terminate state ⑥ (subject to the usual conditions. i.e. Autorange must be true and not on the top range) and start a measurement cycle. A normal upranging sequence will follow. IC24b inhibits STAT and Print Command until the autoranging is complete. It is reset on state ⑤ if the main autorange bistable is reset.

IC27c on pcb 4 detects a count of "14" which is the range overload point, the output on SK4 pin 8 causing up-range to be actioned on pcb 3. The other output (IC27c pin 8) locks-out the clock at full scale "freezing" the counter action.

IC12c also on pcb 4 detects the "12" condition producing down-range at SK4 pin 9. Down range automatically occurs every conversion or 20ms after conversion start whichever is the shorter time, unless during that time it is inhibited by the output from IC12c.

FLASHING LOGIC

Under normal conditions IC29e and IC20c latch is reset. IC29e pin 13 detects analogue overload, IC29e, and IC20c latch. IC32b pin 8 produces a 12.5Hz pulse train which resets the latch while low causing the display to "flash" for as long as the overload persists.

To prevent flashing during auto/normal range change, a low is applied via IC20c pin 10.

To ensure that invalid readings are not displayed during memory update, a blanking pulse is applied to B16 which inhibits IC12 and IC11.

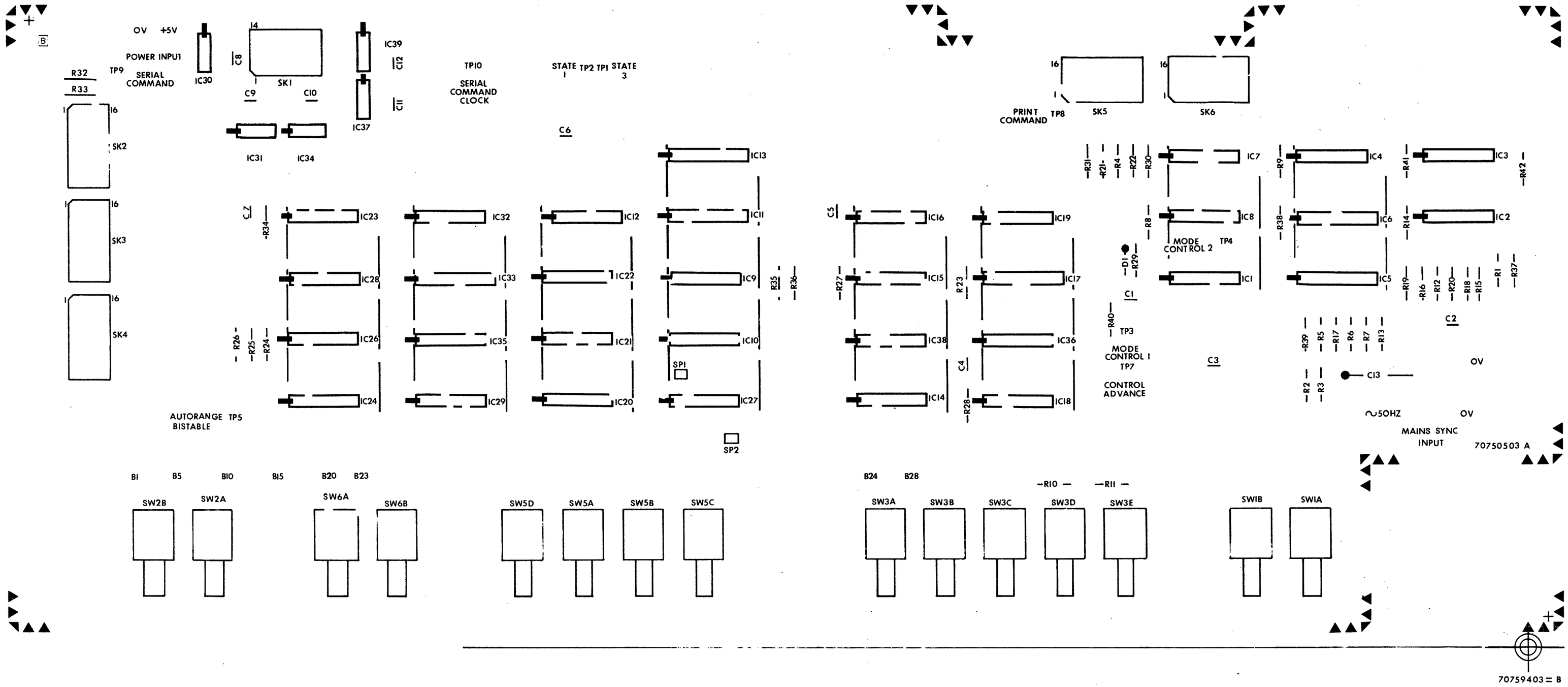
SELF CHECK LOGIC

In the instrument self check mode, the OHMS, AC and DC front panel switches are disabled (IC2f, IC2c and IC3e). Autorange is also disabled via IC3a. IC17 is set via IC3b, by range code 0 1 1. S.I.U. and fan-out are informed from IC8a pin 1 and IC8b pin 4 via IC13 pins 5 and 6. Self check codes are also sent via IC13 pin 11 and 12. The appropriate self check codes are then formed for each test.

The information displayed during the self check of the instrument through its 5 sequential steps is given in section 2.

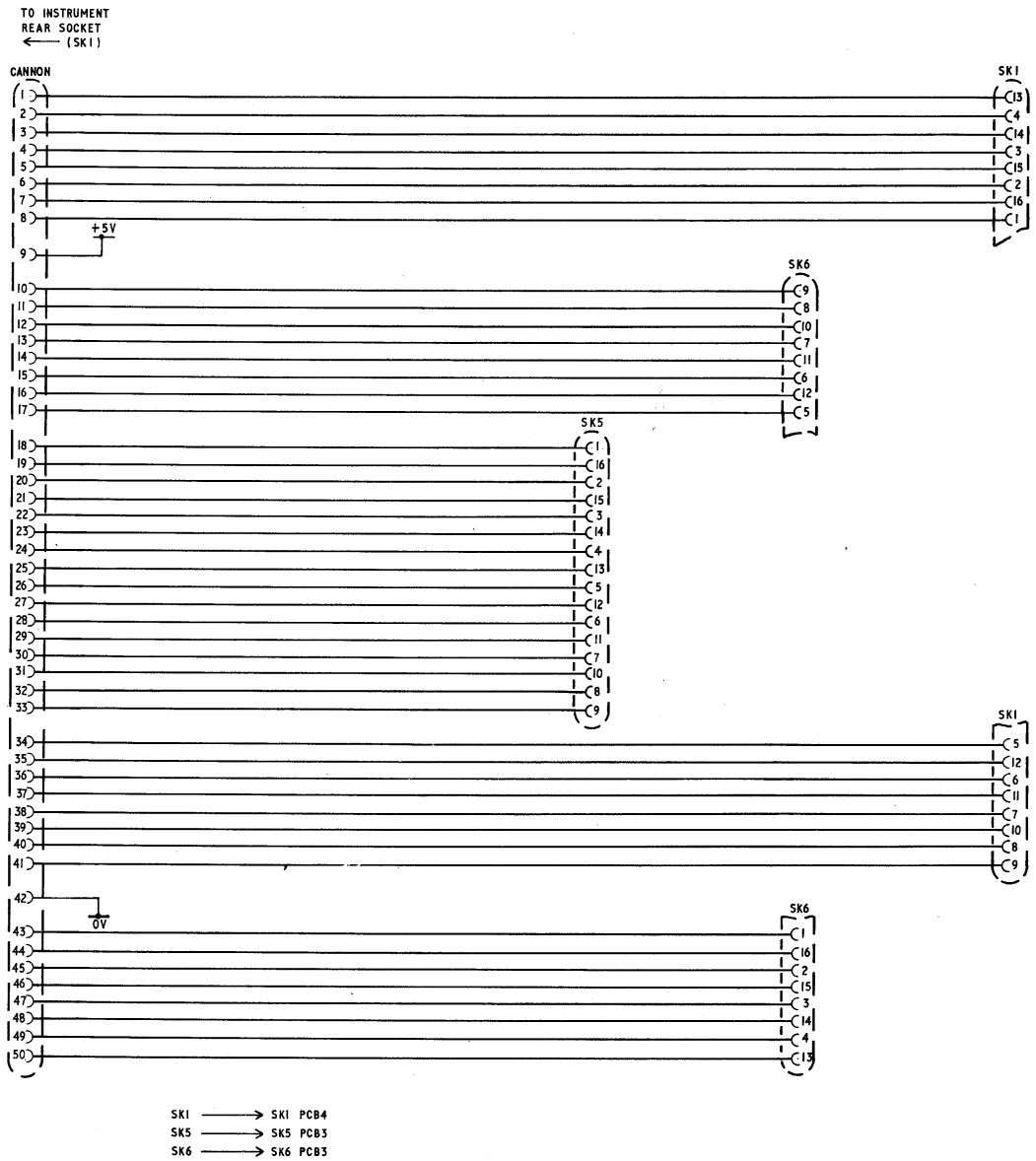
PCB 11

Enables the rear panel socket SK1 for instrument use with ATE in a systems environment.



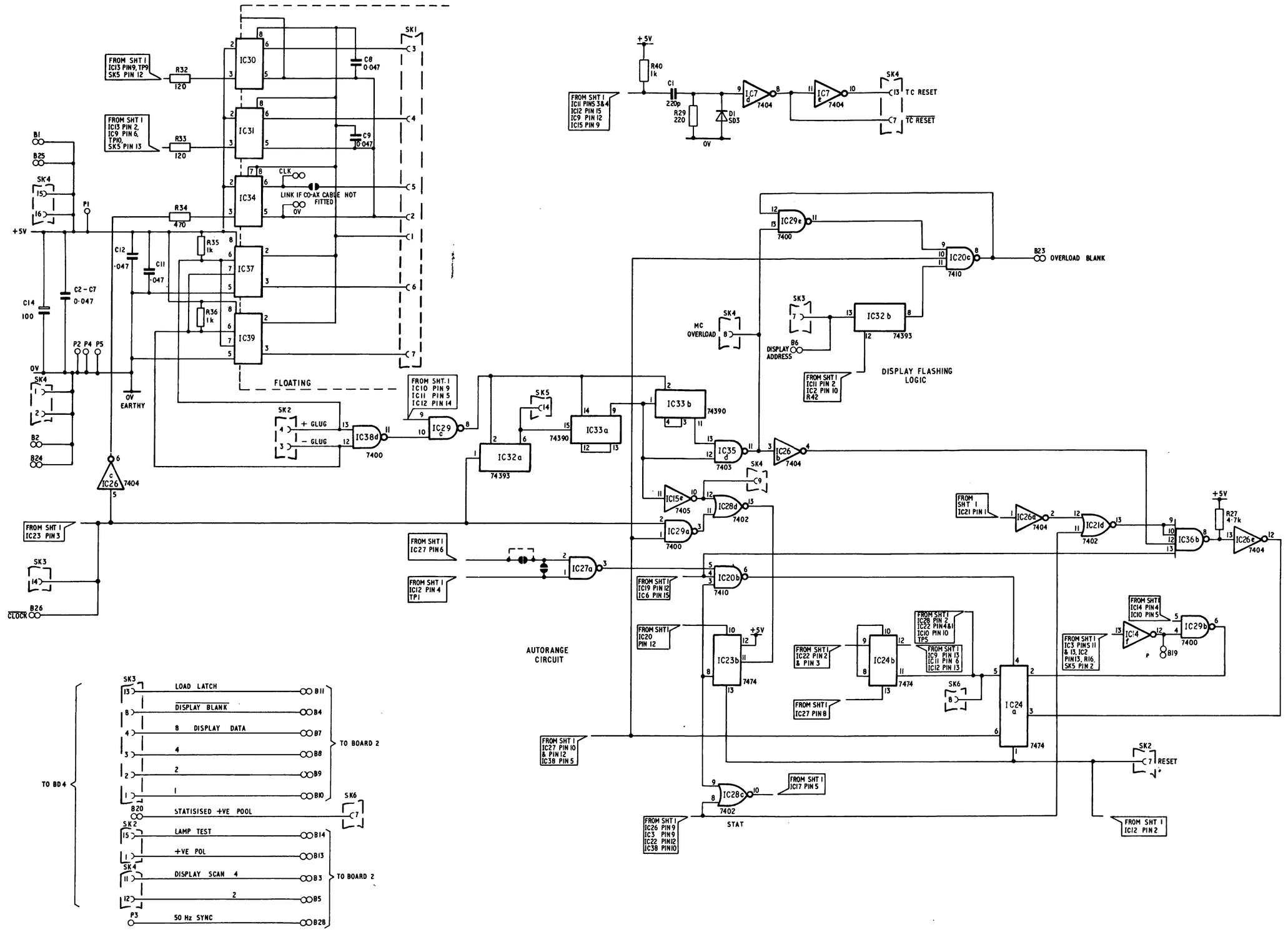
PCB 3 Notations

PCB 11 Interconnections →

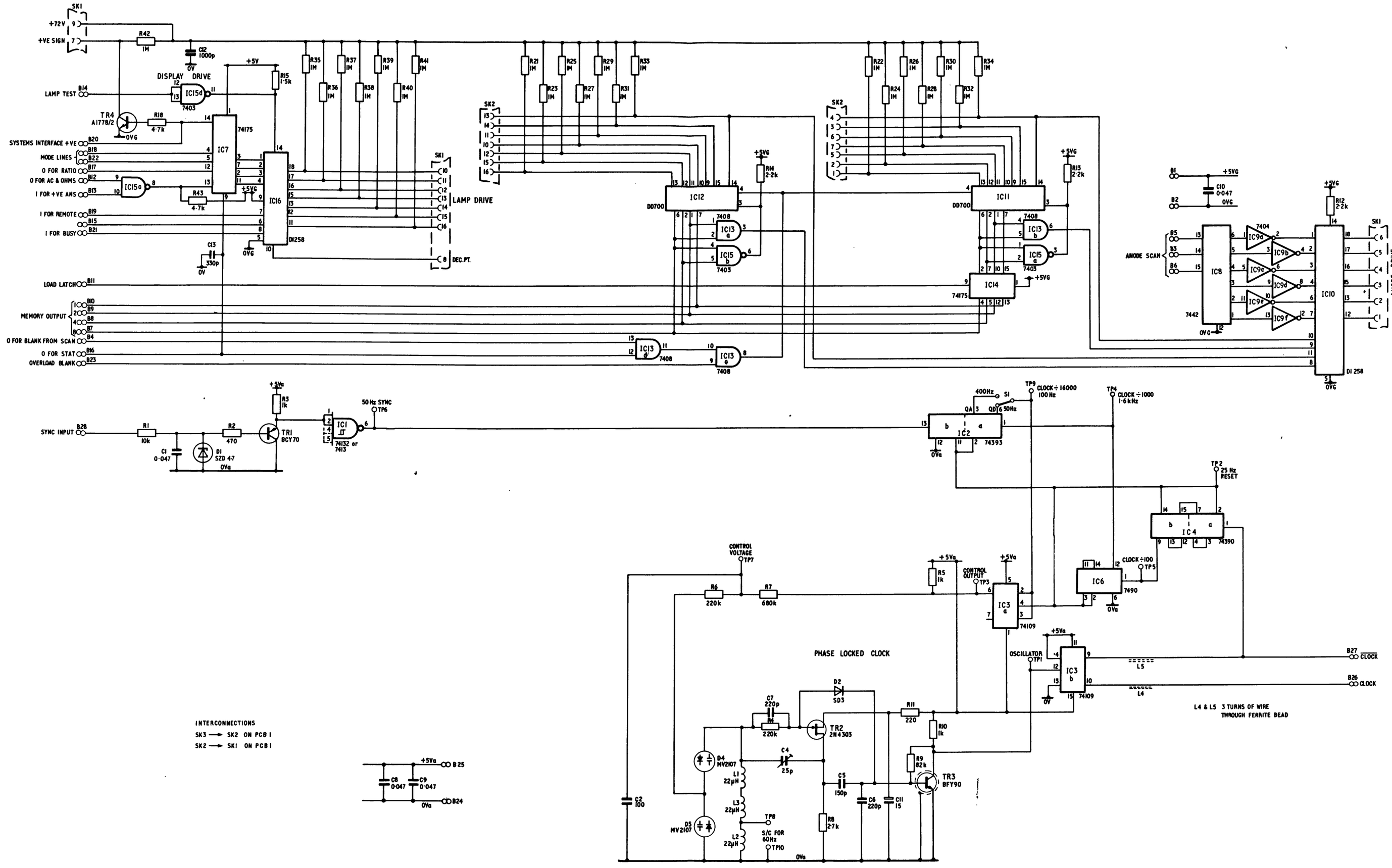


DVM TO S.I.U. INTERCONNECTION BOARD

PCB 11 Interconnections



Control Board Diag. 7.18 pcb 3 (sheet 2)



Display Drive and Phase Locked Clock Diag. 7.19 pcb 2

THE DISPLAY, DISPLAY DRIVE AND PHASE LOCKED CLOCK

PHASE LOCKED CLOCK (Diag 7.19)

A mains derived synchronising signal is shaped by R_1, C_1, D_1, and buffered by TR1 before being applied to IC1. The output from this gate is a repeatable, free from bounce, 50Hz signal but possibly of unequal mark-space ratio. IC2 divides this signal by 2 giving a 25Hz output (TP2) with an equal mark-space ratio.

The voltage controlled clock oscillator is phase locked to the mains frequency. Voltage to frequency adjustment is achieved by C4. For 50Hz operation with a control voltage of 2.2V, frequency should be 3.2 MHz. For 60Hz (TP8 connected to TP10) operation and a control voltage of 2.2V, frequency should be 3.84MHz. Frequency control is by varactor diodes D4 and D5.

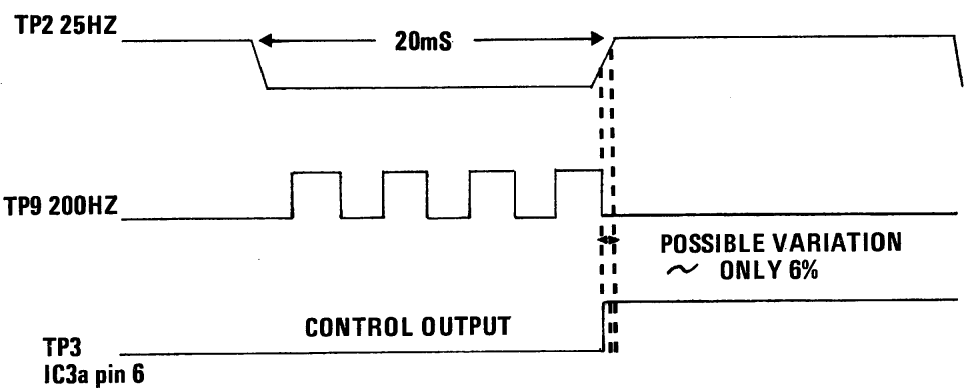
TR3 acts as a buffer, its output (TP1) is applied to the counter chain, the final output of which is 200Hz.

OPERATION

When the level of the synchronising signal (TP2) is high, the counter is held in reset; when it goes low, the chain is enabled. As it returns to the high state, IC3a is clocked and the state of the final 200Hz output is stored until the next cycle. Should the final 200Hz output be high at this instant, the clock is running too slow. Should it be low, the clock is running too fast.

A high on the control voltage tends to reduce the capacitance of D4 and D5 thereby increasing the clock frequency and vice versa. Because the possible error in frequency is 6% maximum, there is no likelihood of sampling the wrong output pulse.

The control voltage is averaged and smoothed by R7, C2 so that a gradual control is achieved. In lock the decision tends to alternate on consecutive samples giving a small slow ramping of the clock frequency. The effect of one decision is arranged to be very small, therefore the extent of the final jitter is also very small.



PHASE LOCKED CLOCK

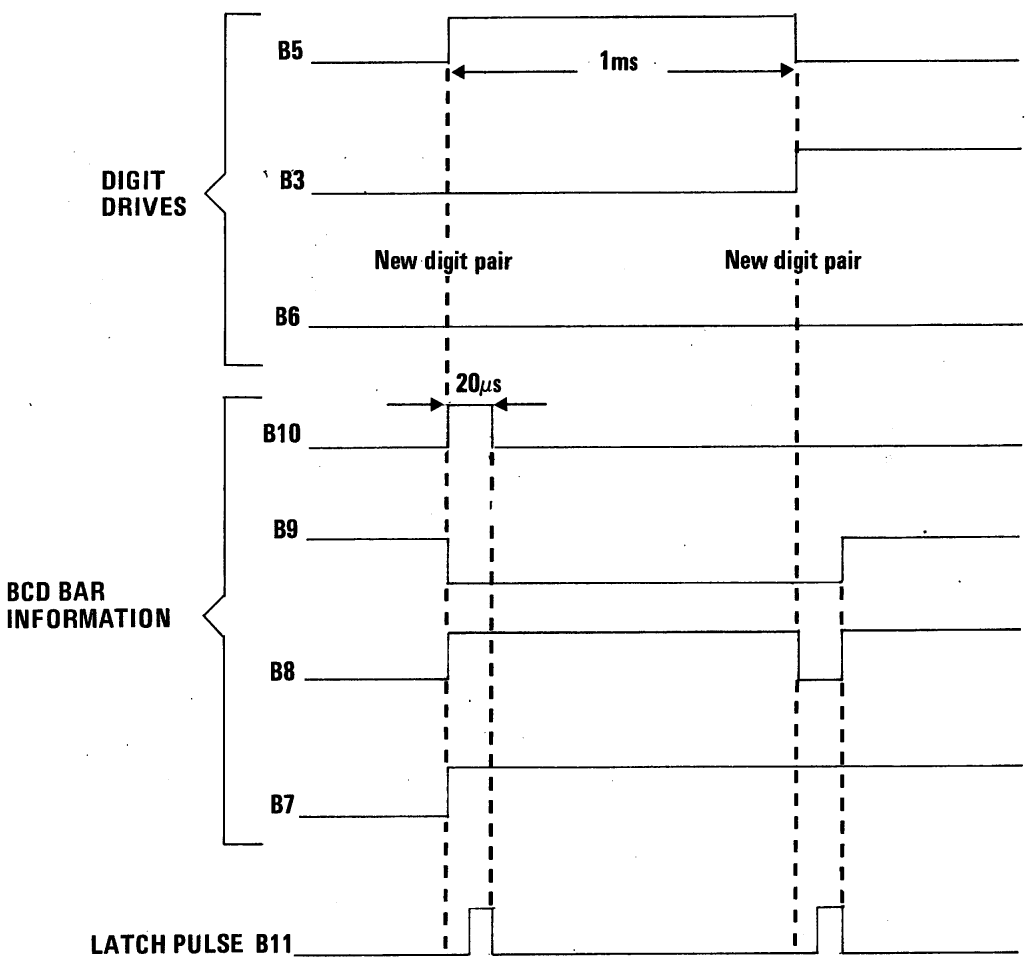
◄——— Diag. 7.19

THE DISPLAY DRIVE

The display is multiplexed, two digits at a time on a 1 in 8 duty cycle. Digit pairs are selected by the BCD information on B5, B3 and B6, decoded by IC8 and level shifted by IC10 to the anode switches on the display board.

For each new digit pair addressed, two sets of 7 bar information are required. These appear, in BCD, on B10, B9, B8 and B7. One set of information is applied for 20μs and stored in IC14, gated by a latch pulse on B11, thence decoded by IC11, IC13b and IC15a (special codes) to drive the left hand digits.

The second set of information is applied for the remainder of the multiplex period, decoded by IC12, IC13a and IC15b driving the right hand digits.



DISPLAY DRIVE WAVEFORMS

The BCD codes are:-

Character	BCD	
0 TO 9	0 TO 9	
A	1 0 1 0	NOT USED
B	1 0 1 1	
BLANK	1 1 0 0	Generated by IC15a
	1 1 0 1	Generated by IC15b
NEGATIVE SIGN	1 1 1 0	Generated by IC13a
	1 1 1 1	Generated by IC13b

R13 and R14 program the current drive to the segments of the display. R21 to R34 clamp the unlit segments to the 75V rail.

When the information for the left hand digit is being accessed, the selected display element pair is blanked by a low applied to B4 which inhibits IC12 and IC11 for 20μs.

ANNUNCIATOR DRIVES

Information for the annunciators appears on B20, 18, 22, 17, 12, 13, 19, 15 and 21. Some lines are latched in IC7 before being applied to IC16 (level shifter). R15 programs the current drive to all the neon annunciators. A high input on B14 removes this program current and blanks the annunciators on lamp test.

Unlit annunciators are clamped to the 75V rail by R35 to R41 to ensure that leakage currents do not cause faint discharges.

THE DISPLAY (Diag 7.20)

An 11 x 9's display is used to facilitate a 7 x 9's scale length in conjunction with the fixed decimal point.

The display decades are 7 bar co-planar gas discharge type.

ANNUNCIATOR DISPLAY

V5 to V10 provide the following annunciator displays:- VOLTS, kΩ, BUSY, REMOTE, RATIO and AC.

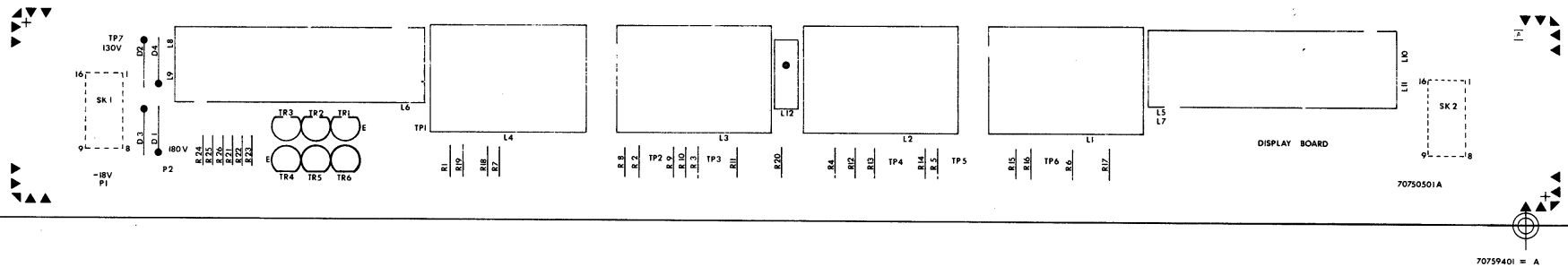
The travelling minus sign is derived from the centre segment of each display element, the positive annunciator is not used.

The VOLTS, kΩ, REMOTE, RATIO and AC annunciators are illuminated on selection of the appropriate function or control button.

The BUSY annunicator is illuminated during range change and on overload. When this occurs, the readings should be regarded as invalid. The annunciator is extinguished when the new range is settled upon, when the new result is displayed, and/or when the overload is removed.

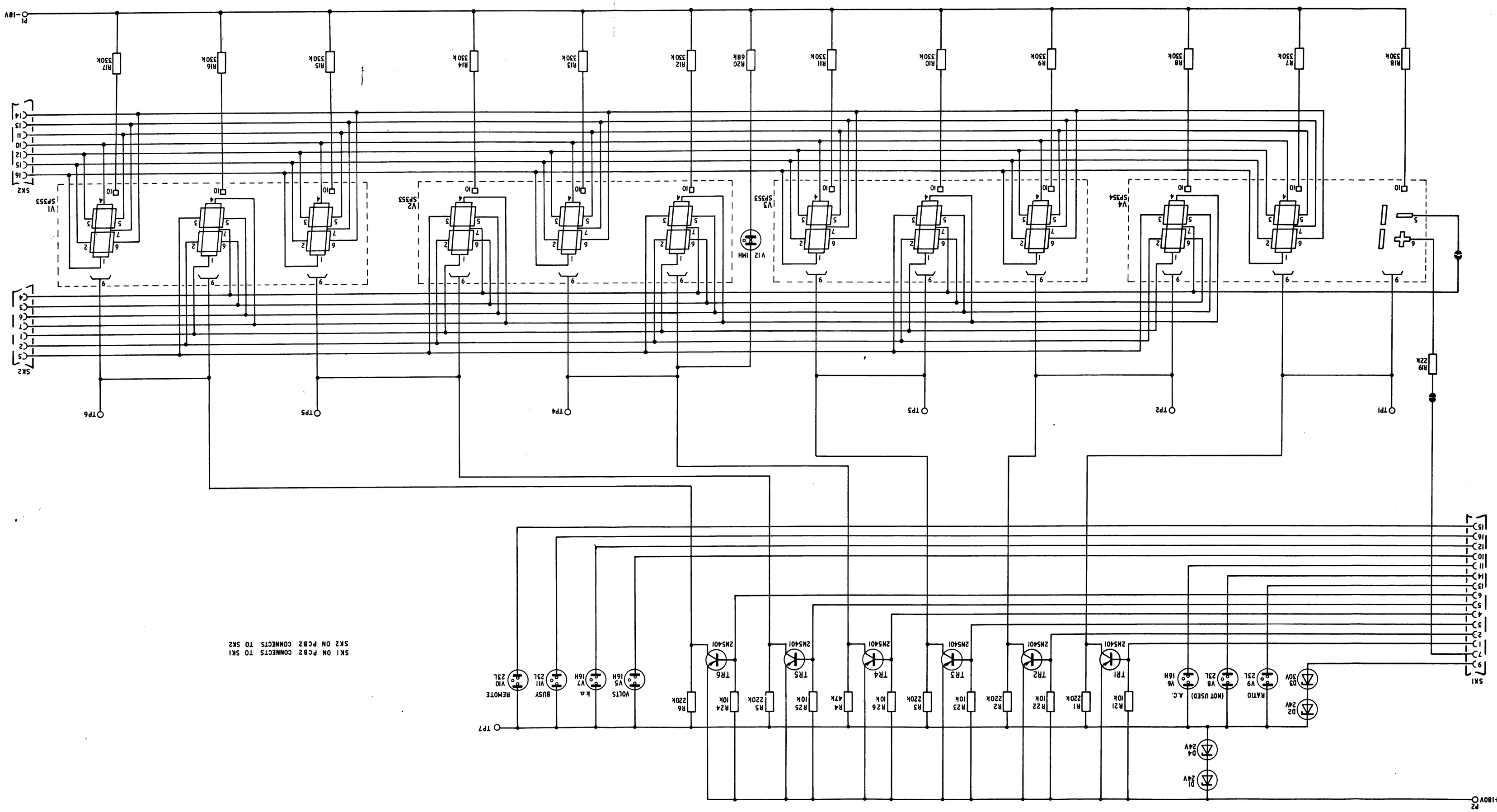
The BUSY signal has the additional function of inhibiting the front panel push buttons, thus once a command has initiated a measurement, the instrument will not abort that reading.

PCB 1 Notations ⟶

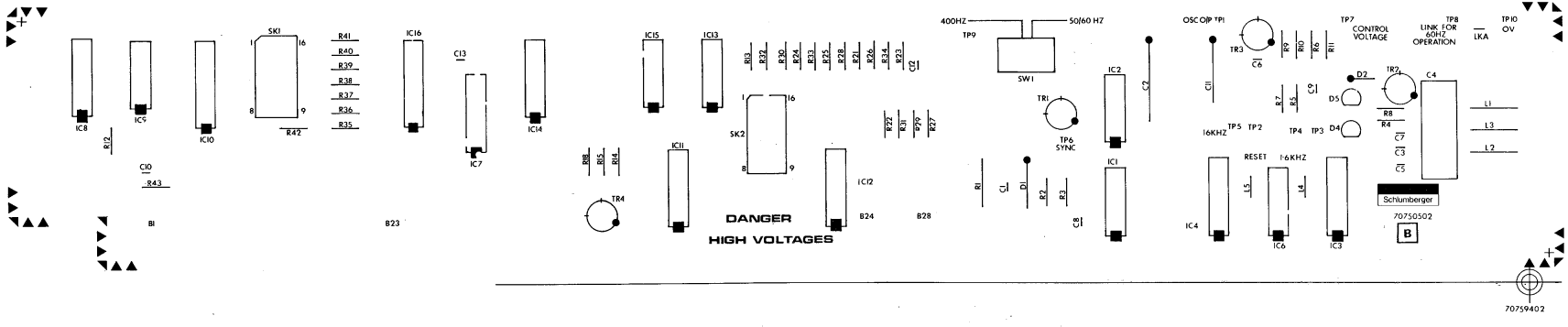


PCB 1 Notations

JWW/7075/5



Display Diag. 7.20 pcb 1



PCB 2 Notations

SECTION 8 Parts List

This section contains detailed parts lists for each of the printed circuit boards fitted in the instrument. When ordering spare parts, it is essential to quote the instrument serial number, located on the rear panel, as well as the full description shown in the appropriate parts list.

Parts lists for the optional Interfaces 70754 and 70755 are shown in Section 9 and 10 respectively.

COMPONENT PARTS LIST ABBREVIATIONS

CIRCUIT REFERENCES

AE	Aerial
B	Battery
C	Capacitor (μF)
CSR	Thyristor
D	Diode
FS	Fuse
IC	Integrated Circuit
L	Inductor
LP	Lamp (including Neon)
LK	Link
M	Motor
ME	Meter
MSP	Mains Selector Panel
PL	Plug
R	Resistor (Ω)
RE	Recording Instrument
RL	Relay
S	Switch
SK	Socket
T	Transformer
TP	Terminal Post (or Test Point)
TR	Transistor
V	Valve
X	Other Components

Also Used:-

RNL	Non Linear Resistor (Ω)
RV	Variable Resistor (Ω)

COMPONENT TYPES

Fixed Resistors		Variable Resistors		Capacitors	
Carbon Composition	CACP	Carbon Front Panel Multiturn	CAFM	Air	AIR
Carbon Film	CAFM	Carbon Front Panel Single Turn	CAFS	Aluminium Electrolytic	ALME
Cracked Carbon	CKCA	Carbon Preset Multiturn	CAPM	Aluminium Solid	ALMS
Metal Film	MEFM	Carbon Preset Single Turn	CAPS	Polycarbonate	CARB
Metal Oxide	MEOX	Cermet Front Panel Multiturn	CMFM	Ceramic	CERM
Power Wirewound	POWW	Cermet Front Panel Single Turn	CMFS	Polyester Foil	ESTF
Precision Wirewound	PRWW	Cermet Preset Multiturn	CMPM	Polyester Metallised	ESTM
Temperature Sensitive	TEMP	Cermet Preset Single Turn	CMPS	Glass	GLAS
Thick Film	TKFM	Wirewound Front Panel Multiturn	WWFM	Mica	MICA
Thin Film	TNFM	Wirewound Front Panel Single Turn	WWFS	Metallised Lacquer	MLAC
Voltage Sensitive	VOLT	Wirewound Preset Multiturn	WWPM	Paper Foil	PAPF
		Wirewound Preset Single Turn	WWPS	Paper Metallised	PAPM
				PTFE	PTFE
				Polypropylene Film	PYLN
				Polystyrene	STYR
				Tantalum Dry	TAND
				Tantalum Foil	TANF
				Tantalum Wet	TANW

PCB 1

Cct. Ref.	General Description				Solartron Part No.
R1 to R3	CACP	220k	1/4W	10%	172052200
R4	CACP	47k	1/4W	10%	172044700
R5	CACP	220k	1/4W	10%	172052200
R6	CACP	220k	1/4W	10%	172052200
R7 to R18	CACP	330k	1/4W	10%	172053300
R19	CACP	22k	1/4W	10%	172042200
R20	CACP	68k	1/4W	10%	172046800
R21 to R26	CACP	10k	1/4W	10%	172041000
D1	Zener	24V	0.4W	5%	300523930
D2	Zener	24V	0.4W	5%	300523930
D3	Zener	30V	0.4W	5%	300521430
D4	Zener	24V	0.4W	5%	300523930
TR1 to TR6	2N5401				300555470
V1 to V3	Display SP353				300730280
V4	Display SP354				300730290
V5 to V7	Neon Hivac 16H				300720300
V8 to V11	Neon, Hivac 23L				300720240
V12	Neon Hivac 1MH				300720460
SK1	16 pin DIL				300584860
SK2	16 pin DIL				300584860

Cct. Ref.	General Description				Solartron Part No.
D1	Zener	4.7V	0.4W	5%	300521470
D2	SD3				300522160
D4	MV2107				300525020
D5	MV2107				300525020
TR1	BCY70				300553590
TR2	2N4303				300553160
TR3	BFY90				300553890
TR4	MPS-A42				300555460
IC1	SN7413N				510000710
IC2	SN74393N				510002150
IC3	SN74109N				510002120
IC4	SN74390N				510002140
IC6	SN7490AN				510000280
IC7	SN74175N				510001310
IC8	SN7442N				510000330
IC9	SN7404N				510000410
IC10	DI258N				510002160
IC11	DD700				510001600
IC12	DD700				510001600
IC13	SN7408N				510000830
IC14	SN74175N				510001310
IC15	SN7403N				510001200
IC16	D1258N				510002160
TP1 to TP10	Disconnect pins				355900550
SK1	16 pin DIL				300584860
SK2	16 pin DIL				300584860
B1 to B28	Horizontal amp				352501700
L1 to L3	Choke, R.F. 22μH				305020630
S1	DPDT				375000510

PCB 2

Cct. Ref.	General Description				Solartron Part No.
R1	CACP	10k	1/2W	10%	172341000
R2	CACP	470	1/4W	10%	172024700
R3	CACP	1k	1/4W	10%	172031000
R4	CACP	220k	1/4W	10%	172052200
R5	CACP	1k	1/4W	10%	172031000
R6	CACP	220k	1/4W	10%	172052200
R7	CACP	680k	1/4W	10%	172056800
R8	CACP	2.7k	1/4W	10%	172032700
R9	CACP	82k	1/4W	10%	172048200
R10	CACP	1k	1/4W	10%	172031000
R11	CACP	220	1/4W	10%	172022200
R12	CACP	2.2k	1/4W	10%	172032200
R13	CACP	2.2k	1/4W	10%	172032200
R14	CACP	2.2k	1/4W	10%	172032200
R15	CACP	1.5k	1/4W	10%	172031500
R18	CACP	4.7k	1/4W	10%	172034700
R21 to R42	CACP	1M	1/4W	10%	172061000
R43	CACP	4.7k	1/4W	10%	172034700
C1	CERM	0.047	25V	+50% −25%	241944700
C2	TAND	100	10V	20%	265481000
C4	GLAS	2—24p	2000		290060020
C5	CERM	150p	500V	20%	241321500
C6	CERM	220p	500V	20%	241322200
C7	CERM	220p	500V	20%	241322200
C8 to C10	CERM	0.047	25V	+50% −25%	241944700
C11	TAND	15.0	20V	20%	265771500
C12	CERM	1000p	500V	20%	241331000
C13	CERM	330p	500V	20%	241323300

PCB 3

Cct. Ref.	General Description				Solartron Part No.
R1 to R3	CACP	4.7k	1/4W	10%	172034700
R4 to R7	CACP	3.3k	1/4W	10%	172033300
R8	CACP	1k	1/4W	10%	172031000
R9 to R12	CACP	4.7k	1/4W	10%	172034700
R13 to R15	CACP	3.3k	1/4W	10%	172033300
R16	CACP	1k	1/4W	10%	172031000
R17 to R22	CACP	3.3k	1/4W	10%	172033300
R23	CACP	2.7k	1/4W	10%	172032700
R24	CACP	3.3k	1/4W	10%	172033300
R25	CACP	3.3k	1/4W	10%	172033300
R26 to R28	CACP	4.7k	1/4W	10%	172034700
R29	CACP	220	1/4W	10%	172022200
R30	CACP	4.7k	1/4W	10%	172034700
R31	CACP	1k	1/4W	10%	172031000
R32	CACP	120	1/4W	10%	172021200
R33	CACP	120	1/4W	10%	172021200
R34	CACP	470	1/4W	10%	172024700
R35	CACP	1k	1/4W	10%	172031000
R36	CACP	1k	1/4W	10%	172031000
R37	CACP	470	1/4W	10%	172024700
R38	CACP	4.7k	1/4W	10%	172034700
R39	CACP	4.7k	1/4W	10%	172034700
R40	CACP	1k	1/4W	10%	172031000

PCB 3 (Cont)

Cct. Ref.	General Description				Solartron Part No.
R41	CACP	4.7k	1/4W	10%	172034700
R42	CACP	4.7k	1/4W	10%	172034700
C1	CERM	220p	500V	20%	241322200
C2 to C7	CERM	0.047	25V	+50% −25%	241944700
C8	CERM	0.047	25V	+50% −25%	241944700
C9 C11	CERM	0.047	25V	+50% −25%	241944700
C12 C13	TAND	15	20V	10%	265771500
C14	TAND	100	20V	20%	265881000
D1	SD3				300522160
IC1	SN7474N				510000490
IC2	SN7405N				510002080
IC3	SN7407N				510000750
IC4	SN7403N				510001200
IC5	SN74175N				510001310
IC6	SN74175N				510001310
IC7	SN7404N				510000410
IC8	SN7402N				510000270
IC9	SN7400N				510000340
IC10	SN7403N				510001200
IC11	SN74390N				510002140
IC12	SN7442N				510000330
IC13	SN74165N				510001480
IC14	SN7404N				510000410
IC15	SN7405N				510002080
IC16	SN7403N				510001200
IC17	SN74191N				510000940
IC18	SN7412N				510002090
IC19	SN7400N				510000340
IC20	SN7410N				510000420
IC21	SN7402N				510000270
IC22	SN7427N				510001590
IC23	SN7474N				510000490
IC24	SN7474N				510000490
IC26	SN7404N				510000410
IC27	SN7400N				510000340
IC28	SN7402N				510000270
IC29	SN7400N				510000340
IC30	5082-4351 Opto Coup.				300540150
IC31	5082-4351 Opto Coup.				300540150
IC32	SN74393N				510002150
IC33	SN74390N				510002140
IC34	5082-4360 Opto Coup.				300540160
IC35	SN7403N				510001200
IC36	SN7422N				510002100
IC37	5082-4360 Opto Coup.				300540160
IC38	SN7400N				510000340
IC39	5082-4360 Opto Coup.				300540160
SW1	2-way DPDT (sample)				379619201
SW2	2-way DPDT (control)				379600101
SW3	5-way DPDT (rate)				379613801
SW5	4-way DPDT (mode)				379613202
SW6	2-way DPDT (sefl check)				379613101
SK1	14 pin DIL				300584680
SK2	16 pin DIL				300584860
SK3	16 pin DIL				300584860
SK4	16 pin DIL				300584860
SK5	16 pin DIL				300584860
SK6	16 pin DIL				300584860
SK8	14 pin DIL				300584680
B1 to B28	Berg Post				355501050
TP1 to TP5	Disconnect pins				355900550
TP7 to TP10	Disconnect pins				355900550
	Test Hook				359600101
	Bus Bars				480090080

PCB 4

Cct. Ref.	General Description				Solartron Part No.
R1	CACP	470	1/4W	10%	172024700
R2	CACP	470	1/4W	10%	172024700
R3	CACP	2.7k	1/4W	10%	172032700
R4	CACP	2.7k	1/4W	10%	172032700
R5 to R12	CACP	4.7k	1/4W	10%	172034700
C1 to C6	CERM	0.047	25V	+50% −25%	241944700
C7	CERM	680p	500V	20%	241326800
C8	CERM	1000p	500V	20%	241331000
C9	CERM	330p	500V	20%	241323300
C10	CERM	330p	500V	20%	241323300
IC1	SN74393N				510002150
IC2 to IC4	SN74390N				510002140
IC5	SN74157N				510001280
IC6	SN7400N				510000340
IC8	SN74151N				510000850
IC9	SN74107N				510000810
IC10	SN7474N				510000490
IC11	SN74107N				510000810
IC12	SN7412N				510002090
IC13	SN7402N				510000270
IC14 to IC20	SN74190N				510000930
IC21 to IC24	SN74151N				510000850
IC25	SN74157N				510001280
IC26	SN7489N				510001300
IC27	SN7438N				510002110
IC28	SN7408N				510000830
IC29	SN7408N				510000830
IC30	SN7432N				510001510
IC31	SN7427N				510001590
IC32	SN7474N				510000490
IC33	SN7410N				510000420
IC34	SN7402N				510000270
IC35	SN7430N				510000430
IC36	SN7404N				510000410
IC37	SN7405N				510002080
IC38	SN7400N				510000340
TP1 to TP7	Disconnect Pins				355900550
SK1 to SK6	16 pin DIL				300584860

PCB 5

Cct. Ref.	General Description				Solartron Part No.
R1 to R4	CAPM	3.3M			169609102
R5	CAPM	100.05k			169609102
R7	CACP	470	1/4W	10%	172024700
R8	CACP	100k	1W	10%	172551000
R9	CACP	470	1/4W	10%	172024700
R10	CACP	100	1/4W	10%	172021000
R12	CACP	100k	1/4W	10%	172051000
R14	CACP	100	1/4W	10%	198221001
R102 to R105	CACP	1k	1/4W	10%	192731001
R108	WWPM	9.3k			169609001
R109	WWPM	909			169609001
R110	WWPM	100.84			169609001
R111	WWPM	276.5k			169609001
R112	MEFM	82k	1/4W	0.5%	198248201
R113	MEFM	10k	1/4W	0.1%	198141001
R114	CACP	220	1/4W	10%	172022200
R116 to R120	CACP	47k	1/4W	10%	172044700
R121	CACP	10k	1/2W	10%	172341000
R122	CACP	10k	1/2W	10%	172341000
R123	CACP	470k	1/4W	10%	172054700
R124	MEFM	1.5k	1/2W	0.5%	198231501
R126	CACP	47M	1/2W	10%	160100105
R201	MEFM	114.35k		0.1%	169608602
R202	MEFM	50k		0.1%	169608602
R203	MEFM	12k	1/4W	0.5%	198241201
R205	MEFM	680k	1/4W	0.5%	192756802
R206	MEFM	47k	1/4W	0.5%	198244701
R207	MEFM	10	1/2W	0.5%	198211001
R208	MEFM	21.5k	1/4W	0.5%	192742152
R209	MEFM	10	1/4W	0.5%	198211001
R210	CACP	10k	1/4W	10%	172041000
R211	CACP	10k	1/4W	10%	172041000
R212 to R215	CACP	4.7k	1/4W	10%	172034700
R217	CACP	1k	1/4W	10%	172031000
R218	CACP	1k	1/4W	10%	172031000
R220	CACP	100k	1/4W	10%	172051000
R224	CACP	100k	1/4W	10%	172051000
R280	CACP	2.2k	1/4W	10%	172032200
R281	CACP	1k	1/4W	10%	172031000
R282	CACP	4.7k	1/4W	10%	172034700
R301	MEFM	620	1/4W	0.5%	198226201
R302	CACP	470	1/4W	10%	172024700
R303	CACP	330	1/4W	10%	172023300
R304	CACP	6.8k	1/4W	10%	172036800
R305	WWPM	44k			169607702
R306	WWPM	44k			169607702
R307	MEFM	22k	1/4W	0.5%	198242201
R308	CACP	470	1/4W	10%	172024700
R309	CACP	6.8k	1/4W	10%	172036800
R310	CACP	330	1/4W	10%	172023300
R311	MEFM	44.2	1/4W	0.5%	160400536
R312	MEFM	86.6	1/4W	1%	160400417
R313	MEFM	169	1/4W	1%	160400418
R314	MEFM	332	1/4W	1%	160400419
R315	MEFM	649	1/4W	1%	160400420
R316	MEFM	1.27k	1/4W	0.5%	198231271
R317	WWPM	2.438k	1/4W	0.1%	169603101
R318	WWPM	4.844k	1/4W	0.1%	169603001
R319	WWPM	9.624k	1/4W	0.1%	169602901
R320	WWPM	19.124k	1/4W	0.1%	169602801
R321	WWPM	43.4k			169607801
R322	WWPM	28.09k			169607801
R323	MEFM	330k	1/4W	0.5%	198253301
R324	MEFM	10	1/4W	0.5%	198211001
R380	CACP	100	1/2W	10%	172321000
R401	CACP	100k	1/4W	10%	172051000
R403	MEOX	1k	1/4W	5%	192731001
R404	MEOX	1k	1/4W	5%	192731001
R405	MEFM	15k	1/4W	0.5%	198241501
R406	MEFM	15k	1/4W	0.5%	198241501
R407	MEOX	27k	1/4W	5%	192742702
R408	MEFM	1.5k	1/4W	0.5%	198231501
R409	MEFM	1.5k	1/4W	0.5%	198231501
R410	MEOX	18k	1/4W	0.5%	195641800
R414	MEOX	27k	1/4W	5%	192742702
R415	MEOX	3.3k	1/4W	5%	195633300
R417	MEOX	10k	1/4W	5%	195641000
R418	MEOX	6.8k	1/4W	5%	195636800
R422	MEOX	15k	1/4W	5%	195641500
R431	CACP	100k	1/4W	10%	172051000
R432	CACP	100k	1/4W	10%	172051000
R433	CACP	10k	1/4W	10%	172041000
R435	MEOX	47k	1/4W	5%	195644700
R437	MEOX	47k	1/4W	5%	195644700
R438	MEOX	47k	1/4W	5%	195644700
R439	MEOX	10k	1/4W	5%	195641000
R440	MEOX	10k	1/4W	5%	195641000
R441	CACP	100k	1/4W	10%	172051000
R442	CACP	100k	1/4W	10%	172051000
R443	CACP	470k	1/4W	10%	172054700
R444	CACP	470k	1/4W	10%	172054700
R445	CACP	2.2k	1/4W	10%	172032200
R446	CACP	1M	1/4W	10%	172061000
R449	CACP	100	1/4W	10%	172021000
R450	CACP	100	1/4W	10%	172021000
R459	CACP	470	1/4W	10%	172024700
R501		1M	1/2W	0.02%	160300430
R502		1M	1/2W	0.02%	160300430
R503		699.5k	1/2W	0.02%	160300413
R504		699.5k	1/2W	0.02%	160300413
R507	MEFM	100K	1/4W	0.5%	198251001
R508	MEFM	10	1/4W	0.5%	198211001
R509	CACP	470	1/4W	10%	172024700
R510	CACP	330	1/4W	10%	172023300
R511	CACP	2.2k	1/4W	10%	172032200
R701	MEFM	990k	2W	0.1%	169600501
R702	MEFM	10k	1/4W	0.1%	198141004
R703	MEFM	1.2k	1/4W	0.1%	198131204
R704	MEFM	94.5k	1/4W	0.5%	160400041
R705	MEFM	14.5k	1/4W	0.5%	198241454
R706	MEFM	100k	1/4W	0.5%	198251001
R707	CACP	1M	1/4W	10%	172061000
R708	MEFM	10M	1/4W	1%	198361001
R709	MEFM	10k	1/8W	5%	192741004
R710	MEFM	10k	1/8W	5%	192741004
R711	CACP	10k	1/4W	10%	172041000
R712	CAFM	10M	1/2W	5%	170871000
R713	MEFM	1.179k	0.2W	0.02%	160400544
R714	MEFM	140.6	0.2W	0.02%	160400550
R715	MEFM	1.8k	1/4W	0.5%	198231801
R716	CACP	470	1/2W	10%	172324700
R717	CACP	10k	1/4W	10%	172041000
R718	MEFM	10k	1/4W	0.5%	172041000
R724	MEFM	10k	1/4W	0.5%	198241001
R738	CACP	100k	1/4W	10%	172051000
R744	CACP	10k	1/4W	10%	172041000
R745	CACP	10k	1/4W	10%	172041000
R746	CACP	100k	1/4W	10%	172051000
R748	CACP	10k	1/4W	10%	172041000
R749	CACP	10k	1/4W	10%	172041000
R751	CACP	100k	1/4W	10%	172051000
R752	MEFM	390k	1/4W	1%	198353901
R753	MEFM	12k	1/4W	0.5%	198241201
R754	CACP	56k	1/4W	10%	172045600
RV1	CMPM	5k		10%	130935000
RV101	CMPM	5k		10%	130935000
RV102	CMPM	20k		10%	130942000
RV103	CMPM	5k		10%	130935000
RV201	MEFM	20		5%	119601901
RV202	CMPM	100k		10%	130951000
RV203	CMPM	10k		10%	130941000
RV301	CMPM	100		10%	130921000
RV302	CMPM	100k		10%	130951000
RV501	CMPM	100k		10%	130951000
RV502	CMPM	1k		10%	130931000
RV503	CMPM	1k		10%	130931000
RV701	CMPM	2k		10%	130932000
RV702	CMPM	10k		10%	130941000
RV703	CMPM	1k		10%	130931000
RV704	CMPM	200		10%	130922000
RV705	CMPM	100k		10%	130951000
RV706	CMPM	2k		10%	130932000
RV707	CMPM	2k		10%	130932000

PCB 5 (Cont.)

Cct. Ref.	General Description				Solartron Part No.
C1	ESTF	1000p	160V	10%	210231000
C2	CERM	0.01	3kV	20%	208450085
C101	ESTF	100p	160V	10%	210221000
C103	CERM	0.047	25V	+50% −25%	241944700
C104	CERM	0.047	25V	+50% −25%	241944700
C201	CERM	0.047	25V	+50% −25%	241944700
C204 to C206	CERM	0.047	25V	+50% −25%	241944700
C208	ESTF	0.1	100V	10%	225451000
C209	ESTF	0.01	100V	10%	225441000
C210	ESTF	0.01	100V	10%	225441000
C211	ESTF	0.01	100V	10%	225441000
C212 to C214	CERM	0.047	25V	+50% −25%	241944700
C220	CERM	100p	500V	20%	241321000
C221	CERM	100p	500V	20%	241321000
C240	CERM	0.047	25V	+50% −25%	241944700
C299	CERM	0.1	30V	+50% −25%	242051000
C302	CERM	0.047	25V	+50% −25%	241944700
C303					
C304	ESTF	0.1	100V	10%	225451000
C305	CERM	0.047	25V	+50% −25%	241944700
C307	CERM	0.047	25V	+50% −25%	241944700
C310	CERM	0.047	25V	+50% −25%	241944700
C312	CERM	0.047	25V	+50% −25%	241944700
C401	TAND	100	25V	10%	273581000
C402	TAND	100	25V	10%	273581000
C404	TAND	4.7	35V	20%	266064700
C405	CERM	1000p	500V	20%	241331000
C406	TAND	47	35V	20%	266074700
C407	TAND	47	35V	20%	266074700
C408	CERM	0.047	25V	+50% −20%	241944700
C409	STYR	1000p	400V	10%	210231000
C411	TAND	15	20V	10%	265771500
C412	TAND	15	20V	10%	265771500
C413	ESTF	0.047	100V	10%	225444700
C414	ESTF	0.047	100V	10%	225444700
C415	CERM	3,300p	500V	20%	241333300
C417	ESTF	0.1	100V	10%	225451000
C418	CERM	10p	200V	10%	240611000
C419	ESTF	2.2	63V	10%	225162200
C421	TAND	4.7	35V	20%	266064700
C422	CERM	150p	500V	20%	241321500
C424	TAND	4.7	35V	20%	266064700
C426	CERM	0.047	25V	+50% −25%	241944700
C428	TAND	15	20V	10%	265771500
C429	CERM	10p	500V	20%	241311000
C501	PYLN	0.033	200V	2%	208100184
C503	PYLN	0.033	200V	2%	208100184
C504 to C506	CERM	0.047	25V	+50% −25%	241944700
C701	ESTF	0.47	400V	20%	226154700
C702	ESTF	0.01	1000V	10%	222841000
C703	STYR	120p	125V	2.5%	210121200
C705	MICA	680p	350V	5%	250326800
C706	CERM	3.3p	200V	15%	240603300
C709	ESTF	0.01	100V	10%	225441000
C710	CERM	100p	500V	20%	241321000
C711	CERM	100p	500V	20%	241321000
C721	TAND	220	10V	20%	265482200
C722	ESTF	1	100V	10%	225461000
C723	ESTF	10	63V	10%	219971000
C725	ESTF	1	100V	10%	225461000
C736	Variable PTFE	2p — 7p			290060080
D1	Zener	13V	0.4W	5%	300523920
D2	Zener	13V	0.4W	5%	300523920
D3	Light Emitting MA2801R				300750090
D4	Light Emitting MA2801R				300750090
D101	ZENER	4.7V	.4W	5%	300521470

Cct. Ref.	General Description				Solartron Part No.
D102	ZENER	4.7V	.4W	5%	300521470
D103	Zener	13V	0.4W	5%	300523920
D104	Zener	13V	0.4W	5%	300523920
D105 to D108	1N3595				300523590
D201	1N3595				300523590
D202	1N3595				300523590
D203	Zener	4.7V	0.4W	5%	300521470
D204	Zener	4.7V	0.4W	5%	300521470
D205	SD3				300522160
D206	SD3				300522160
D208	ZENER	12V		± 5%	300521480
D301	USR 932	9.3V	0.4W	5%	300525610
D303	SD3				300522160
D401	1N3595				300523590
D402	1N3595				300523590
D403	Zener	8.2V	0.4W	5%	300521330
D404	Zener	8.2V	0.4W	5%	300521330
D405	Zener	5.6V	0.4W	5%	300521450
D406	5082—266				300525380
D407	5082—266				300525380
D408	Zener	8.2V	0.4W	5%	300521330
D419	Zener	5.6V	0.4W	5%	300521450
D701 to D703	SD3				300522160
D706	Zener	3.3V	0.4W	5%	300521860
D707	1N3595				300523590
D708	1N3595				300523590
D709	Zener	9.1V	1W	5%	300525410
D710	Zener	9.1V	1W	5%	300525410
D711	ZENER	2.7V		± 5%	300523870
D712	ZENER	2.7V		± 5%	300523870
D801	SD3				300522160
D803	SD3				300522160
D809 to D812	SD3				300522160
D814	SD3				300522160
TR1	WN807				300555380
TR2	WN807				300555380
TR3	U1899				300554320
TR4	U1899				300554320
TR101 to TR104	U1899E				300554320
TR105	U1899				300554320
TR201	U1899				300554320
TR202	U1819				300553800
TR203	U1819				300553800
TR204	U1819				300553800
TR205	U1899				300554320
TR301	BC107				300553320
TR302	BCY70				300553590
TR401	2N2484				300552860
TR402	2N4303				300553160
TR403	Dual FET NDF9410/WD401				300555370
TR404	Dual FET U235				300553810
TR405	2N4303				300553160
TR408	Dual FET NDF9410/WD401				300555370
TR409	Dual FET NDF9410/WD401				300555370
TR410	2N2484				300552860
TR411	2N4303				300553160
TR501	BC107				300553320
TR701	3N163				300554530
TR702	BC107				300553320
TR703	3N163				300554530
TR704	Dual FET, U235				300553810
TR705	U1899				300554320
TR706	U1899				300554320
TR707	BC107				300553320
TR708	U1899				300554320
TR709	U1899				300554320
IC101	AD506LH				510090260
IC201	Mono OP-07CJ				510090310
IC202	LM301AH				510000620
IC203	LM311H				510090050
IC204	LM311H				510090050
IC205	SN7474N				510000490

PCB 5 (Cont.)

Cct. Ref.	General Description	Solartron Part No.
IC206	SN7474N	510000490
IC301	Mono OP-07CJ	510090310
IC302	Mono OP-07CJ	510090310
IC401	CA3183 AE.NPN Array	300555390
IC402	LM301AH	510000620
IC404	CA3084, PNP Array	300555360
IC405	LM301AH	510000620
IC406	AD 506L	510090260
IC408	LM201AH	510090300
IC501	Mono OP-07CJ	510090310
IC701	LM318H	510090210
IC706	RMS-DC Converter	559600401
RLF1 to RLF3	MRA 500 Reed	300670120
RLE1 to RLE3	MRA-500 Reed 30AT	300670120
RLB	Relay 2p C/O, 2p N/O Varley	301200805
RLC	Relay 2p C/O Varley	301201903
RLK	Relay 1p c/o R5-24V ITT	300651980
RLL	Relay 1p c/o R5-24V ITT	300651980
LDR1 to LDR4	NSL-364C	300540070
	Ceramic Beads 5.5mm length	470120060
	Reed Drive Coils 1.4k	309506702
	Disconnect pins	355900550
	TO5 Heatsinks	300584200
SK1 to SK5	14 pin DIL	300584680
	Posts, Berg	355500980
TH301	Oven 007 (80°C)	300584370
	Eyelet	356020050

PCB 6

Cct. Ref.	General Description				Solartron Part No.
R216	CACP	470	1/4W	10%	172024700
R219	CACP	3.3k	1/4W	10%	172033300
R220	CACP	1k	1/4W	10%	172031000
R221	CACP	10k	1/4W	10%	172041000
R223	CACP	33k	1/4W	10%	172043300
R228	CACP	33k	1/4W	10%	172043300
R229	CACP	470	1/4W	10%	172024700
R451	CACP	4.7k	1/4W	10%	172034700
R452	CACP	47k	1/4W	10%	172044700
R454	CACP	6.8k	1/4W	10%	172036800
R455	CACP	68k	1/4W	10%	172046800
R456	CACP	22k	1/4W	10%	172042200
R457	CACP	1.8k	1/4W	10%	172031800
R458	CACP	2.2k	1/4W	10%	172032200
R601	MEFM	68k	1/4W	0.5%	198246801
R602	WWPM	69.96k	1/2W	0.1%	169608501
R603	MEFM	44.2	1/4W	0.5%	160400536
R604	WWPM	82k	1/2W	0.1%	169608501
R605	WWPM	8.208k	1/4W	0.005%	169603405
R606	WWPM	910.6k	1/4W	0.005%	169603304
R607	WWPM	8.19M	1/4W	0.05%	160300450
R608	MEFM	10.96k	1/2W	0.1%	160400549
R610	POWW	5.6k	6W	5%	173735600
R611	CACP	10k	1/4W	10%	172041000
R612	CACP	6.8M	1/2W	10%	172366800
R613	MEFM	780k	1/4W	0.5%	198257801
R614	MEFM	6.96k	1/4W	0.1%	160400537
R803 to R807	CACP	10k	1/4W	10%	172041000
R809	CACP	10k	1/4W	10%	172041000
R811 to R814	CACP	10k	1/4W	10%	172041000
R816 to R819	CACP	10k	1/4W	10%	172041000
R820	CACP	2.2k	1/4W	10%	172032200
R821	CACP	10k	1/4W	10%	172041000
R822	CACP	33k	1/4W	10%	172043300

Cct. Ref.	General Description				Solartron Part No.
R825	CACP	2.2k	1/4W	10%	172032200
R826	CACP	2.2k	1/4W	10%	172032200
R828	CACP	120	1/2W	10%	172321200
RV601	CERM	50		10%	130915000
RV602	CERM	1k		10%	130931000
RV603	CERM	20k		10%	130942000
RV604	CERM	100		10%	130921000
C217	MICA	390p	500V	5%	250323900
C218	MICA	390p	500V	5%	250323900
C425	ESTF	0.15	100V	10%	225451500
C427	CERM	0.047	25V	+50% −25%	241944700
C601	STYR	1000p	160V	10%	210231000
C602	CERM	33p	500V	20%	241313300
C604	CERM	100p	500V	20%	241321000
C605	CERM	33p	500V	20%	241313300
C801	CERM	0.047	25V	+50% −25%	241944700
C802	ESTF	0.01	100V	10%	225441000
C803	CERM	3,300p	500V	20%	241333300
C804	TAND	22	35V	10%	266072200
C805	CERM	0.047	25V	+50% −25%	241944700
C806	CERM	470p	500V	20%	241324700
C807	CERM	470p	500V	20%	241324700
D207	Zener	10V	0.4W	5%	300522760
D208	Zener	12V	0.4W	5%	300521480
D410	SD3				300522160
D411	SD3				300522160
D416	Zener 9.1V		0.4W	5%	300521340
D601	SD3				300522160
D606	1N4007				300524990
D802	SD3				300522160
D804 to D808	SD3				300522160
D813	SD3				300522160
D815 to D817	SD3				300522160
TR601	WN807				300555380
TR602	3N163				300554530
TR605	WN807				300555380
TR606	WN807				300555380
TR412	BC107				300553320
TR413	BC107				300553320
IC207	SN74123N				510000980
IC208	SN74393N				510002150
IC209	SN74390N				510002140
IC210	SN7406N				510000760
IC407	LM301AH				510000620
IC601	Mono OP-07CJ				510090310
IC602	AD506LH				510090260
IC603	LM301AH				510000620
IC802	SN74159N				510002180
IC803	SN7445N				510000900
IC804	SN74156N				510001270
IC805	D125BP				510002060
IC806	SN7445N				510000900
IC807	SN74156N				510001270
IC808	D125BP				510002060
IC809	SN7414N				510001990
IC810	SN7407N				510000750
IC811	SN74L00N				510001030
IC812	SN7406N				510000760
IC813	SN74L00N				510001030
IC814	SN74175N				510001310
IC815	SN74175N				510001310
IC816	SN74123N				510000980
IC818	SN74L00N				510001030
IC819	SN74164N				510001150
RLH1	Reed Relay				301202201
RLH2	Reed Relay				301202201
RLG1	Reed Relay				301202201
RLG2	Reed Relay				301202201
RLD1	Reed MRA500				300670120
RLD2	Reed MRA500				300670120
SK1 to SK8	14 pin DIL				300584680

PCB 7

Cct. Ref.	General Description				Solartron Part No.
R1	CACP	470k	1/2W	10%	172354700
R2	CACP	12k	1/2W	10%	172341200
R3	CACP	3.3k	1/4W	10%	172043300
R4	CACP	3.3k	1/4W	10%	172033300
R5	MEOX	330k	1/2W	1%	195453300
R6	CACP	3.3k	1/4W	10%	172033300
R7	MEXO	100k	1/4W	5%	195651000
R9	MEOX	33k	1/4W	5%	195643300
R10	MEOX	470	1/4W	5%	195624700
R11	MEFM	36k	1/2W	1%	192743602
R12	CACP	22k	1/4W	10%	172042200
R13	CACP	10	1/4W	10%	172011000
R14	CACP	10k	1/4W	10%	172041000
R15	POWW	1k	6W	5%	173731000
R16	CACP	3.3k	1/4W	10%	172033300
R17	CACP	27	1/4W	10%	172012700
R18	POWW	2.2	2½W	5%	173042200
R19	CACP	10k	1/4W	10%	172031000
R20	MEOX	100k	1/4W	5%	195651000
R22	MEOX	100k	1/4W	5%	195651000
R23	MEOX	33k	1/4W	5%	195643300
R24	MEOX	68k	1/4W	5%	195646800
R25	CACP	68	1/4W	10%	172016800
R26	CACP	22	1/4W	10%	172012200
R27	CACP	22	1/4W	10%	172012200
R28	CACP	3.3k	1/4W	10%	172033300
R29	CACP	68k	1/4W	10%	172046800
R30	CACP	68k	1/4W	10%	172046800
R31	CACP	3.3k	1/4W	10%	172033300
R32	CACP	22	1/4W	10%	172012200
R33	CACP	22	1/4W	10%	172012200
R101	CACP	150	1/4W	±10%	172021500
R102	CACP	100	1/4W	±10%	172021000
R103	CACP	33	1/4W	±10%	172013300
R104	CACP	330	1/2W	±10%	172323300
R105	CACP	1M	1/4W	±10%	172061000
R106	CACP	22	1/4W	±10%	172012200
RV1	CMPM	10k	1/3W	10%	130641000
RV2	CMPM	20k	1/3W	10%	130642000
RV101	CAPS	10k	1/2W	±20%	137341000
C1	ESTM	0.047	100V	10%	225444700
C2	ESTF	0.1	400V	±10%	226151000
C3	ESTM	3.3	100V	±10%	225463300
C4	CERM	0.047	25V	+50% −20%	241944700
C5	ESTF	6800p	100V	±10%	227036800
C6	TAND	10	20V	±20%	265871000
C7	TAND	1	35V	±20%	266061000
C8	ESTF	680p	160V	±10%	221326800
C9	TAND	1	35V	±20%	266061000
C10	CERM	1000p	400V	±20%	241331000
C11	CERM	1000p	400V	±20%	241331000
C12	ESTM	0.1	160V		220351000
C13	CERM	0.01	25V		241941000
C14	CERM	0.01	25V		241941000
C15	CERM	3.3	1000V	±10%	225463300
C16	CERM	100p	500V	±20%	241321000
C17	CERM	0.1	30V		242051000
C101	CERM	0.047	30V	+50% −10%	241944700
C102	CERM	0.047	30V	+50% −10%	241044700
C103	CERM	3300p	500V	±20%	241333300
C104	ALME	47	40V	+100% −20%	273774700
C105	ALME	47	40V	+100% −20%	273774700
C106	ALME	22	40V	+100% −20%	273772200
C107	ALME	22	40V	+100% −20%	273772200
C108	CERM	3300p	500V	±20%	241333300
C109	ALME	49	40V	+100% −20%	273774700
C110	ALME	47	40V	+100% −20%	273774700
C111	CERM	0.047	30V	+50% −20%	241944700
C112	CERM	0.047	30V	+50% −20%	241944700
C113	ALME	220	10V	+100% −10%	273182200
C114	CERM	0.047	33V	+50% −20%	241944700
C115	ALME	220	10V	+100% −10%	273182200
C116	CERM	0.047	30V	+50% −20%	241944700
C117	CERM	0.1	30V	+50% −25%	242051000
C118	CERM	0.1	30V	+50% −25%	242051000
C119	ALME	1.0	350V		274561000
C122	CERM	1000p	500V	±20%	241331000
C123	TAND	1	35V	±20%	266061000
C124	CERM	2.2p	500V		208450094
D1	IN4007				300524990
D2	Zener	13V			300523920
D3	Zener	15V			300524820
D4	SD3				300522160
D5	SD3				300522160
D6	MR856				300525550
D7	Zener	15V	1W		300524820
D8	Zener	82V	IN5375B		
D9	SD3				300522160
D10	Zener	5.6V			300521450
D11	Bay 72				300524530
D12	Bay 72				300524530
D13	Zener	2.7V			300523870
D14	Bay 72				300524530
D15	Zener	15V			300521390
D101 to D108	BAY 72				300524530
D109	MR850				300525560
D110	MR850				300525560
D111	IN5821 (SHOTTKY)				300525630
D112	IN5821 (SHOTTKY)				300525630
D113	MR856				300525550
D114	MR856				300525550
D115	SD3				300522160
D116	SD3				300522160
D119	Zener	10V			300522760
IC1	LM318				510090210
IC2	LM318				510090210
IC101			+18V		510090340
IC102			−18V		510090350
TR1	TIP 50				300555450
TR2	BCY 70				300553590
TR4	TIP 54				300555350
TR6	2N5401				300555470
TR7	BC107				300553320
TR8	BC107				300553320
TR9	BCY70				300553590
TR10	BC107				300553320
TR11	BC107				300553320
TR12	TIP 54				300555350
TR13	TIP 54				300555350
T1	RM6				309608702
T2					309608805
T3					309608805
L1	RM10	4mH			3095086
L2	FX1115				309010060
L3	FX1115				309010060
L101	40µH				309507001
L103	40µH				309507001
IC101	+18V				510090340
IC102	−18V				510090350
SK1	14 pin d.i.l.				300584680
FS1	Fuse Clips 20mm				360208110
	Fast Blo 500mA				360106090
	Disconnect pins				355900550
	Ceramic beads				470120060

PCB 10

Cct. Ref.	General Description	Solartron Part No.
D1 to D4	MA2801R LED	300750090
SK	Bottom Entry Vertical PV	352501680

PCB 11

Cct. Ref.	General Description	Solartron Part No.
SK1	16 way DIL	300584860
SK2	Cannon 50 way	352550110
SK5	16 way DIL	300584860
SK6	16 way DIL	300584860
	Disconnect Pins	355900550

PCB 12

Cct. Ref.	General Description				Solartron Part No.
R1	CACP	4.7k	1/4W	10%	172034700
R2	CACP	330	1/4W	10%	172023300
R3	CACP	150k	1/4W	10%	172051500
R4	CACP	47k	1/4W	10%	172044700
R5	CACP	4.7k	1/4W	10%	172034700
R6	CACP	470	1/4W	10%	172024700
R7	CACP	470	1/4W	10%	172024700
R8	CACP	4.7k	1/4W	10%	172034700
R9	CACP	330	1/4W	10%	172023300
R10	CACP	150k	1/4W	10%	172051500
R11	CACP	47k	1/4W	10%	172044700
R12	CACP	4.7k	1/4W	10%	172034700
R13	CACP	10k	1/4W	10%	172041000
R14	CACP	10k	1/4W	10%	172041000
R15	CACP	330	1/4W	10%	172023300
R16	CACP	4.7k	1/4W	10%	172034700
R17	CACP	47k	1/4W	10%	172044700
R18	CACP	68k	1/4W	10%	172046800
R19	CACP	47k	1/4W	10%	172044700
R20	CACP	47k	1/4W	10%	172044700
C1 to C5	CERM	220p	500V	20%	241322200
C6	CERM	10p	500V	20%	241311000
C7	CERM	10p	500V	20%	241311000
C8	CERM	0.047	25V	+50% —25%	241944700
C9	CERM	0.047	25V	+50% —25%	241944700
C10	CERM	33p	500V	20%	241313300
C11	CERM	10p	500V	20%	241311000
C12	CERM	100p	500V	20%	241321000
D1	SD3				300522160
D2	SD3				300522160
TR1	BCY70				300553590
TR2	BC107				300553320
TR3 to TR5	BCY70				300553590
TR6	BC107				300553320
TR7	BCY70				300553590
TR8	BC107				300553320
	Horizontal Amp Sockets				352501700

PCB 13

Cct. Ref.	General Description				Solartron Part No.
TH1	VA1104			+50%	161000024
C1	ALME	190	400V	—25%	274882200
D1 to D4	IN4007				300524990
	Disconnect Pins				355900550

MAIN ASSEMBLY

Cct. Ref.	General Description	Solartron Part No.
R1	Zenamic Voltage Suppressor Z10L471	110024080
SKA	Front Input	352105010
SKB	Rear Input	352105010
SKC	Mains Filter	550000990
FS1	800mA	360206010
SA	Mains On/Off	377000290
T1	Transformer	309610501
	Escutcheon	420610050
	Bush	419600101
	Ext. Ref. Terminal Post 4mm Red	355100510
	Ext. Ref. Terminal Post 4mm Black	355100500
	Fuse Link 20mm Slo-Blo	360106310
PL	14 way DIL	351314050
PL	16 way DIL	351316010
	14 way 3M Cable	480095330
	16 way 3M Cable	480095440

SETTING UP AND CALIBRATION

INTRODUCTION

This section provides a comprehensive setting-up and calibration procedure which may be necessary after rectification and/or a component replacement on the Digital Voltmeter.

It is divided into two parts as follows:-

1) Setting-Up Procedures

   These involve partial strip down of the instrument in order to effect initial adjustments of the circuit parameters.

2) Calibration Procedures

   The final adjustments provide an instrument performance which is compatible with the specification published in Part 1, Section 2 of this manual. For normal calibration only Part 2 of this section should be followed. Where an instrument fails a calibration, or has undergone rectification and/or a component replacement, it is advisable to carry out the full procedure detailed in this section.

NOTE: It is essential when carrying out setting-up or final calibration procedures that they be completed and carried out in the order given.

TEST EQUIPMENT

The test equipment used must have an accuracy/uncertainty equal to or better than that shown in the calibration tables.

The test equipment listed below should be available to perform the following procedures correctly.

a) Mains Isolation Transformer

b) Variac.

c) Digital Voltmeter (e.g. Type 7040).

d) Oscilloscope plus x 10 probe (e.g. A100).

e) D.C. Voltage Standard.

f) A.C. Voltage Standard (e.g. Hewlett Packard 745A).

g) Resistance Standard 100Ω to 10MΩ (e.g. ESI DB62 or ESI RS624 and separate 10MΩ Standard).

h) Voltage Divider (e.g. ESI RV722).

additional items required.

5-terminal input lead

Cannon plug (Connect pins 10, 12, 14 and 42 together).

PART 1– SETTING-UP PROCEDURES

PRELIMINARY

1. Prepare the instrument as follows:-

CAUTION: THE INSTRUMENT SHOULD BE DISCONNECTED FROM THE MAINS SUPPLY BEFORE ANY ATTEMPT IS MADE TO REMOVE THE TOP COVER.

BEWARE OF GUARD POTENTIAL ON THE GUARD PLATE WITH THE TOP COVER REMOVED.

BEWARE OF MAINS POTENTIAL ON THE POWER SUPPLY WITH THE TOP COVER REMOVED.

a) At the top corners, on the rear of the instrument, remove the screw securing each buffer.

b) Remove the two buffers.

c) Remove the top cover by sliding it away from the front panel.

2. Check that the correct fuse is fitted as indicated beside the fuse holder.

POWER SUPPLY SWITCHING WAVEFORM

1. Connect the 7075 to the mains isolating transformer, as shown in Fig 9.1

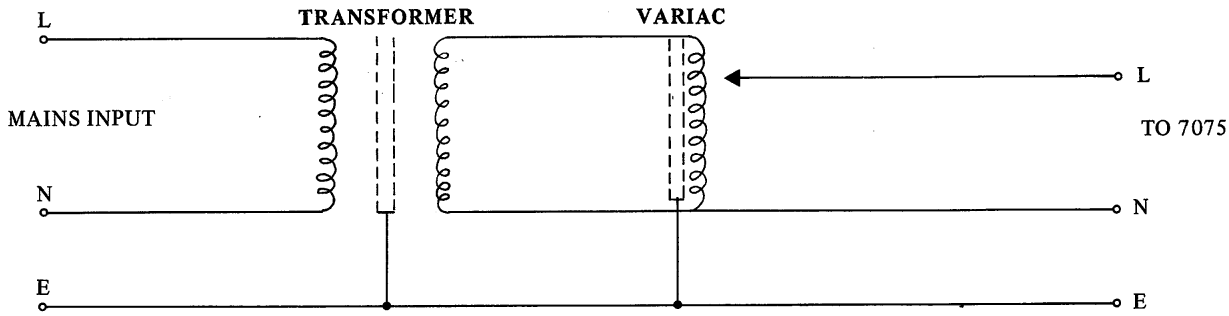


Fig 9.1

2. Set the variac for minimum output.

3. Connect a voltmeter between TP2 and input negative on pcb 7.

4. Connect an oscilloscope via a x 10 probe to TP3 on pcb 7 and input negative.

5. Switch on the instrument.

6. Adjust the variac for 60V input and check the following:.

   a) A display should begin to appear on the instrument under test.

   b) A reading of 50V ±15V on the voltmeter, and

   c) A 60V p/p amplitude waveform on the oscilloscope.

7. Adjust the variac for 120V input.

8. Check that the voltmeter reading is 60V ±10V.

9. Increase the input to 240V.

10. Check that the switching waveform is within the limits shown. (Fig 9.2)

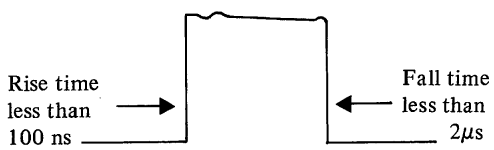


FIG 9.2 Switching Waveform

11 Disconnect the oscilloscope from TP3 and connect to TP4.

12. Check that the display is 30V p/p ±3V p/p and 46μs±5μs duration. The difference between two half cycles must not exceed 5μs.

13. Disconnect the oscilloscope from TP4.

14. Disconnect the voltmeter from TP2.

RAIL CHECKS

1. Connect a voltmeter to TP20 (+30V) and adjacent 0V pin on pcb 6.

2. Adjust RV1 on pcb 7 for a voltmeter reading of 30V ±0.1V

3. Vary the mains input between 120V and 260V.

4. Ensure that the reading does not change by more than ±0.2V from that in operation 2.

5. Adjust the mains input to 230V.

6. Switch off the instrument under test.

7. Disconnect the voltmeter from TP20 and the 0V pin.

The Table 9.1 below summarises the voltage rails in the instrument. These need not be checked unless a fault is suspect.

Table 9.1

AREA	RAIL	VALUE
FLOATING RAILS PCB 6 (measure with respect to OV floating)	+30V	+30V ± 0.1V
	+20V	+20.5V ± 1.5V
	+21V	+21V ± 1V
	+18V	+18V ± 1V
	−18V	−18V ± 1V
	−21V	−21V ± 1V
	−20V	−20V ± 1V
	−30V	−30V ± 1V
	+5V	+5V ± 0.5V
EARTHY RAILS PCB 7 (measure with respect to OV)	+180V	+175V ± 5V
	+5V	+5V ± 0.5V
	−18V	−18V ± 3V

EARTHY LOGIC CHECKS

1. Remove the plug from SK7 on pcb 6.

2. Switch on the instrument.

3. Select the following modes: D.C., LOCAL, 20ms, REP.

4. The display should read ±0.000000V.

CLOCK OSCILLATOR ADJUSTMENTS

1. Switch S1 to 50Hz operation.
2. Connect a voltmeter between TP7 (+ve) and TP10 (-ve) 0V on pcb 2.
3. Adjust C4 on pcb 2 for a reading of 2.2V ±100mV on the voltmeter.
4. Disconnect the voltmeter from TP7 and TP10.

CONVERSION TO 60Hz OPERATION (operate instrument from a 60Hz supply)

1. On pcb 2 link TP8 to TP10. (Diag. 7.19 refers).
2. On pcb 6, open circuit zener diode D207 by removing the bridging solder from the split pad.
3. Connect a voltmeter between TP7 (+ve) and TP10 (-ve).
4. Adjust C4 on pcb 2 for a reading 2.2V ±100mV on the voltmeter.
5. Reset the forcing waveform as in operation 8 of the floating checks.

CONVERSION TO 400Hz OPERATION (operate instrument from a 400Hz supply).

1. With all circuit arrangements as for 50Hz operation, set switch S1 on pcb 2 to the 400Hz position.

INTEGRATION TIMES

1. Press the TEST button on the instrument front panel, the display should read 00.000V.

On selection of the integration rate buttons the appropriate readings should be displayed:-

Integration time	Display reading
1mS	±00.00V
20mS	±00.000V
100mS	±00.0000V
1s	±00.00000V
10s	±00.000000V *

* It may be necessary to wait up to 10s before the last zero appears.

ANNUNCIATOR CHECKS

1. Release the TEST button.
2. Select the 1s integration time.
3. Press the SINGLE SAMPLE button once.
4. The BUSY annunciator should illuminate for approximately 1 second.
5. Select REP.

6. Select RATIO, check that the RATIO annunciator is illuminated.

7. Release RATIO.

8. Select AC, check that the AC annunciator is illuminated.

9. Select Ω , check that the kΩ annunciator is illuminated.

10. Select RATIO, check that the RATIO annunciator is NOT illuminated. (with Ω selected)

11. Release the RATIO button.

12. Switch off the instrument.

13. Reconnect the plug to SK7 on pcb 6.

FLOATING CHECKS **Self-check system and forcing waveform**

1. Switch on the instrument.

2. Select the 100ms integration time and D.C. mode.

3. Select TEST. The display should read 07.0000V ±0.1V. 07.000 3/4

4. Press the STEP button. The display should now read 00.0000V ±20mV. +250μV

5. Adjust RV202 (10V ZERO) on pcb 5 as necessary for a reading of 00.0000V ±1mV.

6. Set RV203 on pcb 5 fully clockwise.

7. Connect an oscilloscope between TP5 and TP7 (0V) on pcb 6.

8. Adjust RV203 until the waveform is 20μs ±2μs duration. If RV203 has insufficient range to adjust the waveform, remove the soldered track across the split-pad (behind D207 and D208 on pcb 6) and repeat the adjustment.*

9. Disconnect the oscilloscope from TP5 and TP7.

10. Press the STEP button. The display should read 10.0000V ±3V. 10.0816 V

11. Press the STEP button again. The display should now read 10.0000kΩ ±200Ω. 10.0084 kΩ

12. Press the STEP button once more.

13. All the bars in all the positions should be displayed, (a row of 8's).

14. Release the TEST button.

*This facility is only available on instruments with Serial Numbers from 001441 onwards.

INPUT AMPLIFIER

1. Select the 1s integration time button.

2. Fit the 2-terminal cables to the front panel input socket and short circuit the leads.

3. The display should read within the limits ±20μV. +240 μV

4. Check that the μV zero control can be adjusted to obtain a reading within the limits ± 8μV.

5. Finally adjust the μV zero control for a reading of zero, or as near zero as possible.

6. Remove the short circuit.

7. Connect a 1MΩ resistor across the input terminals.

8. The display should settle to less than ± 70μV. Disconnect the 1MΩ resistor from the input terminals.

   NOTE: If available, the use of a 1MΩ resistor enclosed in an input plug removes the effects of movement near the input cable.

9. Connect a voltmeter to TP14 and 0V on pcb 6.

10. Apply -10V to the 7075 input noting the voltmeter reading at TP14.

11. Apply +10V to the instrument input. Ensure that the voltmeter reading does not exceed that in operation 10., above, by more than 15mV.

12. Disconnect the voltmeter from TP14 and 0V.

13. Note the instrument display reading.

14. Connect a 1MΩ resistor in series with the high input and the DC source.

15. The display reading should be within ±50 bits of that in operation 13.

16. Repeat operations 13, 14, 15 at the rear input socket on the instrument with a negative voltage.

17. Remove the DC source.

18. Remove the input lead from the rear socket.

19. Disconnect the resistor fitted in operation 14.

20. Connect the input lead to the front panel input socket.

NOISE CHECK

1. Ensure the 1s integration rate is selected.
2. Short circuit the input leads and adjust the μV zero control for a reading as near to zero as possible.
3. Select the 100ms rate.
4. The display should not exceed ±1 bit for 10 seconds.
5. Select the 20ms rate.
6. The display should not exceed ±2 bits for 10 seconds.

REFERENCE ADJUSTMENTS

A DC Standard should be used for the reference and ratio checks.

1. Fit the Cannon plug to the systems interface socket SK1 at the rear panel of the instrument to command the 10V range remotely. (refer to additional Test Equipment, see page 9.2)
2. Select the 1s integration ratio.
3. Adjust RV202 (10V zero) on pcb 5 for a display reading of zero ±5 bits.
4. Remove the short circuit from input leads.
5. Apply -10V to the input
6. Adjust RV301 (-10V Cal) for a reading of -10.0000V ±20 bits.

The total scatter on readings with ±10V input to the instrument should not exceed 4 bits. If RV301 does not have enough adjustment, links A to K will require re-adjustment. Normally adjustment of links A, B or C will be sufficient. However if the Zener D301 has been changed it may be necessary to adjust some of the other links; this is best done by successive approximation bearing in mind the weighting of each link (see Fig. 7.9).

RATIO CALIBRATION

1. Select RATIO and the 100ms integration rate buttons.
2. Apply the voltages in Table 9.2 to the external reference terminals located on the rear panel of the instrument and to the input socket on the front panel.

Table 9.2

TEST	INPUTS		OPERATION	READING	± BITS	NOISE ± BITS
	EXT REF TERMINALS	FRONT PANEL INPUT				
1	+ 10V	− 10V	RV503 (RATIO CMR)	− 10.0000V	3	1
2	+ 2V	− 2V	RV501 (RATIO ZERO)	− 10.0000V	5	3
3	Repeat tests 1 and 2 as necessary					
4	+ 10V	+ 10V	RV502 (RATIO CAL)	+ 10.0000V	3	1
5	+ 2V	+ 2V	RV302 (RATIO CAL BAL)	+ 10.0000V	5	3
6	Repeat tests 4 and 5 as necessary					

3. Release the RATIO button.

4. Remove the DC source.

5. Remove the external reference leads.

6. Remove the 10V range command plug from SK1.

COMMON MODE

DC REJECTION

1. Connect the instrument as shown in Fig . 9.3

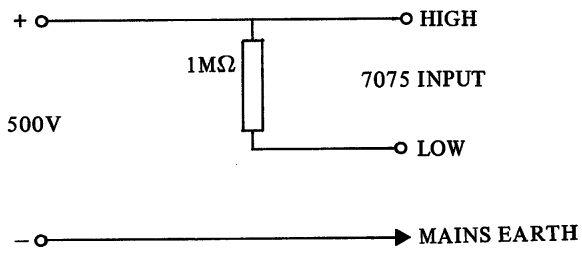


Fig 9.3

2. Apply 500V to the instrument.

3. The reading on the display should not exceed 10mV.

4. Remove the DC source.

5. Disconnect the 1MΩ resistor.

DC RANGE CALIBRATION

10V RANGE

1. Select the 1s integration rate.

2. Command the 10V range remotely.

3. Short circuit the input leads.

4. Adjust RV202 (10V ZERO) for a reading of 0.00000V ±1 bit.

5. Remove the short circuit from the input leads.

6. Apply -10V to the input.

7. Adjust RV301 (-10V Cal) for a reading of -10.00000V ±5 bits.

8. Apply +10V to the input.

9. Adjust RV201 (+10V Cal) for a reading of 10.00000V ±5 bits.

Repeat operations 6 to 9 as necessary.

LINEARITY

1. With the 10V range commanded and the 10V DC Standard and Decavider connected to the input terminals, check the linearity in accordance with Table 9.3

Table 9.3

INPUT	READING	TOLERANCE (bits)
10V	10.00000V	± 3
9V	9.00000V	± 3
8V	8.00000V	± 3
7V	7.00000V	± 3
6V	6.00000V	± 3
5V	5.00000V	± 3
4V	4.00000V	± 3
3V	3.00000V	± 3
2V	2.00000V	± 3
1V	1.00000V	± 3
0.1V	0.10000V	± 2
0.01V	0.01000V	± 2
0.001V	0.00100V	± 2
0V	0.00000V	± 2

2. Repeat for negative values using the same voltage source.

3. Increase the DC source to the Decavider to +100V, adjusting the Decavider for a display reading of +10.00000V ±1 bit on the instrument under test.

4. Change the Decavider output to 13.90000V.

5. Ensure the 7075 display reading is 13.90000V ±3 bits.

6. Repeat operation 3 to 5 for negative polarity.

7. Remove DC source.

8. Remove the 10V range command plug from SK1.

10mV AND 1V RANGE CALIBRATION

1. Select the 1s integration rate.

2. Short out the input leads.

3. Adjust the μV zero control for a zero reading on the display.

4. Remove the short circuit.

5. Apply the voltages as per table 9.4., using a DC standard and Decavider.

Table 9.4

TEST	INPUT	OPERATION	READINGS	
			VALUE	± bits
1	− 10 mV	RV 103 (10mVDC)	0.010000V	1
2	− 100mV	RV 102 (100mVDC)	0.100000V	2
3	− 1V	RV 101 (1V DC)	1.000000V	5
4	Repeat tests 1 to 3 as necessary			

6. Apply similar positive inputs and check that the readings obtained for the two polarities do not differ by more than:

   a) 1μV on the 10mV range.

   b) 4μV on the 100mV range.

   c) 24μV on the 1V range.

100V AND 1000V RANGE CALIBRATION

1. Apply -100V to the 7075 input direct from the DC source.

2. Adjust RV1 on pcb 5 (100V DC) for a reading of −100,0000V ± 20 bits

3. Increase the input to -1000V. The display should settle to -1000.000V ±50 bits.

4. The drift after 1 minute should be less than ±5 bits.

5. Remove the DC source.

AC CALIBRATION

1. Connect the AC standard to the instrument.

2. Select the AC and 20ms modes.

3. Apply the voltages in Table 9.5

Table 9.5

TEST	INPUT	FREQUENCY	OPERATION	READING	
				VALUE	± bits
1	1V	1 kHz	RV706 (1V LF)	1.0000V	3
2	0.15V	1 kHz	RV705 (AC ZERO)	0.1498V	1
3	0. 5V	1 kHz	Check	0.5000V	5
4	1V	10 kHz	"	1.0000V	10
5	1V	100 kHz	"	1.0000V	30
6	0.15V	100 kHz	"	0.1500V	20
7	0. 1V	1 kHz	RV704 (100mV LF)	0.10000V	3
8	0.01V	1 kHz	Check	0.01000V	5
9	0. 1V	100 kHz	"	0.10000V	30
10	10V	100 kHz	RV702 (10V L.F)	10.000V	5
11	10V	100 kHz	C736 (SET HF)	10.000V	30
12	10V	10 kHz	Check	10.000V	10
13	100V	1 kHz	"	100.00V	10
14	100V	100 kHz	"	100.00V	50
15	100V	10 kHz	"	100.00V	15
16	800V	1 kHz	RV703 (1000V LF)	800.00V	8
17	500V	100 kHz	Check	500.00V	50
18	150V	10 kHz	"	150.00V	10

Repeat tests 1 and 2 as necessary

4. Remove the AC source.

5. Short circuit the input leads.

6. The display should be less than 50 bits .

7. Remove the short circuit.

8. Select the 1s integration time.

9. Apply 1V at 10Hz.

10. The display should be 1.00000V ±350 bits.

11. Select the 20ms integration time.

12. Press the TEST button.

13. Press the STEP button twice.

14. The AC self check reading should be displayed.

15. Adjust RV701 (10V AC SELF CHECK) on pcb 5 as necessary for a reading of 10.000V ±50 bits.

16. Release the TEST button.

17. Disconnect the input lead from the instrument.

OHMS CALIBRATION

1. Select the OHMS mode.

2. Connect the 5 terminal lead to the front panel input socket.

3. Short circuit 4 terminals (Leaving the DC low "black" terminal floating).

4. Adjust RV604 (OHMS ZERO) on pcb 6 for a reading of less than 1Ω.

5. Remove the short circuit.

OHMS RANGE CALIBRATION

1. Connect the resistance standard to the instrument and carry out checks as per Table 9.6

Table 9.6

TEST	INPUT	OPERATION	READINGS	
			VALUE	± bits
1	10 kΩ	RV601 (SET 10 kΩ)	10.00000 kΩ	10
2	10 MΩ	RV603 (SET 10 MΩ)	10000.00 kΩ	30
3	1 MΩ	RV602 (SET 1 MΩ)	1000.000 kΩ	10
4	Repeat tests 1 to 3 as necessary			
5	1kΩ	Check	1.000000 kΩ	20
6	13.9 kΩ	"	13.90000 kΩ	25
7	100 kΩ	"	100.0000 k Ω	70

2. Repeat test 6 of Table 9.6 using the rear input socket

3. Disconnect the resistance standard from the instrument.

4. Disconnect the input lead.

5. Switch off the instrument.

This concludes the setting up of the DVM and it should now be followed by a full calibration.

PART 2 - CALIBRATION PROCEDURES

INTRODUCTION

The following calibration is basically the final calibration to which all instruments are subjected prior to despatch from the factory.

For the greatest accuracy the DVM top cover should be removed and its calibration cover, Part No. 70759D, fitted. Failing this, allowances must be made for variations in the working temperatures.

See Appendix for details of calibration cover.

PRELIMINARY PROCEDURE

For the following checks the DVM will have its top cover removed and be fitted with its calibration cover (if available).

1. Prepare the instrument as follows:-

CAUTION: THE INSTRUMENT SHOULD BE DISCONNECTED FROM THE MAINS SUPPLY BEFORE ANY ATTEMPT IS MADE TO REMOVE THE TOP COVER.

BEWARE OF GUARD POTENTIAL ON THE GUARD PLATE WITH THE TOP COVER REMOVED.

BEWARE OF MAINS POTENTIAL ON THE POWER SUPPLY WITH THE TOP COVER REMOVED.

a) At the top corners on the rear of the instrument, remove the screw securing each buffer.

b) Remove the two buffers.

c) Remove the top cover by sliding it away from the front panel.

2. Check that the correct fuse is fitted as indicated beside the fuse holder:

For calibration procedures to be carried out at $20^{o}C$, it is essential that the following test equipment or its equivalent is available.

TEST EQUIPMENT

a) Guildline Standard Cell plus stand-by power supply.

b) Cambridge Potentiometer with 2V and 4V primary cells.

c) Sullivan Volts ratio box.

d) Cropico Null Detector.

e) DC Source (COHU)

f) Resistance standard 10Ω to $10M\Omega$.

g. Temperature control conditions.

additional items required.

5-terminal input lead

Cannon plug (Connect pins 10, 12, 14 and 42 together).

It should be noted that if the calibration equipment used does not meet the uncertainty specification of the items listed, the Limits of Error specified in Section 2 of this manual will not be achieved. Measurements made with the dvm after such recalibration therefore, while exhibiting errors no worse than those specified, *will be related to the calibration equipment* rather than to the internationally agreed volt.

CALIBRATION

The calibration sequence must be carried out in the order given. Calibration should be carried out at an ambient temperature 20°C ±1°C after a warm-up period of at least 2 hours with the calibration cover fitted.

CALIBRATION AT 20°C

1. Fit the 7075 with its calibration cover.
2. Switch on the instrument at least 2 hours before commencing calibration.
3. Command the 10V range remotely, via the rear connector socket SK1.
4. Select 1s integration rate, DC and REP.
5. Connect the 2-terminal lead to the front panel input socket.
6. Short circuit the input leads.
7. Adjust RV202 (10V zero) for a reading of zero ±1 bit.
8. Remove the short circuit.
9. Apply -10V to the input lead.
10. Adjust RV301 (-10V) for a reading of -10.00000V ±3 bits.
11. Apply +10V to the input.
12. Adjust RV201 (+10V) for a reading of 10.00000V ±3 bits.
13. Repeat operations 9 to 12. as necessary until the readings meet the limits specified.
14. Select RATIO.
15. Apply the voltages as per Table 9.7

    Allow time for the 7075 readings to stabilize after each change of reference voltage.

Table 9.7

TEST	INPUTS		OPERATION	READING	± BITS	NOISE ± BITS
	EXT REF TERMINALS	FRONT PANEL INPUT				
1	+ 10	– 10V	RV503 (RATIO CMR)	– 10.00000V	20	4
2	+ 2	– 2V	RV501 (RATIO ZERO)	– 10.00000V	50	20
3	Repeat test 1 and 2 as necessary					
4	+ 10V	+ 10V	RV502 (RATIO CAL)	+ 10.00000V	20	4
5	+ 2V	+ 2V	RV302 (RATIO CAL BAL)	+ 10.00000V	50	20
6	Repeat test 4 and 5 as necessary					

16. Remove the external reference leads.

17. Release RATIO.

18. Recheck tests 6 to 12, allowing time for the display readings to stabilize.

19. Remove the 10V range command plug from socket SK1.

D.C. RANGE - CALIBRATION

1. Connect the 7075 low input terminal to earth.
2. Short circuit the input leads.
3. Adjust the μV zero control for a display reading of zero.
4. Remove the short circuit.
5. Apply the voltages as per Table 9.8

Table 9.8

TEST	INPUT	OPERATION	READING	
			VALUE	± bits
1	– 10mV	RV103 (100mV DC)	– 0.010000V	1
2	+ 10mV	Check	0.010000V	1
3	– 100mV	RV102 (100mV DC)	– 0.100000V	2
4	+ 100mV	Check	0.100000V	2
5	–1V	RV101 (IVDC)	– 1.000000V	4
6	+ 1V	Check	1.000000V	4
7	Repeat tests 1 to 6 as necessary			
8	– 1000V	RV1 (100V DC)	– 1000.000V	5
9	+ 1000V	Check	1000.000V	5
10	– 100V	Check	– 100.0000V	8
	+ 100V	Check	100.0000V	8

6. Disconnect the input lead from the instrument.

Note: Adjust for equal readings. Share any deviations equally between readings.

OHMS RANGE CALIBRATION

1. Connect the 5-terminal lead to the front panel input socket.
2. Select the OHMS mode.
3. Apply the resistance values as per Table 9.9

Table 9.9

TEST	INPUT	OPERATION	READINGS	
			VALUE	± bits
1	10kΩ*	RV 601 (SET 10kΩ)	10.00000KΩ	5
2	10MΩ	RV 603 (SET 10MΩ)	10000.00KΩ	10
3	1 kΩ	RV 602 (SET 1MΩ)	1000.000KΩ	5
4	Repeat tests 1 to 3 as necessary			
5	100 kΩ		100.0000KΩ	20
6	1 kΩ		1.000000KΩ	
7	10 Ω		0.010000KΩ	

* Note: Allow 5 minutes for 7075 reading to stabilize.

4. Disconnect the cable fitted in operation 1.

AC RANGE CALIBRATION

1. Connect the 2-terminal lead to the front panel input socket.
2. Select AC and the 100ms integration rate.
3. Apply the voltages as per Table 9.10

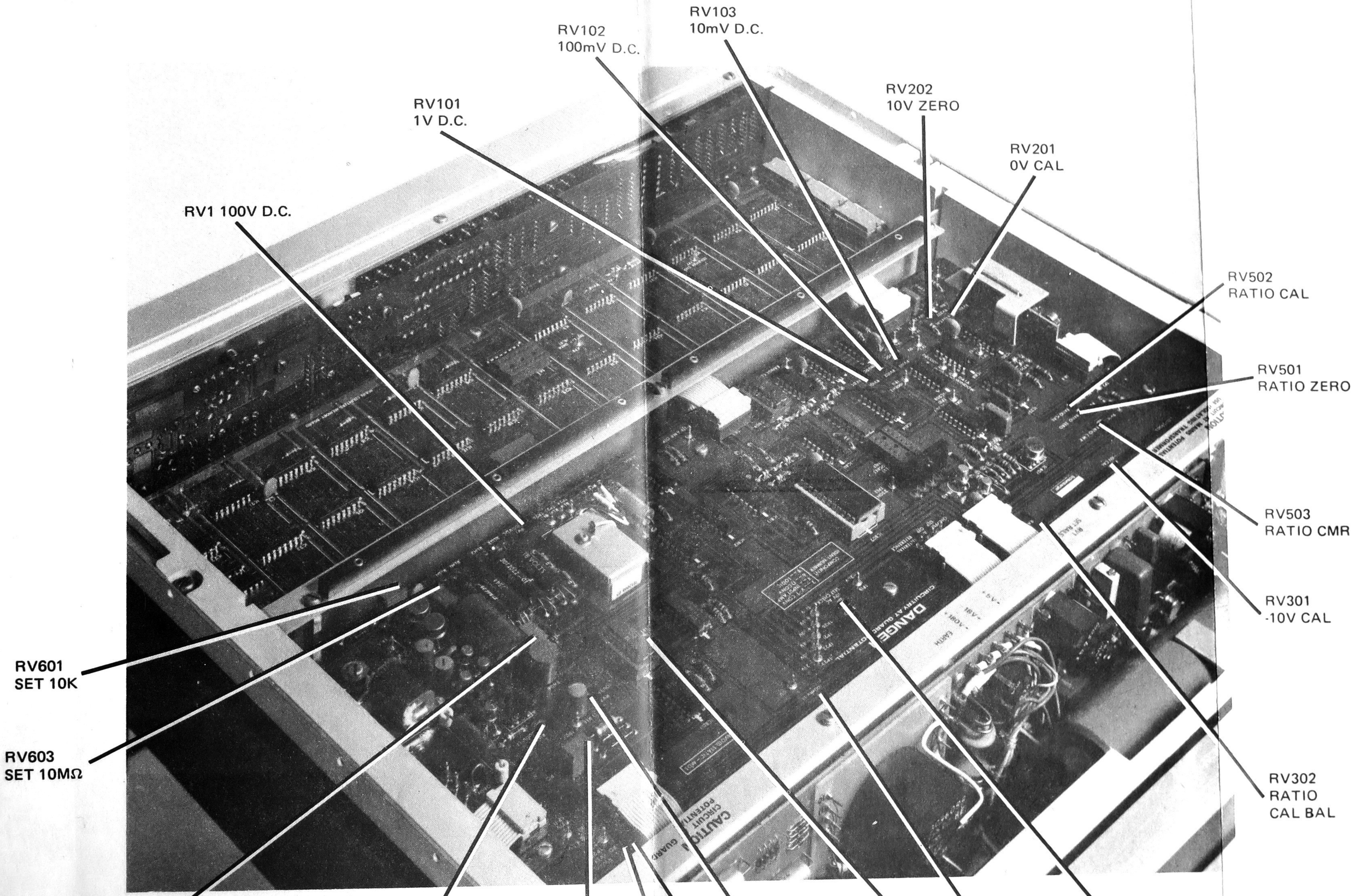
Table 9.10

TEST	INPUT	FREQUENCY	OPERATION	READING	
				VALUE	± bits
1	1V	1 KHZ	RV 706 (1U L.F)	1.00000V	20
2	0.15V	1 KHZ	RV 705 (AC ZERO)	0.14980V	10
3	Repeat tests 1 and 2 as necessary				
4	1V	10 KHZ		1.00000V	100
5	1V	100 KHZ		1.00000V	300
6	0.15V	100 KHZ		0.15000V	150
7	0. 1V	1 KHZ	RV 704 (100 mV L.F)	0.100000V	20
8	0. 1V	100 KHZ		0.100000V	400
9	0.01V	1 KHZ		0.010000V	50
10	10V	1 KHZ	RV 702 (10V L.F)	10.0000V	20
11	10V	100 KHZ	C736 (SET H.F)	10.0000V	400
12	10V	10 KHZ		10.0000V	100
13	1. 5V	10 KHZ		1.5000V	50
14	100V	1 KHZ		100.000V	20
15	100V	10 KHZ		100.000V	100
16	100V	100 KHZ		100.000V	300
17	15V	10 KHZ		15.000V	50
18	750V	1 KHZ	RV 703 (1000V L.F)	750.00V	20
19	750V	10 KHZ		750.00V	100
20	200V	100 KHZ		200.00V	200
21	150V	10 KHZ		150.00V	50
22	10V	100 KHZ		10.0000V	300

Notes:

1. Test 18, allow time for reading to settle.
2. Test 11. Adjust C736 as necessary for best overall frequency response.
3. Test 22. Check Test 18 does not produce any significant changes to Test 11 readings.

This concludes the calibration of the DVM.


RV103
10mV D.C.
RV102
100mV D.C.
RV202
10V ZERO
RV101
1V D.C.
RV201
0V CAL
RV1 100V D.C.
RV502
RATIO CAL
RV501
RATIO ZERO
RV503
RATIO CMR
RV301
-10V CAL
RV601
SET 10K
RV603
SET 10MΩ
RV302
RATIO
CAL BAL
RV602
SET 1MΩ
RV703
1000V LF
RV604
ZERO Ω
RV705
AC ZERO
RV706
IV L.F.
RV702
C736
SET H.F.
RV704
100mV
L.F.
AC701
10V AC
SELF CHECK

Servicing: Data Systems Options

SECTION 10

Parallel BCD Interface Unit 70754

PARALLEL BCD INTERFACE UNIT
Circuit Description

Board 1 Diag 10.1

Commands from board 2 arrive on cable S and are fed directly to the 7075 via PLA.

FRONT PANEL LOCKOUT is OR-ed with REMOTE from the front panel to disable all front panel buttons except SAMPLE.

FRONT PANEL LOCKOUT disables the SAMPLE buttons directly (PLA pin 48).

SAMPLE commands (PULSE or CONTACT) on cable S pin 15 are passed by ICIc if:–

a. The instrument is in SINGLE SAMPLE

or b. cable S pin 16 FRONT PANEL LOCKOUT is active (Low).

PRINT COMMAND on pin 21 of PLA is transmitted to board 3 via ICIa if the instrument is in the SINGLE SAMPLE mode.

Command data and an eight pulse strobe signal arrive on pins 27 and 25 of PLA respectively, soon after a SAMPLE command is given. IC8a compares this information as it is transferred into the shift register IC3, with that already present and being shifted out from the previous transfer. IC6b provides a signal DATA IS CHANGED which is output on PLA pin 45 to the DVM. This contributes to the delay before a measurement is started. For an unconditional 20ms delay link SP1 may be broken.

The final information on IC3 is used for the mode and range output information. SP2, 3 and 5, the range output codes, control the adder IC4. The final code appears on cable T pins 11, 12 and 13, the mode output information on cable T pins 9 and 10. When PRINT COMMAND is active (High) IC10a inhibits transfers, thus protecting the output information.

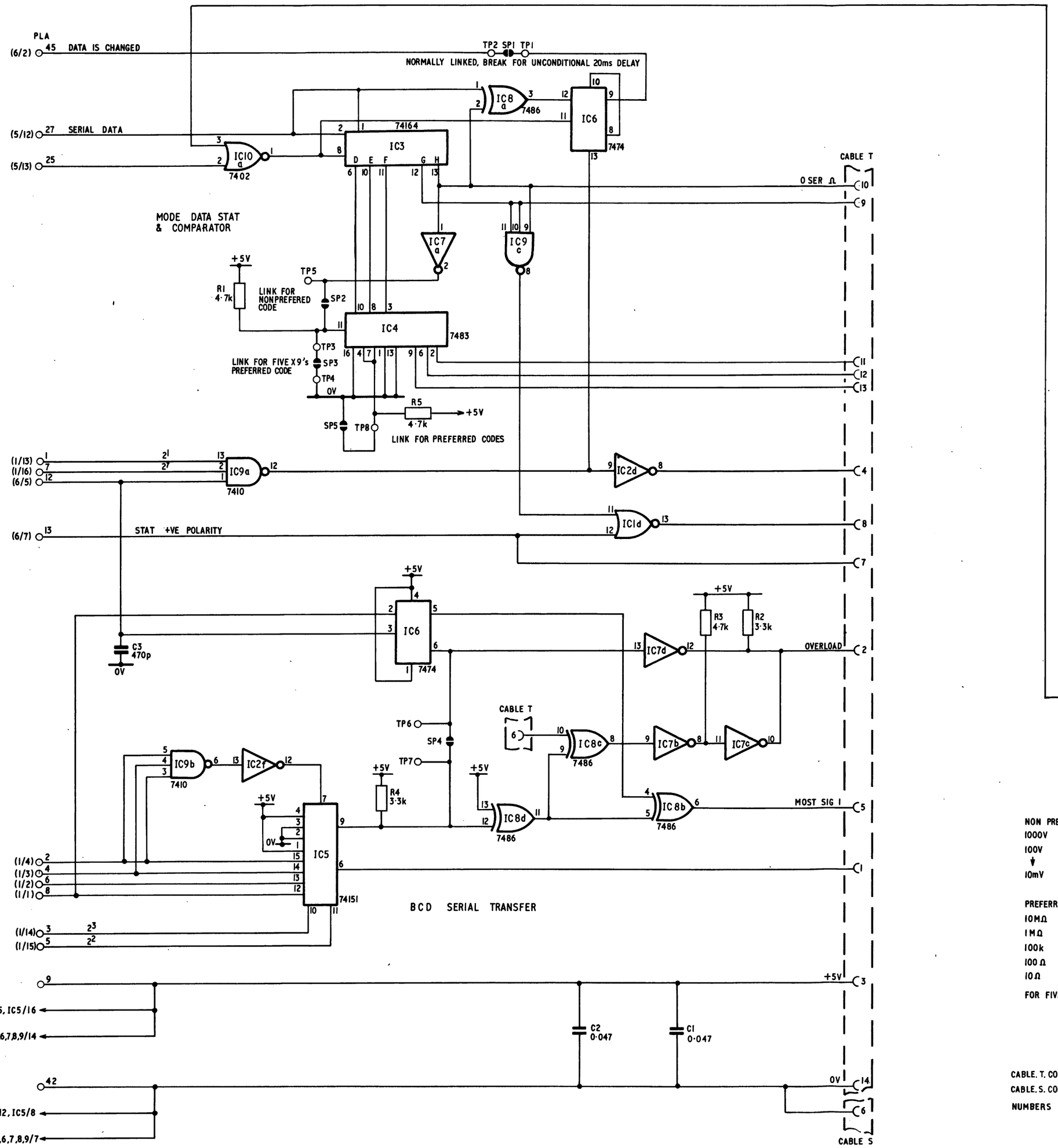
Measurement data from the 7075 arrives bit-parallel, word-serial on pins 2, 4, 6 and 8 of PLA and is converted to bit serial, word-serial by the multiplexer IC5. The timing lines on pin 3 and 5 of PLA count from 0-3 while each BCD word is present, selecting each bit in sequence and applying it to cable T pin 1. Data is always present and the relevant 8 BCD words are selected by IC9a which gates shift clock pulses through to board 3 *only* during STAT (IC9a pin 1 High) and IC9a pin 2 High (a slow timing line). This results in a burst of 32 pulses in phase with the serial bits on cable T pin 1 at the end of each measurement.

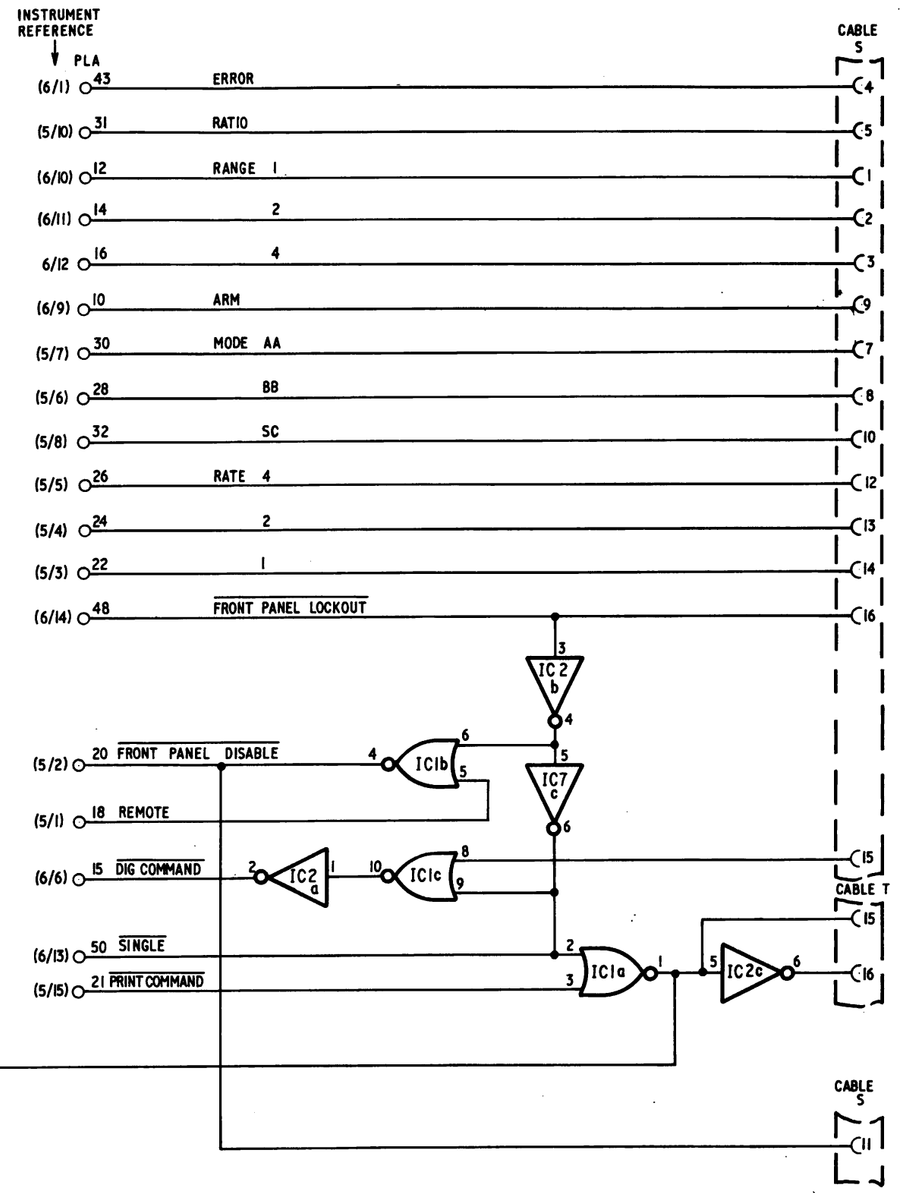
For non-BCD characters on pins 2, 4, 6 and 8 of PLA, IC9b forces IC 5 pin 6 high, causing zero's to appear on the outputs of board 3. The most significant 1 BCD character is present at the beginning of this sequence and is clocked into IC6a from pin 12 on PLA. This is normally applied to board 3 via IC8b.

Overload (cable T pin 2) is normally active (High) for a most significant 1 on IC6a pin 6 and a "4" in the second BCD word on board 3 outputs (cable T pin 6 = high) i.e. a full scale reading of 1400000.

If link SP4 is made, full scale is reduced to 999999.

A most significant 1 detected by IC6a pin 6 forces IC5 pin 9 Low selecting, for the rest of the transfer, the BCD word 9 present on IC5 inputs 4. 3, 2, 1. This word is fed in place of the input data to board 3. Overload is than active for readings above 999999. Cable T pin 6 will be low and overload is directly determined by IC6a. Cable T pin 5 is also held at a Low.





NON PREFERRED RANGE OUTPUT CODE

1000V	000	10MΩ
100V	001	1MΩ
↓		
10mV	101	100Ω
	110	10Ω

PREFERRED RANGE OUTPUT CODE 6 X 9's

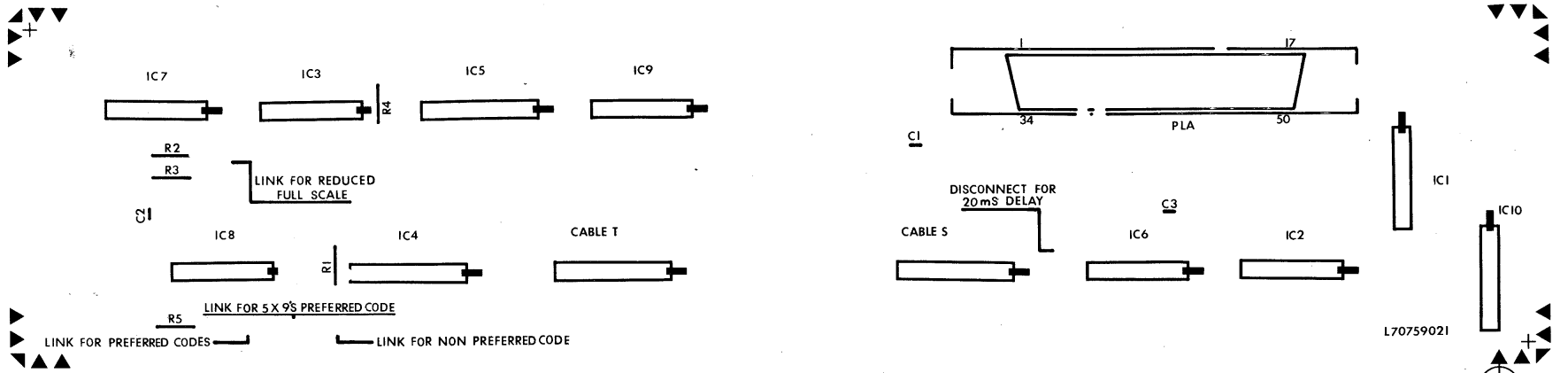
10MΩ	1	010
1MΩ	1000V	011
100k	100V	100
100Ω	100mV	111
10Ω	10mV	000

FOR FIVE X 9's PREFERRED CODE SUBTRACT ONE

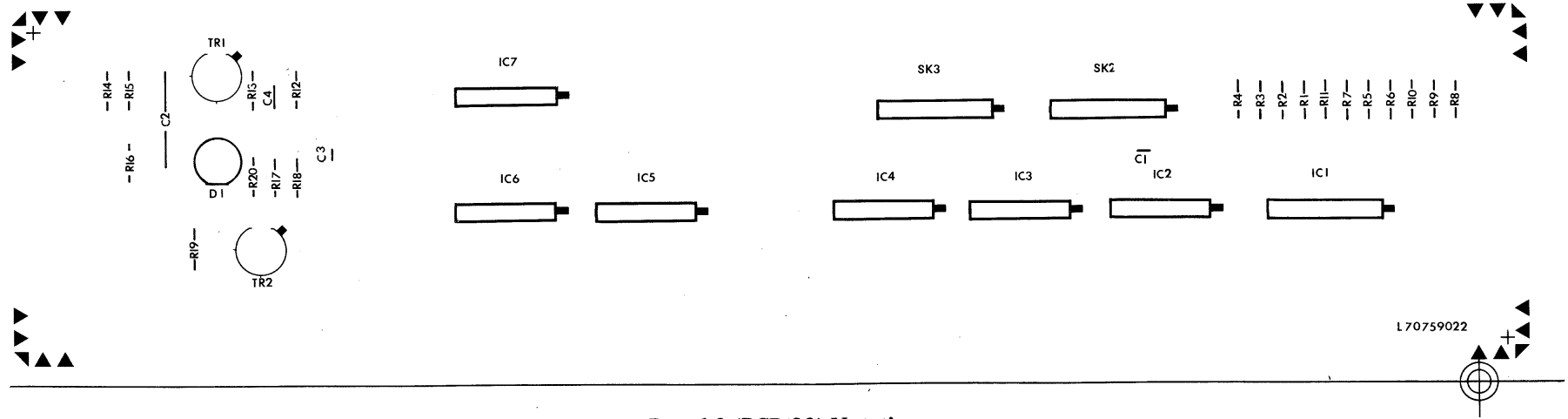
CABLE. T. CONNECTS TO SK1 ON BOARD 3] 16 PIN D.I.L. SOCKETS
CABLE. S. CONNECTS TO SK3 ON BOARD 2]

NUMBERS NEXT TO CIRCLES REFER TO PIN CONNECTIONS ON 50 WAY CANNON. PLUG PLA

Board 1 Diag. 10.1



Board 1 (PCB 21) Notations



Board 2 (PCB 22) Notations

Board 2 Diag 10.2

RANGE COMMAND codes applied to ICI are converted to internal codes, by incrementing by 1 for the OHMS mode and 2 for the VOLTS DC/AC mode.

IC3a, b and d disable these range commands if:–

1. ERROR is detected by the instrument on SK3 pin 4 (IC 6 pin 1 goes low).

2. in Local operation, IC7 pin 1 high→IC6 pin 6 high →IC6 pin 2 low.

3. in the Self Check mode, SK3 pin 10 low.

RATIO COMMAND (Low at SK2 pin 1) is transmitted to the instrument via SK3 pin 5 unless:–

1. It is in the OHMS mode (IC 5 pin 4 not low)

or 2. in the Self Check mode (IC 6 pin 4 low)

or 3. in Local operation (IC 7 pin 1 high).

MODE codes on SK2 pins 9 and 10 are transmitted to the instrument unless:–

1. It is the Self Check mode

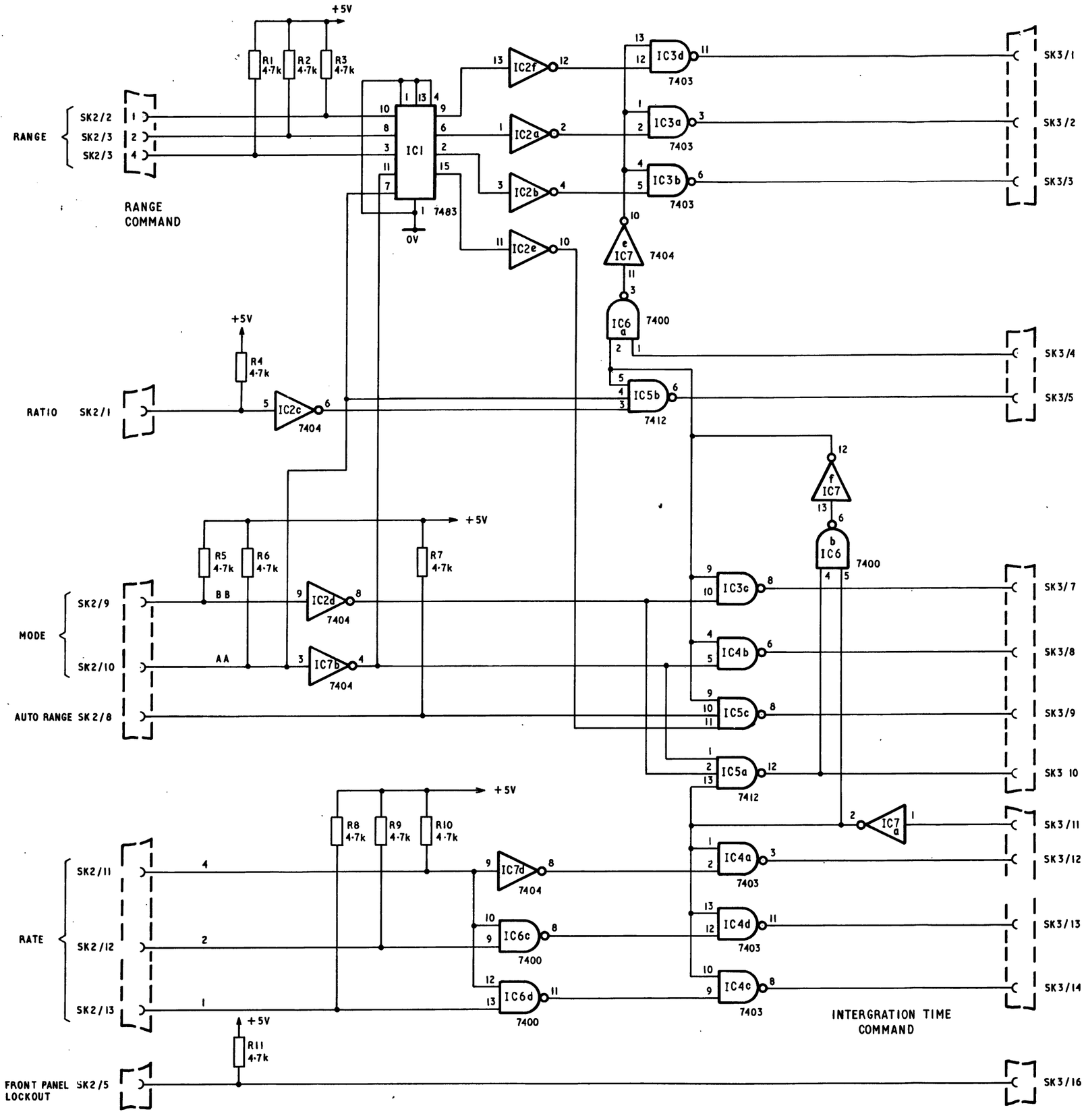
or 2. in Local operation when IC3c and IC4b will block commands.

RATE COMMANDS on SK2 pins 11, 12 and 13 are transmitted to the instrument via SK3 pins 12, 13 and 14 unless it is in Local operation, when the commands will be blocked by IC4 a, c and d.

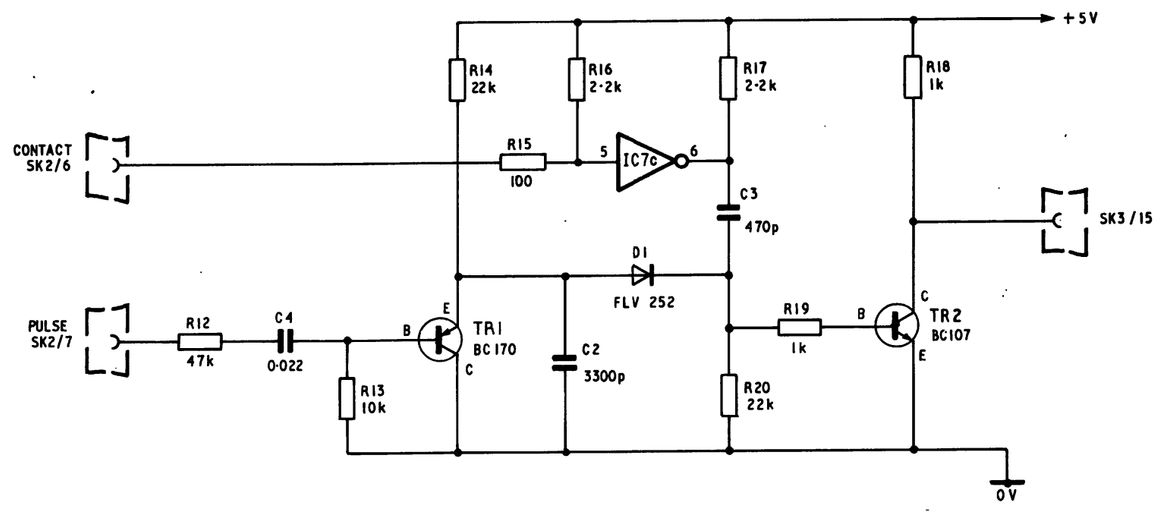
IC6c and d force code 0 on SK3 pins 12, 13 and 14 for input commands 0, 1, 2, 3. Input commands 4, 5, 6, 7 are unaffected.

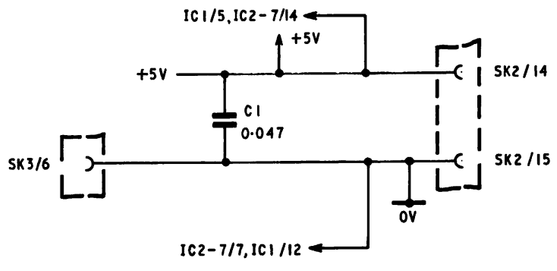
CONTACT and PULSE SAMPLES are filtered for optimum noise rejection and OR-ed together to produce a low on SK3 pin 15. The specifications for these inputs are given in this section of the manual.

← PCB 21 & 22 Notations



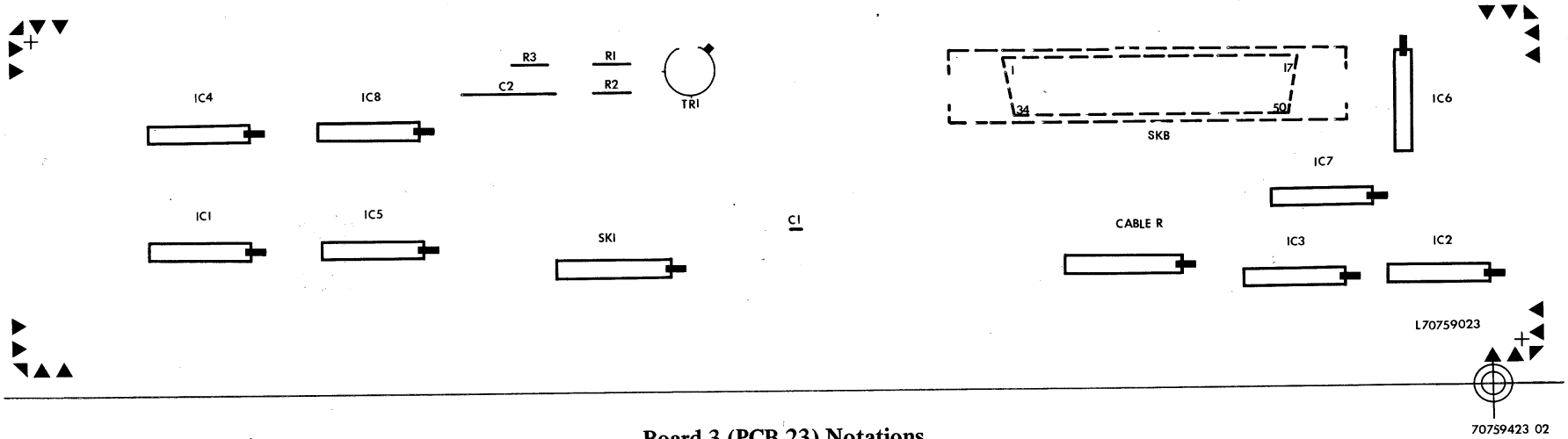
DIG COMMAND SHAPING





SK2 CONNECTS TO CABLE R ON BOARD 3
SK3 CONNECTS TO CABLE S ON BOARD 1
} 16 PIN D.I.L. SOCKETS

Board 2 Diag. 10.2



Board 3 (PCB 23) Notations

Board 3 Diag 10.3

Input Commands on SKB are passed directly to board 2 via cable R.

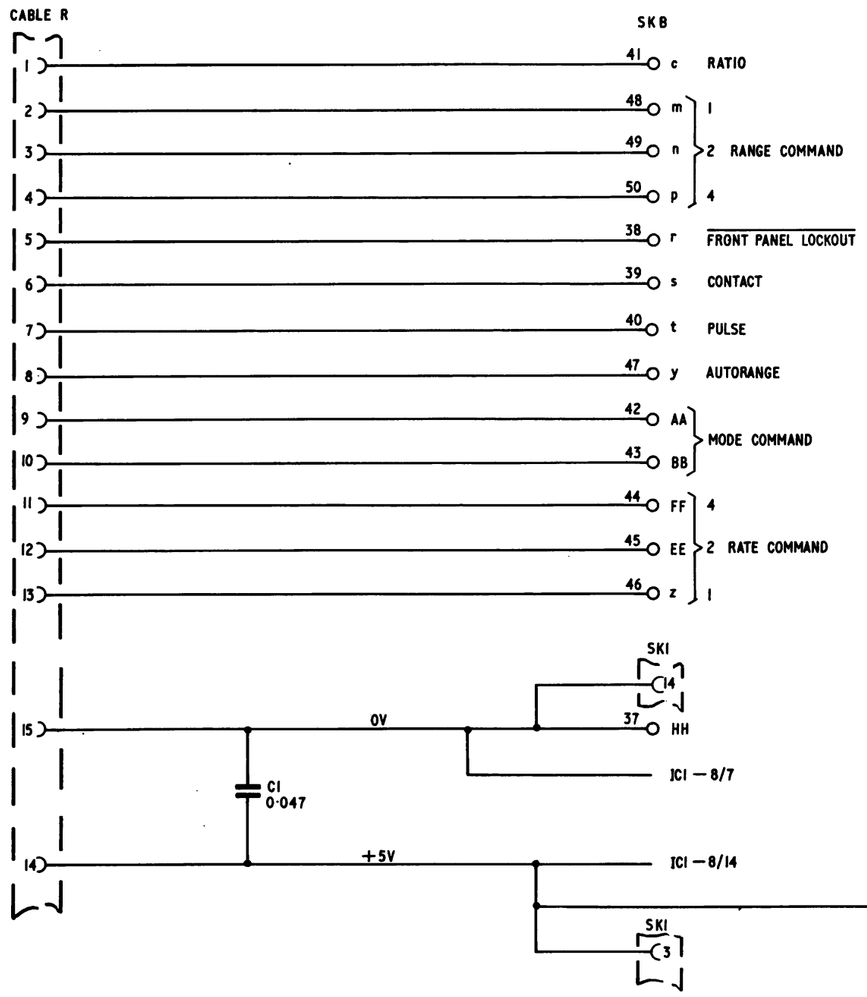
Output information from board 1 is applied directly to SKB.

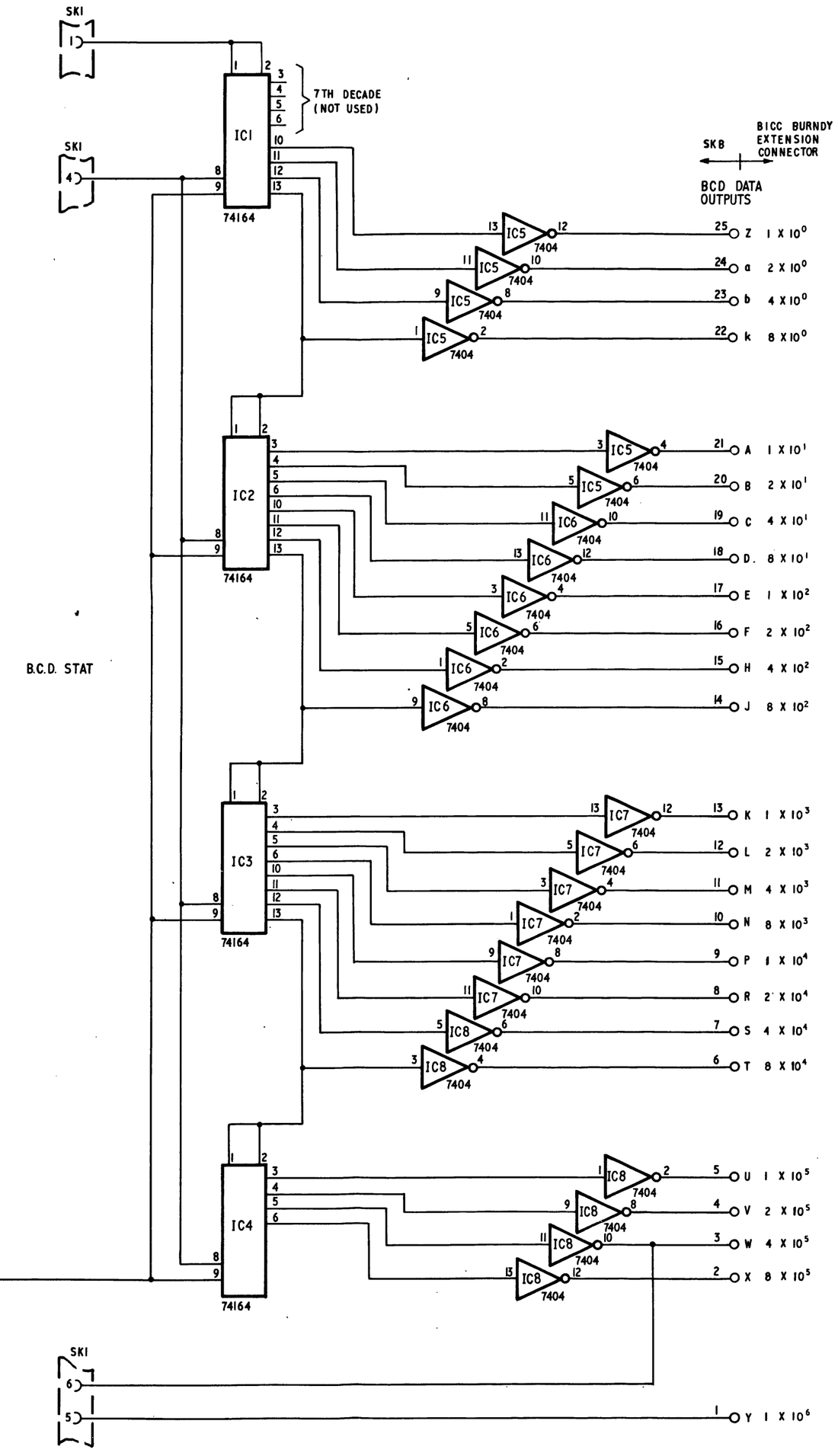
A PRINT COMMAND PULSE of 12μs duration is produced by TRI when DATA CAN CHANGE goes low.

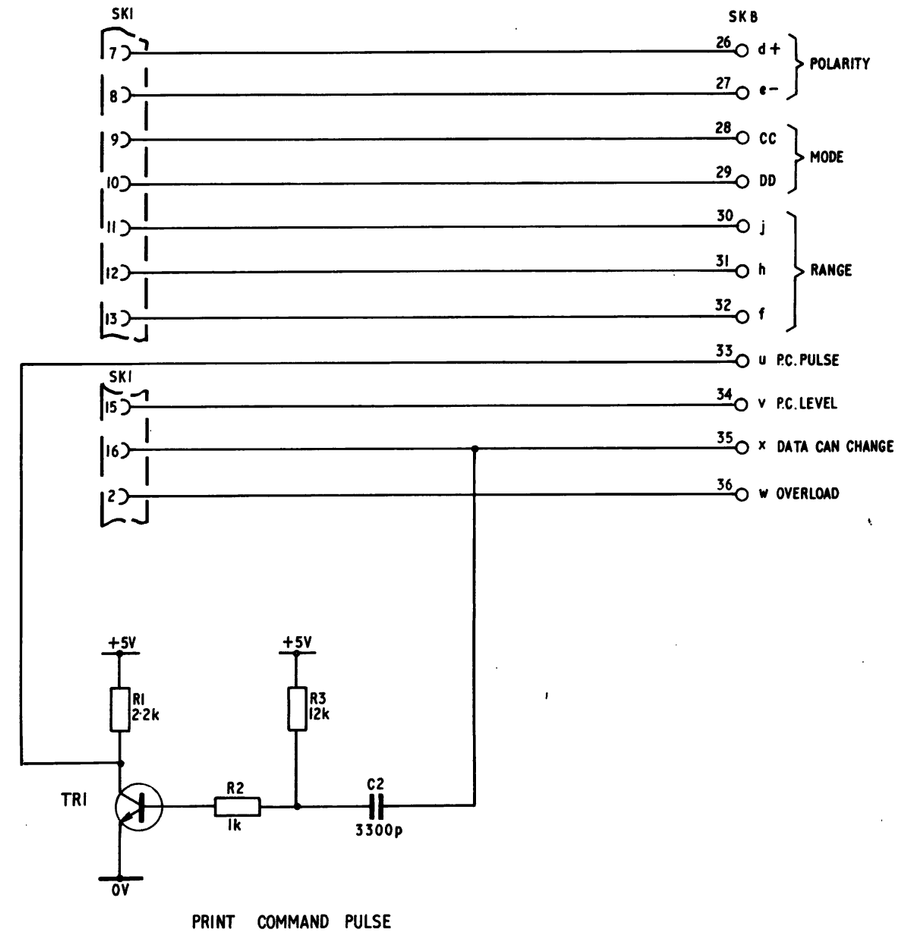
32 clock pulses are applied to the clock inputs of shift registers IC's 1 to 4 at 800 kHZ while the serial information is applied to ICI pins 1 and 2. The transfer lasts for 40μs. IC's 5 to 8 invert and buffer the outputs.

Note. Current jumper lead notations refer to modules ser no 000161 onwards. On modules prior to this serial number:
Cable R was annotated T.
Cable S was annotated R.
Cable T was annotated S.

PCB 23 Notations ←







CABLE R CONNECTS TO SK2 ON BOARD 2
SKI CONNECTS TO CABLE T ON BOARD 1
SKB CONNECTS TO EXTENSION BICC— BURNDY CONNECTOR

Board 3 Diag. 10.3

Component Parts Lists

PCB 21

Cct. Ref.	General Description				Solartron Part No.
R1	CACP	4.7k	1/4W	10%	172034700
R2	CACP	3.3k	1/4W	10%	172033300
R3	CACP	4.7k	1/4W	10%	172034700
R4	CACP	3.3k	1/4W	10%	172033300
R5	CACP	4.7k	1/4W	10%	172034700
C1	CERM	0.047	25V	+50% −20%	241944700
C2	CERM	0.047	25V	+50% −20%	241944700
C3	CERM	470p	500V	+50% −20%	241324700
IC1	SN7402N				510000270
IC2	SN7404N				510000410
IC3	SN74164N				510001150
IC4	SN7483N				510000840
IC5	SN74151N				510000850
IC6	SN7474N				510000490
IC7	SN7405N				510002080
IC8	SN7486N				510000650
IC9	SN7410N				510000420
IC10	SN7402N				510000270
PLA	50 way Cannon Plug DD-50P-OL1				

PCB 22

Cct. Ref.	General Description				Solartron Part No.
R1 to R12	CACP	4.7k	1/4W	10%	172034700
R13	CACP	10k	1/4W	10%	172041000
R14	CACP	2.2k	1/4W	10%	172032200
R15	CACP	100	1/4W	10%	172021000
R16	CACP	2.2k	1/4W	10%	172032200
R17	CACP	2.2k	1/4W	10%	172032200
R18	CACP	1k	1/4W	10%	172031000
R19	CACP	1k	1/4W	10%	172031000
R20	CACP	2.2k	1/4W	10%	172032200
C1	CERM	0.047	25V	+50% −20%	241944700
C2	ESTF	3300p	160V	10%	222333300
C3	CERM	470p	500V	+50% −20%	241324700
C4	ESTF	0.022	100V	10%	225442200
D1	LED	FLV252			300750090
TR1	BCY70				300553590
TR2	BC107				300553320
IC1	SN7483N				510000840
IC2	SN7404N				510000410
IC3	SN7403N				510001200
IC4	SN7403N				510001200
IC5	SN7412N				510002090
IC6	SN7400N				510000340
IC7	SN7404N				510000410
SK2	16 pin DIL				300584860
SK3	16 pin DIL				300584860

PCB 23

Cct. Ref.	General Description				Solartron Part No.
R1	CACP	2.2k	1/4W	10%	172032200
R2	CACP	1k	1/4W	10%	172031000
R3	CACP	12k	1/4W	10%	172041200
C1	CERM	0.047	25V	+50% −20%	241944700
C2	ESTF	3300p	160V	10%	222333300
TR1	BC107				300553320
IC1 to IC4	SN74164N				510001150
IC5 to IC8	SN7404N				510000410
SK1	16 pin DIL				300584860
SKB	50-way Cannon				352550110

SECTION 11 GP-IB Interface 70755

This Section contains technical information on the 70755 GP-IB Interface Unit, as follows:

Associated publications

70755 Interface Operating Manual (Part No. 70750012)

PlusBus – the Solartron GP-IB

INTRODUCTION

The 70755 GP-IB Interface Unit permits data interchange between the 7075 dvm and any suitable device connected to a GP-IB (General Purpose Interface Bus). The Interface is designed to meet the IEC TC66 Byte-serial Bit-parallel GP-IB system.

The Interface fits at the rear of the 7075 dvm and derives its power (5V supply) from the dvm.

The Interface has 2 external connectors: a 50way Cannon plug which mates directly with SK1 (fan-out connector) at the rear of the dvm and a 25way Cannon D-type plug which accepts a connector fitted to the GP-IB.

The 70755 circuitry is contained on three pcb's interconnected by two 16way ribbon (Scotchflex) cables which carry the internal bus signals. The Interface is microprocessor controlled.

The Simplified Block Diagram (Fig. 11.1) shows the interconnections between the pcb's and provides reference to the relevant circuit diagrams (Figs. 11.3, 11.4, 11.5). Circuit descriptions are shown adjacent to the circuit diagrams. The MPU (Microprocessor Unit) is described briefly in the pcb 32 circuit description. Three PIA's (Peripheral Interface Adaptors) are used in the interface; the PIA is briefly described on page 11.12.

Before attempting to dismantle or re-assemble the 70755 (i.e. for fault finding) the instructions given on page 11.16 should be read.

The three pcb's in the Interface 70750531, 70750532 and 70750535 are, for simplicity, referred to as PCB 31, 32 and 35 respectively.

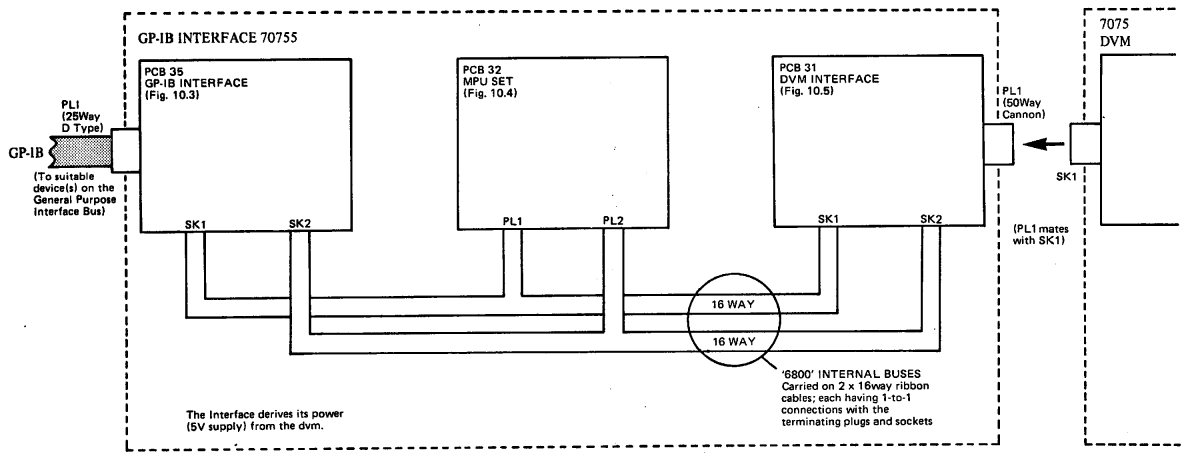


Fig. 11.1 GP-IB Interface 70755: Simplified Block Diagram

PCB 32, MPU SET: Circuit description

This pcb contains the MPU set and associated circuitry which control the overall flow of data, address and control signals between GP-IB and the 7075 dvm.

PCB 32 contains the following circuit elements;

- MPU (Microprocessor Unit) IC1
- Two 128 x 8 bit RAM's (Random Access Memory) IC2, IC13
- Three pairs of 1024 x 4 bit ROM's (Read Only Memory) IC9, 10, IC11, 12, IC14, 15
- Clocks generator IC3, TR1-4
- Address decoders IC4, IC5
- Power-up/reset generator TR8, 9, IC8
- Vcc Switches TR5-7

A simplified block diagram of PCB32 is shown in Fig. 11.2. The circuit diagram is shown in Fig. 11.3

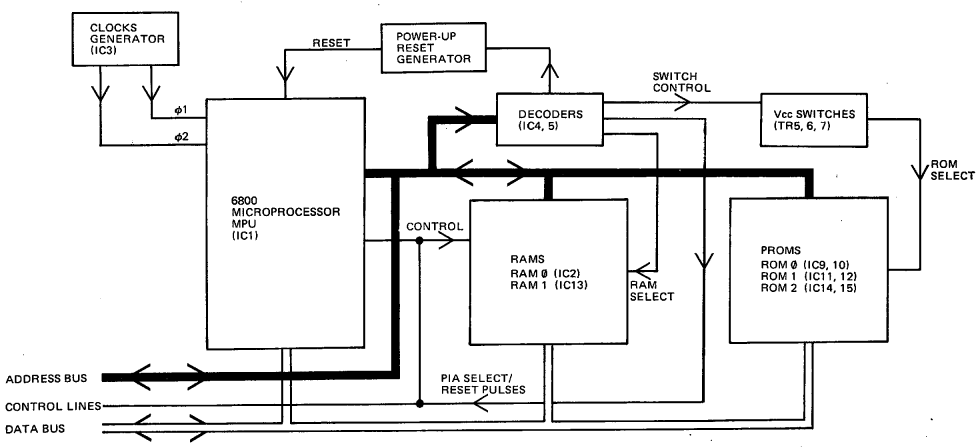
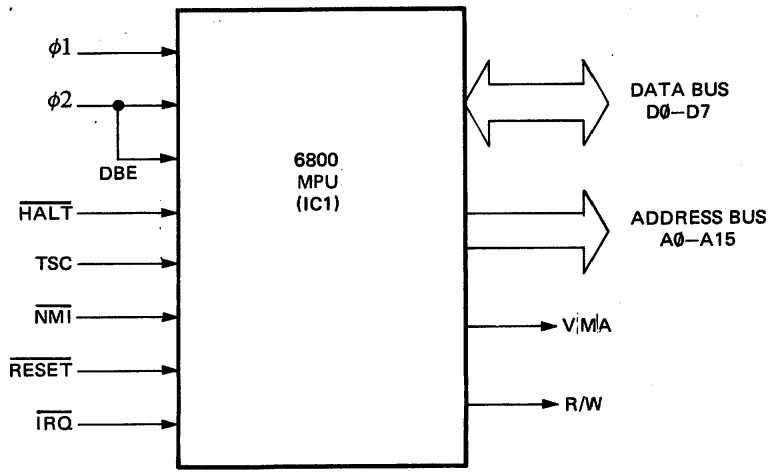


Fig. 11.2 PCB 32, MPU SET : Simplified Block Diagram

The overall timing of MPU action is controlled by the two-phase clock generator (IC3, TR1-4). The outputs from multivibrator IC3 are fed via gating to pulse-shapers/buffers TR1-4. The resulting outputs are 2 non-overlapping clock signals $\phi 1$ and $\phi 2$, the frequency of each is 1MHz. The gating, IC16, is designed for special test purposes using an EXORCISOR (Motorola Development System) and USE (User System Emulator).

The MPU (Microprocessor Unit)

The 6800 MPU is an eight-bit parallel device having an address capability of 64k words. The various inputs and outputs are briefly described below.



DØ–D7 : 8 line bi-directional Data Bus
AØ–A15 : 16 line Address Bus, used to specify ROM/RAM and PIA memory locations.

Controlling Signals

φ1 φ2 : Inputs derived from the 2 phase clock, used for overall timing of MPU action. φ2 is also used as a data transfer synchronising signal.

$\overline{\text{RESET}}$: Input from the 'Power Up' circuit, used to reset and start when power is first applied ($\overline{\text{RESET}}$ is also routed to the PIA's)

$\overline{\text{IRQ}}$: Interrupt Request input from the PIA's, notifying the MPU of a request for service.

$\overline{\text{NMI}}$: Non-Maskable Interrupt input, similar to $\overline{\text{IRQ}}$ except that NMI will always be serviced regardless of the state of the programmable interrupt mask contained in the MPU (i.e. higher priority than $\overline{\text{IRQ}}$)

R/W : Read/Write output indicating that MPU is reading or writing data on the Data Bus. (Read = 1, Write = 0)

VMA : Valid Memory Address output indicating that a valid address is on the address bus.

DBE : Data Bus Enable input, derived from the φ2 clock, enabling the Data Bus.

TSC : Three State Control input, being held permanently 'low', maintains the Address Bus and R/W line in an enabled state.

$\overline{\text{HALT}}$: Halt input, being held permanently 'high', enables MPU operation.

Table 11.1 MPU Addressing Codes

LOCATION	ADDRESS												ADDRESS RANGE (HEX)
	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	AØ	
PIA 1 (IC6 pcb 35)	Ø	Ø	·	Ø	Ø	·	·	·	Ø	Ø	X	X	ØØØØ–ØØØ3
PIA 2 (IC2 pcb 31)	Ø	Ø	·	Ø	Ø	·	·	·	Ø	1	X	X	ØØØ4–ØØØ7
PIA 3 (IC3 pcb 31)	Ø	Ø	·	Ø	Ø	·	·	·	1	Ø	X	X	ØØØ8–ØØØB
RAM Ø (IC2)	Ø	Ø	·	Ø	1	X	X	X	X	X	X	X	8Ø–FF
RAM 1 (IC13)	Ø	Ø	·	1	Ø	X	X	X	X	X	X	X	1ØØ–17F
RESET Ø (see below)	Ø	Ø	·	1	1	Ø	Ø	Ø	·	·	·	·	18Ø
RESET 1 (see below)	Ø	Ø	·	1	1	Ø	Ø	1	·	·	·	·	19Ø
RESET 2 (see below)	Ø	Ø	·	1	1	Ø	1	Ø	·	·	·	·	1AØ
RESET 3 (see below)	Ø	Ø	·	1	1	Ø	1	1	·	·	·	·	1BØ
RESET 4 (see below)	Ø	Ø	·	1	1	1	Ø	Ø	·	·	·	·	1CØ
ROM Ø (IC9/10)	Ø	1	X	X	X	X	X	X	X	X	X	X	1400–17FF †
ROM 1 (IC11/12)	1	Ø	X	X	X	X	X	X	X	X	X	X	1800–1BFF †
ROM 2 (IC14/15)	1	1	X	X	X	X	X	X	X	X	X	X	1C00–1FFF †

· not decoded
X contains either '1' or 'Ø'
Ø decodes 'Ø'
1 decodes '1'

† Assumes A12 is a '1' in the program, to aid debugging. There is no need to decode A12.

RESET pulses: These are 1 μs wide negative-going pulses used to access a particular location.

RESET Ø is used to reset the 'FORCE' bistable (IC 12 pins 1–6, on pcb 35) after an ATN change has occurred on the GP-IB

RESET 1 is used to reset the $\overline{\text{REN}}$ bistable (IC 8 pins 1–6, on pcb 35) after the MPU has processed its change.

RESET 2 is used to set the LLO bistable (IC 13 on pcb 35) after receipt of the LLO command from the GP-IB

RESET 3 not used

RESET 4 is the Power-up Inhibit signal. This is generated at regular intervals when the MPU is functioning correctly. The repetition rate of this signal will vary according to the part of the program being implemented.

R/W (Read/Write) Addressing: Read = 1, Write = 0

The MPU sequentially addresses locations in the PROM's (via the Address Bus A∅–A11) and fetches program instructions (via the Data Bus D∅–D7) held in the PROM's. The RAM's are used as a scratch-pad memory, holding data until required. The MPU addresses various locations in the PIA's, RAM's and ROM's (see Table 11.1) and effects data transfer between these circuit elements.

The MPU can modify its sequence of addresses on the basis of results of previous operations. When interrupted (by $\overline{IRQ}$) the MPU can store its present state and continue from where the program left off when the interrupt cycle is finished.

Part of the address from the MPU causes the Decoders (IC4, 5) to generate the following signals:

chip select (CS1), to enable the RAM's
$\overline{PIA}$, to enable IC6 on pcb 35 and IC2, 3 on pcb 31.
Vcc Switch drive, enabling pairs of PROM's
$\overline{RESET}$ ∅, 1, 2 and 3, resetting the set/reset bistables on pcb 35
Power-up Inhibit, to input of the Power-up Reset Generator

When the MPU is running normally the Power-up Inhibit pulses to TR8 (Power-up Reset Generator) inhibit the oscillator TR9/IC8 (pins 1-6). At power-up, or in the case of a fault condition (i.e. the MPU is not producing Power-up Inhibit pulses), the oscillator runs and produces $\overline{RESET}$ pulses thus resetting the MPU (and the PIA's on pcb 31 and 35).

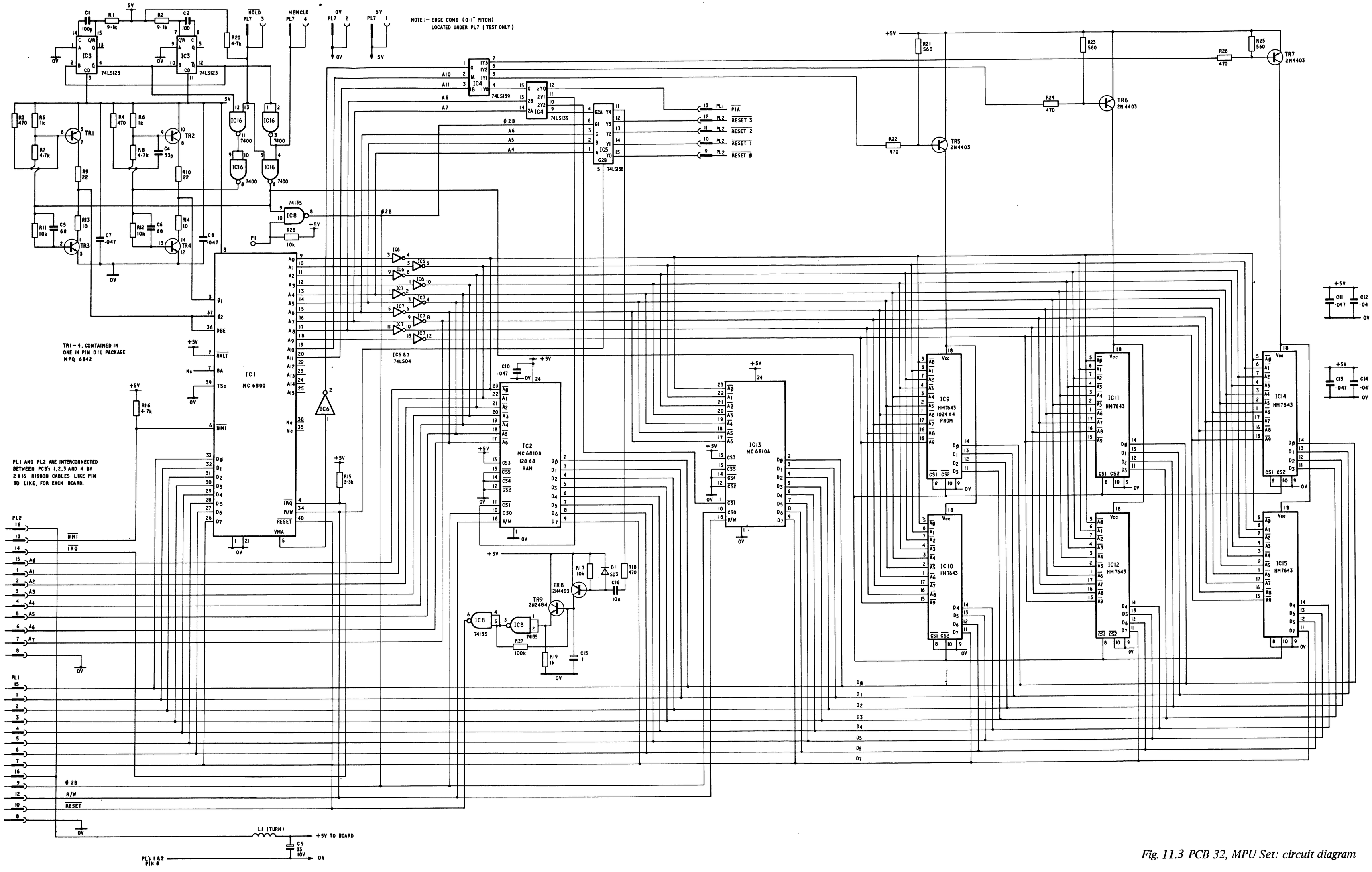


Fig. 11.3 PCB 32, MPU Set: circuit diagram

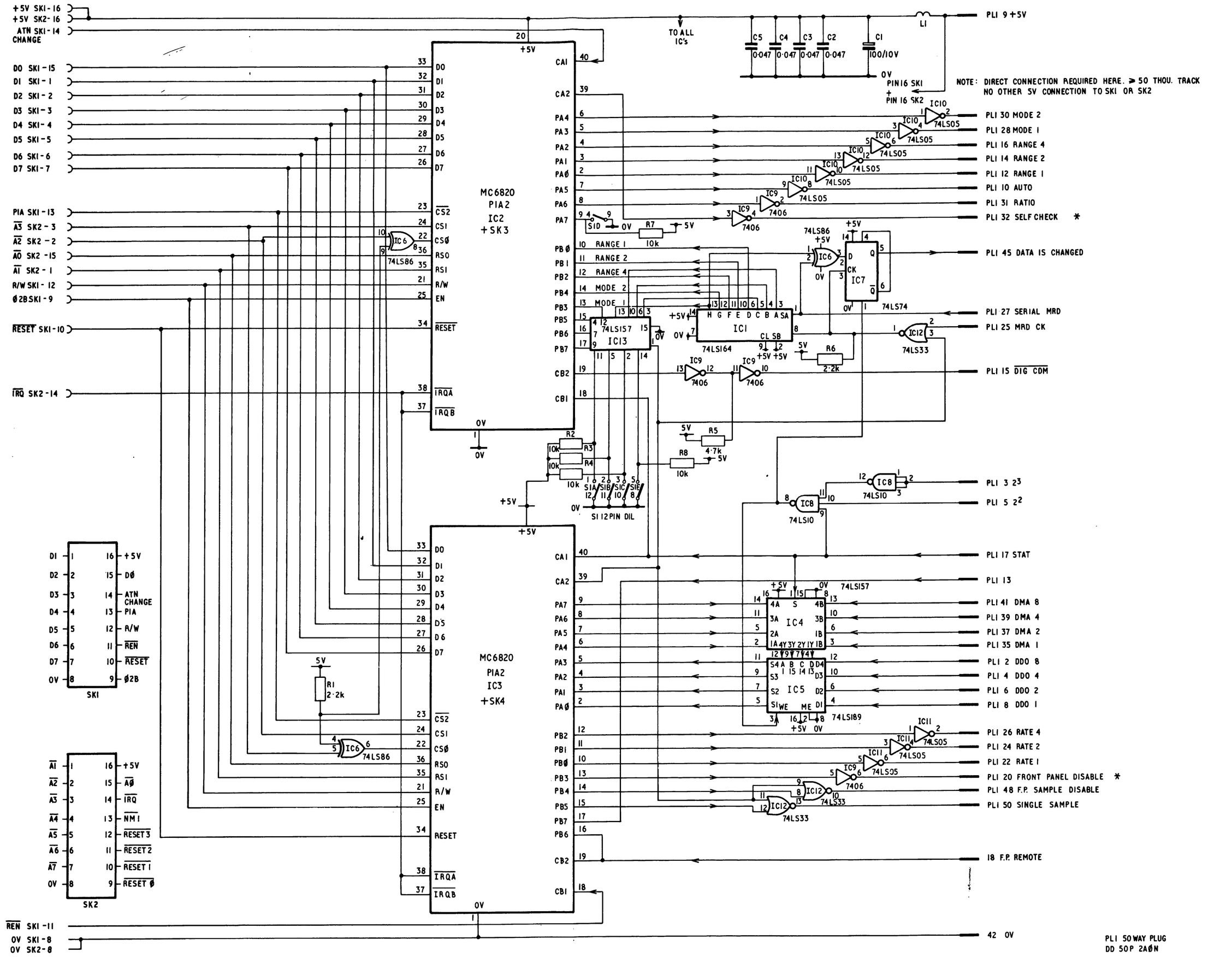


Fig. 11.4 PCB 31, DVM Interface : circuit diagram

PCB 31, DVM INTERFACE: Circuit description

This pcb interfaces the dvm (at PL1) with the '6800' Internal Buses (at SK1 and 2). Data, address and control signals from the Buses are routed to the 2 PIA's (IC2 and 3). PIA information is shown on page 11.12.

The PAØ–PA7 outputs from IC2 provide controlling signals for the dvm. The Digitise Command signal ($\overline{\text{DIG CMD}}$), derived from CB2 IC2, is sent after the PAØ–PA7 signals. Serial Mode Range Data (MRD) from the dvm is clocked into the 8 bit shift register IC1 using the gated MRD CK signal.

The MRD is then presented to the PBØ–PB7 terminals on IC2 in parallel form, the A, B, C and H inputs being multiplexed (in IC13) with levels obtained from the preset delimiting switches SW1a, b, c and e. IC13 is switched by the CA2 signal from IC3; 'O' selects the delimiting inputs, '1' selects the shift register inputs. IC6, pins 1 and 2, compare the present MRD with the previous MRD in the shift register. If the signals differ a DATA IS CHANGED signal is produced at IC7 Q output. This is output to the dvm to provide a longer time between measurements, required for processing, whenever the data has changed.

The sampled (measurement) data is output from the dvm and appears, in BCD form, at the DD1, 2, 4, 8 inputs; each digit is addressed by the DMA1, 2, 4, 8 signals and strobed by the 2^2, 2^3 clock signals. When STAT is high the address signals are multiplexed through IC4, to IC5 (a 16 X 4 bit store) and the sampled data digits are loaded into the store. Subsequently the data from IC5 is read by the MPU (on pcb 32) via the PIA, IC3. The digit address from IC3 (PA4–7) is multiplexed through IC4 while the STAT line is low.

The PBØ–PB5 outputs from IC3 provide controlling signals to the dvm.

PCB 35, GP-IB INTERFACE: Circuit description

This pcb interfaces the GP-IB (at PL1) with the '6800' Internal Buses (at SK1 and 2). Data, address and control signals are passed between the GP-IB and the Buses via transceivers, gating and the PIA, IC6 (PIA information is shown on page 11.12).

IC1, 2, 3 and 4 are quad transceivers which effect transmit/receive mode at the GP-IB. Data is always enabled through IC1, 2, 3 and 4 in the receive mode (i.e. incoming data at pins 2, 7, 15 and 9 appears on pins 3, 6, 14 and 10.) The transmit mode is enabled when the enable input (pin 12) is at a '0' (i.e. outgoing data at pins 4, 5, 13 and 11 appears on pins 2, 7, 15 and 9).

The tri-state buffers in IC5 are enabled, via gating, by the TALK signal from IC6, CB2 output.

IC14 is a parity generator which monitors the data on inputs A–H and, according to the switch settings of SW2, generates an odd/even parity bit for output to the GP-IB.

IC7 is a multiplexer which outputs data (on pins 4, 7, 9 and 12) from either the GP-IB input (on pins 2, 5, 11 and 14) or the SW1 levels (at pins 3, 6, 10 and 13). IC7, having a 3-state output, is controlled by the Control input (pin 15) and the Select input (pin 1).

The PAØ–PA7 ports of IC6 are used for bi-directional data flow. The PBØ–PB7 ports are used for sending or receiving control signals.

IC13 forms a set/reset bistable which is used to store the LLO (Local Lockout) state. IC8 (pins 1–6) forms a similar bistable which is used to latch the $\overline{\text{REN}}$ ($\overline{\text{Remote Enable}}$) signal.

The ATN signal from the controller on the GP-IB is received via IC4 at IC6, CA1 input. The ATN signal is compared with the MPU ATN signal (output from IC6 CA2) at IC9 (pins 1–3). If the signals differ the bistable IC12 (pins 1–6) latches and an ATN CHANGE (Attention change) signal is produced indicating that the GP-IB control mode has changed.
GP-IB ATN line = 0 indicates that control or address information is present on the data bus.
GP-IB ATN line = 1 (i.e. $\overline{\text{ATN}}$) indicates that data is present on the data bus.
N.B. All GP-IB signals are negative logic.

The output from bistable IC12 is buffered by IC10 to produce a $\overline{\text{FORCE}}$ signal at IC6, PB1. $\overline{\text{FORCE}}$ is used to suspend GP-IB message transfers until the MPU has actioned the ATN mode change.

TR1, R6 and C8 form a delay circuit which inhibits the IFC signal (from the GP-IB) and so delays the $\overline{\text{NMI}}$ output for 10ms after a power up $\overline{\text{RESET}}$ signal. This allows the MPU time to complete its power-up sequence without interruption.

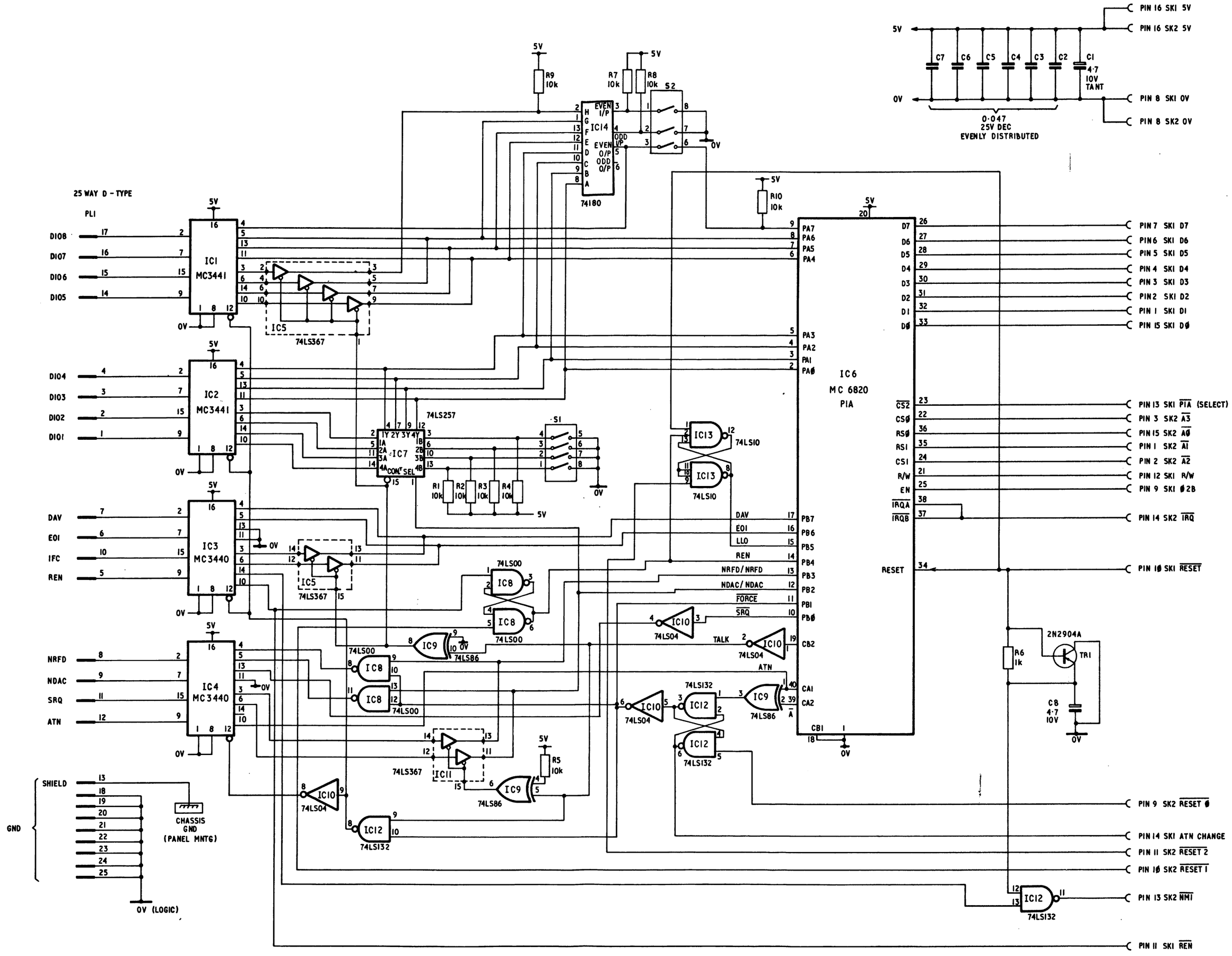
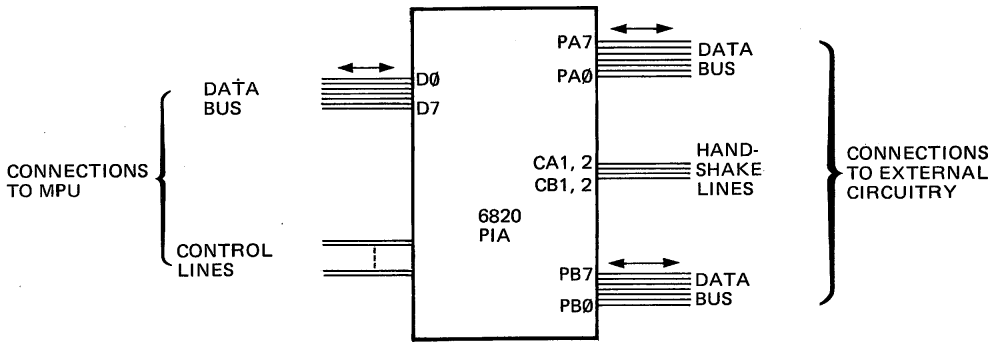


Fig. 11.5 PCB 35, GP-IB Interface: circuit diagram

The 6820 PIA (Peripheral Interface Adaptor)

Three 6820 PIA's are used in the 70755: PIA1 (IC6) on pcb 35, PIA2 and 3 (IC2 and 3) on pcb 31. The PIA's enable the MPU to interface with external circuitry (i.e. the 7075 and the GP-IB devices). Each PIA is basically a read/write memory having 4 memory locations. The MPU–PIA connections consist of 8 bi-directional data lines (DØ–D7) and various control lines. The PIA–external circuitry connections consist of two 8-wire bi-directional data buses (PAØ–PA7 and PBØ–PB7) and handshake lines, see simplified diagram below.



The connections to the PIA are briefly described below

MPU–PIA

DØ–D7 : An 8-line bi-directional data bus

CS0, CS1, CS2 : 'Chip Select' inputs for selecting a particular PIA.

RS0, RS1 : 'Register Select' inputs for selecting a specific register in the PIA.

R/W : Read/Write input, enabling the MPU to control the direction of data flow (R/W = 1 = Read, R/W = 0 = Write).

EN : Enable input accepts the ϕ2B clock signal from the clock generator, this synchronises data read/write. (Data transfer takes place during the ϕ2 portion of the clock cycle).

$\overline{\text{RESET}}$: Reset input accepts signals from the Power-Up circuit, when power is first applied or if erroneous pulses occur. This input resets the internal registers in the PIA to their initial values.

$\overline{\text{IRQA/B}}$: Interrupt request outputs which enable the PIA to interrupt the MPU when necessary.

PIA – external device

PAØ–PA7, PBØ–PB7 : Two 8-wire bi-directional data buses.

CA1, CB1 CA2, CB2 : Handshake lines which accept inputs to control the IRQA/B interrupt request lines. Additionally CA2, CB2 may be used as peripheral control outputs.

SERVICING

The 70755 circuitry consists essentially of MOS and TTL components, there are no pre-set potentiometers or pre-set resistors. Servicing as such is therefore not required but if a fault develops then fault diagnosis and rectification will be necessary.
Caution: Exercise care when handling the MOS integrated circuits as static electricity can damage these devices.

FAULT DIAGNOSIS

The following fundamental checks (Tests 1–5) should first be carried out when attempting to ascertain the faulty component(s). Reference should also be made to the circuit diagrams and descriptions. Prior to fault diagnosis the 70755 should be dismantled as described on page 11.16
Caution: *Changing the ROM's (IC9–12, 14 and 15 on pcb 32). If any of the 6 ROM's are removed they must be replaced strictly in their original positions. Replacement ROM's are obtainable only from Solartron (each ROM is programmed 'in-house'); no other ROM's should be fitted. (See Parts List, page 11.19.)*

1. Checking the supply voltage

Equipment required: AVO or similar

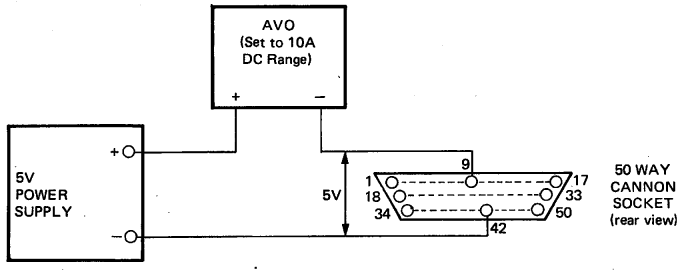
1.1 Disconnect the GP-IB from the 70755.
Fit the 70755 to the dvm and switch on.

1.2 Using the AVO measure the +5V supply (to the 70755 from the dvm) at PL1; PL1 pin 9 = +5V, PL1 pin 42 = 0V. The measured voltage must be 5V ± 0.25V.
Switch off the dvm.

2. Checking the current consumption

Equipment required: 5V DC Power Supply (1.5A capability)
AVO or similar
50-way Cannon socket

2.1 Connect the Power Supply, AVO and Cannon socket as shown below. Set the AVO to 10A DC range.



2.2 Disconnect the 70755 from the dvm. Connect the 50 way Cannon socket to PL1 on the 70755.

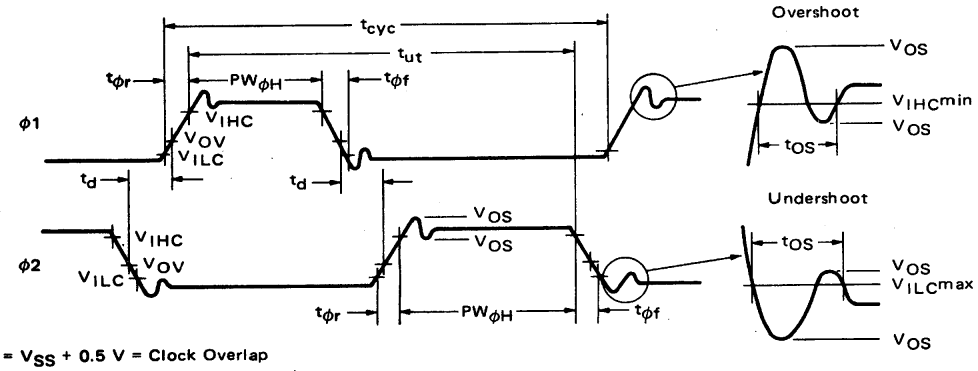
2.3 Switch on the Power Supply and note the AVO reading. The current indication must be <1.1A. If the current is greater than 1.1A a fault is indicated; this must be rectified before reconnecting the 70755 to the dvm.

2.4 Switch off the Power Supply, disconnect the Cannon socket and reconnect the 70755 to the dvm.

3 Checking the MPU clock signals (PCB 32)

Equipment required: Dual beam oscilloscope.

3.1 Switch on the dvm. Using the oscilloscope monitor the MPU clock signals $\phi 1$ and $\phi 2$ at IC1, pins 3 and 37 respectively (pcb 32). The signals should satisfy the following specification. Switch off the dvm.



$V_{OV} = V_{SS} + 0.5\ V$ = Clock Overlap measurement point

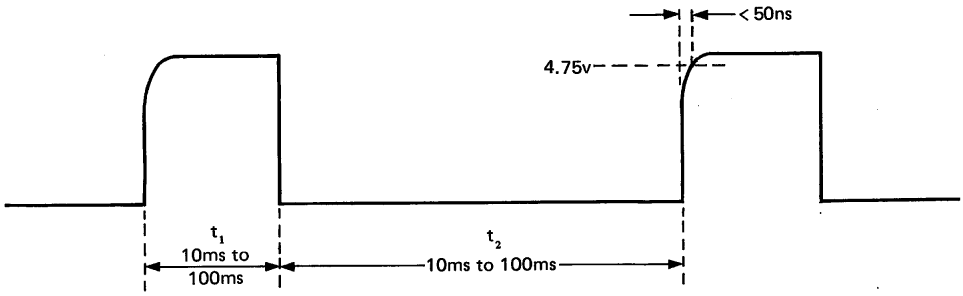
ABBREVIATION	PARAMETER	VALUE min	VALUE max	
t_{cyc}	Cycle Time	1.0	1.1	μs
$PW_{\phi H}$	Clock Pulse Width (Measured at V_{cc} –0.3V)			
	$\phi 1$	430	435	ns
	$\phi 2$	450	455	ns
t_{ut}	Total $\phi 1$ and $\phi 2$ Up Time	940	–	ns
$t_{\phi r}$, $t_{\phi f}$	Rise and Fall Times $\phi 1$, $\phi 2$ (Measured between V_{ss} +0.3V and V_{cc} – 0.3V)	5.0	5.5	ns
t_d	Delay Time or Clock Separation (Measured at $V_{0V} = V_{ss}$ +0.5V)	0	40	ns
t_{os}	Overshoot Duration	0	40	ns

4 Checking the Power-up Reset Generator (PCB 32)

Equipment required: Oscilloscope

4.1 With the dvm switched off, carefully remove IC1 (MPU) from pcb 32. Switch on the dvm.

4.2 Using the oscilloscope monitor the $\overline{\text{RESET}}$ signal at IC1 socket pin 40. The waveform should be as shown below. Switch off the dvm, and replace IC1.

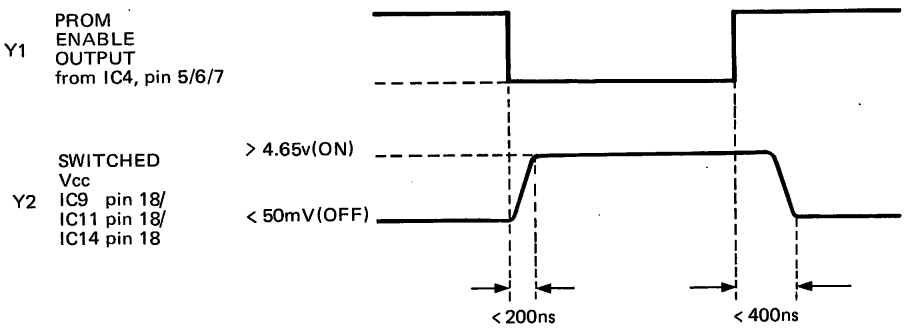


The mark-space ratio $\frac{t_1}{t_2}$ may be between 0.1 and 10

5 Checking the PROM Vcc Switching (PCB 32)

Equipment required: Dual beam oscilloscope

5.1 Switch on the dvm.
Using the dual beam oscilloscope compare the PROM Enable Output at IC4 pin 5 with the resulting Switched V_{CC} signal at IC9 pin 18. The waveforms should appear as shown below.



5.2 Repeat (5.1) for the PROM Enable Output at IC4 pin 6 and the resulting Switched Vcc signal at IC11 pin 18.

5.3 Repeat (5.1) for the PROM Enable Output at IC4 pin 7 and the resulting Switched Vcc signal at IC14 pin 18.

5.4 Switch off the dvm.

DISMANTLING AND RE-ASSEMBLY PROCEDURE

Dismantling

1. Switch off the 7075 dvm. Remove the 70755 from the dvm by releasing the 2 retaining screws.
2. Remove the 6 securing screws located on the top of the 70755. Withdraw the assembly of 3 pcb's from the case.
3. Refer to Fig. 11.6. Remove the 6 plastic caps from the underside of pcb 32 (at locations A–F) then remove the screws and washers. (This will release pcb 32 from the assembly, but it will remain connected by the ribbon cable.)
4. Using a 4BA spanner, remove the 4 hexagonal pillars from the underside of pcb 35 at locations A, B, C and E. Remove the 2 pillars from the top side of pcb 31 at location D and F. (This will release pcb 31 from pcb 35 but they will remain connected by the ribbon cable.)
5. Open out the 3 pcb's as shown in Fig. 11.7. (This permits re-connection to both dvm and GP-IB together with easy access to each side of all pcb's.)
   Note: The ribbon cable may be unplugged from pcb's 31 and 35 but it is soldered to pcb 32.
6. Carefully remove the cable guards (retained by 'W-buttons') from pcb's 31 and 35 if required, see Fig. 11.8 for location of cable guards.

Re-assembly

1. Refer to Fig. 11.8 and Fig. 11.6. Refit cable guards and 'W-buttons', to pcb's 31 and 35, if these have been removed. Refit the ribbon cables, if these have been removed, as shown in Fig. 11.8.
2. Fit together pcb's 31 and 35 by replacing the 2 hexagonal pillars on topside of pcb 31 at locations D and F, and the 4 pillars on underside of pcb 35 at locations A, B, C and E; ensure that the ribbon cables loop round as shown in Fig. 11.8.
3. Fit pcb 32 to the assembly by replacing the 6 securing screws and washers; ensure that the insulating washers are correctly fitted and that the ribbon cables loop round as shown in Fig. 3. Replace the 6 plastic caps.
4. Slide the whole assembly back into the case, ensuring that the 2 retaining screws pass through the guides on pcb 31. Replace the 6 securing screws, on top of case.

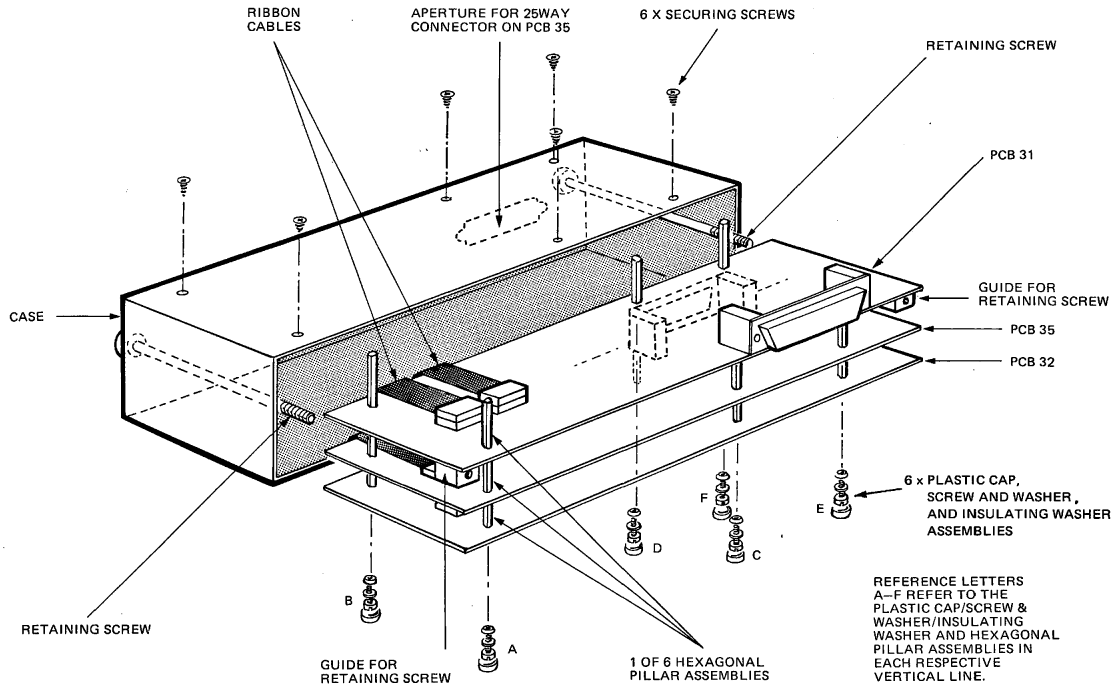
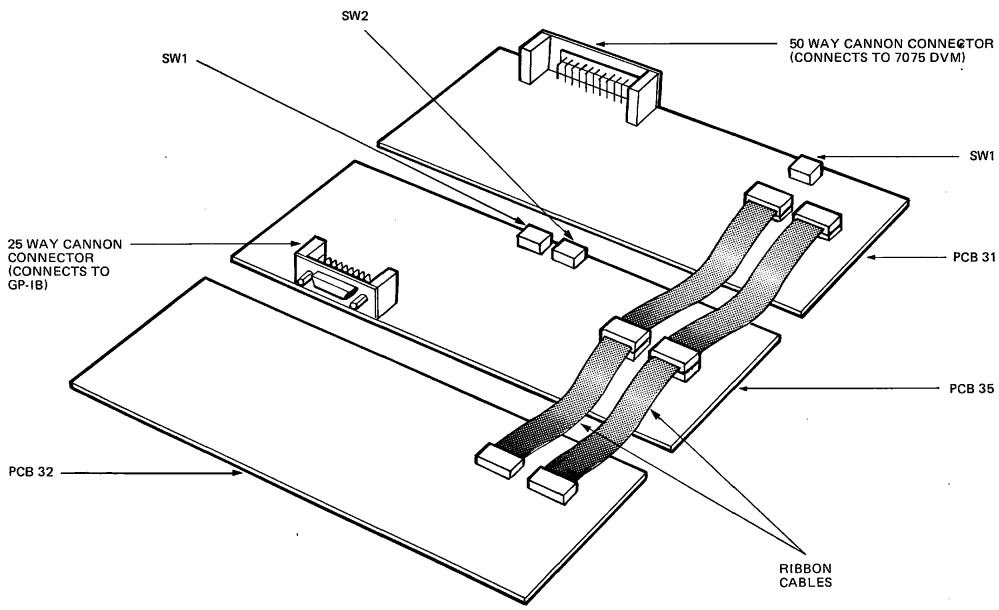


Fig. 11.6 Simplified exploded view showing pcb assembly removed from case



The settings for rocker switches (SW1 pcb 31, SW1 & 2 pcb 35) are detailed in the 70755 Operating Manual.

Fig. 11.7 Simplified view showing pcb's opened out for servicing

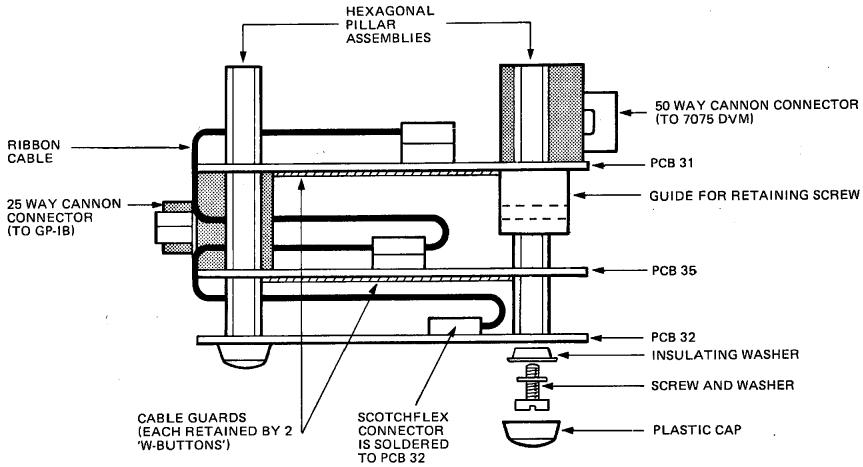
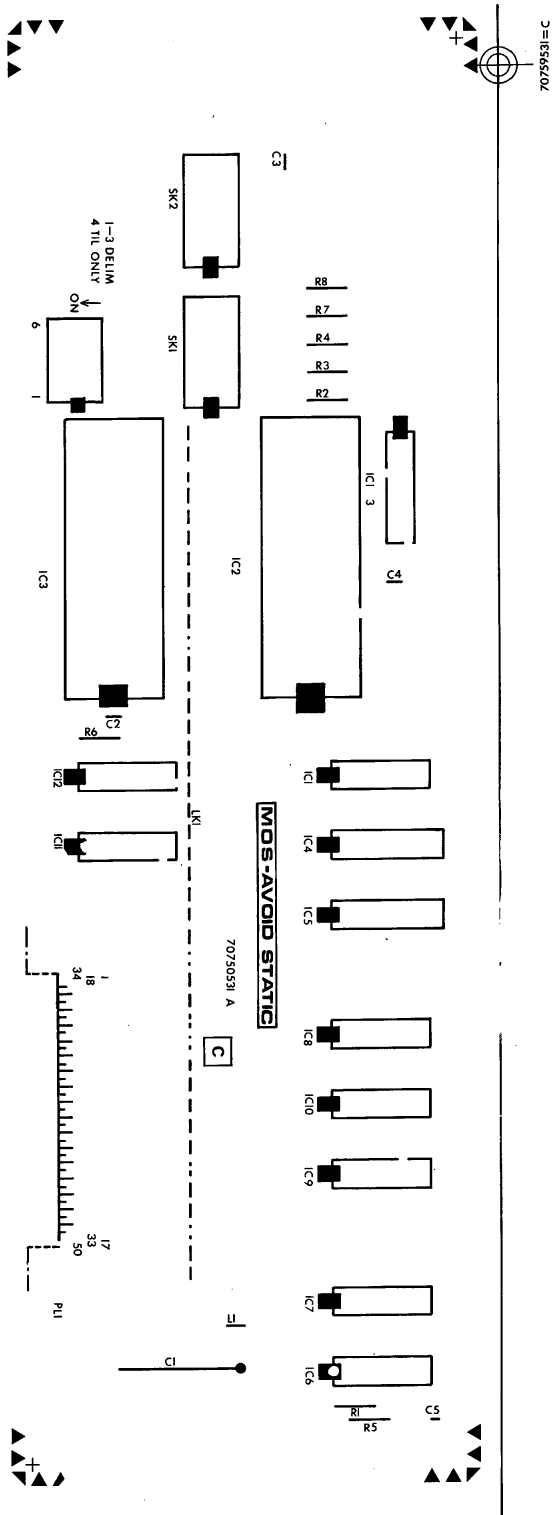


Fig. 11.8 End view of pcb assembly

PCB COMPONENT LAYOUTS AND PARTS LISTS

Component Parts List for PCB 31, DVM Interface

Cct Ref.	General Description				Solartron Part No.
R1 R2 to R4	CACP	2.2k	1/4W	±10%	172032200
	CACP	10k	1/4W	±10%	172041000
R5	CACP	4.7k	1/4W	±10%	172034700
R6	CACP	2.2k	1/4W	±10%	172032200
R7	CACP	10k	1/4W	±10%	172041000
R8	CACP	10k	1/4W	±10%	172041000
C1	TAND	100	10V	±20%	265481000
C2 to C5	CERM	0.047	25V	+50% −25%	241944700
IC1	74LS164				510002890
IC2	MC6820				510002850
IC3	MC6820				510002850
IC4	74LS157				510002240
IC5	74S189				510002840
IC6	74LS86				510002880
IC7	74LS74				510002600
IC8	74LS10				510002870
IC9	7406				510000760
IC10	74LS05				510002900
IC11	74LS05				510002900
IC12	74LS33				510002920
IC13	74LS157				510002240
PL1	50-Way Cannon				352350080
SK1	16-pin DIL socket				300584860
SK2	16-pin DIL socket				300584860
SW1	6-pole DIL switch				375000570
L1	FX1115				309010060

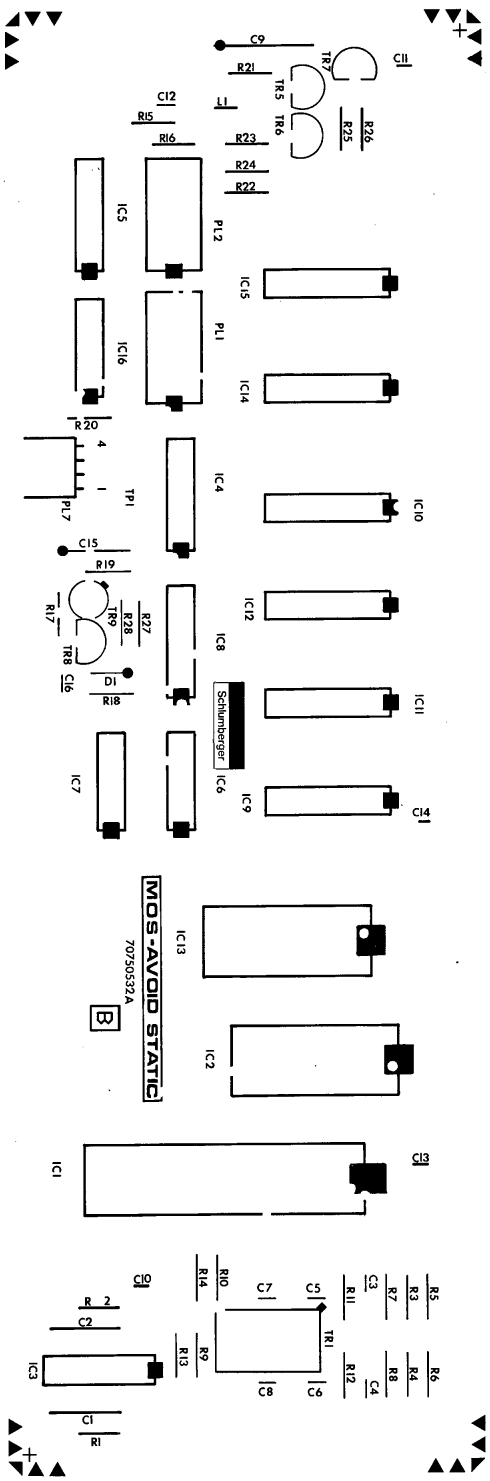


PCB 31: Component Layout

Component Parts List for PCB 32, MPU Set

Cct Ref.	General Description				Solartron Part No.
R1	MEOX	9.1k	1/4W	±0.25%	195639100
R2	MEOX	9.1k	1/4W	±0.25%	195639100
R3	CACP	470	1/4W	±10%	172024700
R4	CACP	470	1/4W	±10%	172024700
R5	CACP	1k	1/4W	±10%	172031000
R6	CACP	1k	1/4W	±10%	172031000
R7	CACP	4.7k	1/4W	±10%	172034700
R8	CACP	4.7k	1/4W	±10%	172034700
R9	CACP	22	1/4W	±10%	172012200
R10	CACP	22	1/4W	±10%	172012200
R11	CACP	10k	1/4W	±10%	172041000
R12	CACP	10k	1/4W	±10%	172041000
R13	CACP	10	1/4W	±10%	172011000
R14	CACP	10	1/4W	±10%	172011000
R15	CACP	3.3k	1/4W	±10%	172033300
R16	CACP	4.7k	1/4W	±10%	172034700
R17	CACP	10k	1/4W	±10%	172041000
R18	CACP	470	1/4W	±10%	172024700
R19	CACP	1k	1/4W	±10%	172031000
R20	CACP	4.7k	1/4W	±10%	172034700
R21	CACP	560	1/4W	±10%	172025600
R22	CACP	470	1/4W	±10%	172024700
R23	CACP	560	1/4W	±10%	172025600
R24	CACP	470	1/4W	±10%	172024700
R25	CACP	560	1/4W	±10%	172025600
R26	CACP	470	1/4W	±10%	172024700
R27	CACP	100k	1/4W	±10%	172051000
R28	CACP	10k	1/4W	±10%	172041000
C1	ESTF	100p	400V	±10%	222321000
C2	ESTF	100p	400V	±10%	222321000
C3	CERM	33p	500V	±20%	241313300
C4	CERM	33p	500V	±20%	241313300
C5	CERM	68p	500V	±20%	241316800
C6	CERM	68p	500V	±20%	241316800
C7	CERM	0.047	25V	+50% −20%	241944700
C8	CERM	0.047	25V	+50% −20%	241944700

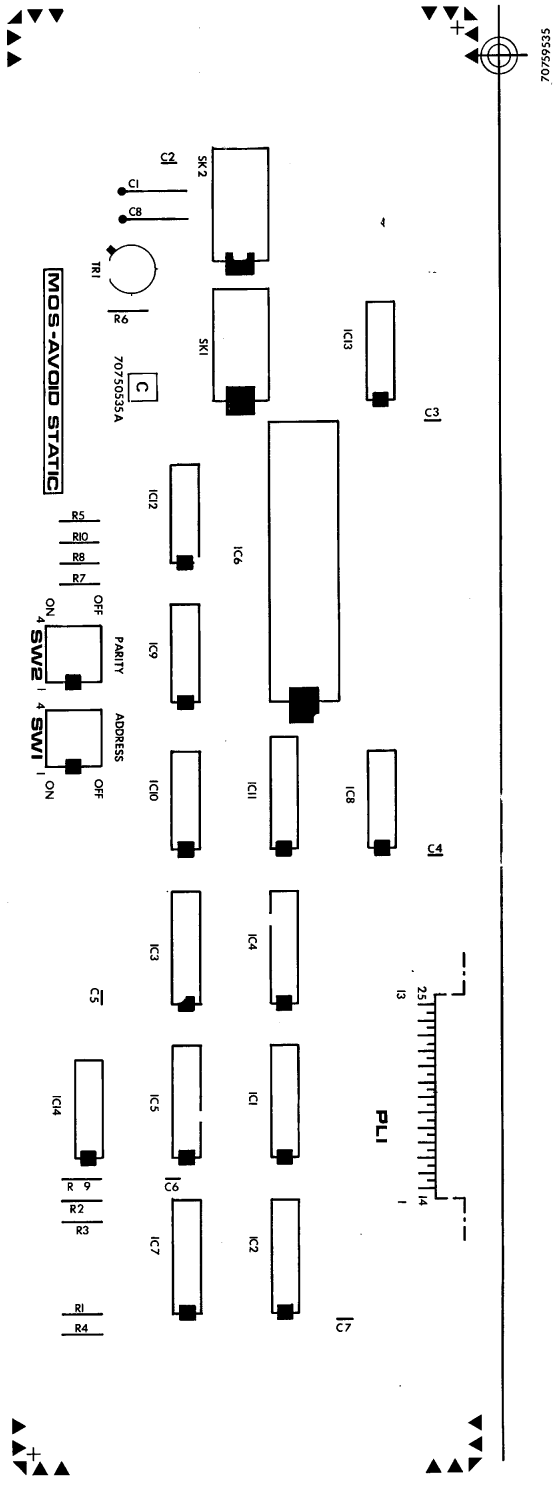
Cct Ref.	General Description				Solartron Part No.
C9	TANT	33	10V	±10%	265373300
C10 to C14	CERM	0.047	25V	+50% −20%	241944700
C15	TANT	1	35V	±20%	266061000
C16	CERM	0.01	25V	+50% −20%	241941000
D1	SD3				300522160
TR1 to TR4	MPQ6842				**30055740**
TR5 to TR8	2N 4403				300555570
TR9	2N 2484				300552860
IC1	MC6800				510002750
IC2	MC6810				510002760
IC3	74LS123				510002950
IC4	74LS139				510002960
IC5	SN74LS138				510003530
IC6	74LS04				510002690
IC7	74LS04				510002690
IC8	74135				510001430
IC9	HM7643 (Pre-programmed)				519604102
IC10	HM7643 (Pre-programmed)				519604202
IC11	HM7643 (Pre-programmed)				519604302
IC12	HM7643 (Pre-programmed)				519604402
IC13	MC6810				510002760
IC14	HM7643 (Pre-programmed)				519604502
IC15	HM7643 (Pre-programmed)				519604602
IC16	7400				510000340
PL1	16 pin DIL plug				300585040
PL2	16 pin DIL plug				300585040
PL7	Plug fixed 4-way				352304070
L1	Ferrite Bead FX1115				309010060



PCB 32: Component Layout

Component Parts List for PCB 35, GP-IB Interface

Cct Ref	General Description				Solartron Part No.
R1 to R5	CACP	10k	1/4W	±10%	172041000
R6	CACP	1k	1/4W	±10%	172031000
R7 to R10	CACP	10k	1/4W	±10%	172041000
C1	TANT	4.7	10V	±10%	265364700
C2 to C7	CERM	0.047	25V	+50% −20%	241944700
C8	TANT	4.7	10V	±10%	265364700
IC1	MC3441				510004130
IC2	MC3441				510004130
IC3	MC3440				510004120
IC4	MC3440				510004120
IC5	74LS367				510003030
IC6	MC6820				510002850
IC7	74LS257				510002990
IC8	74LS00				510002000
IC9	74LS86				510002880
IC10	74LS04				510002690
IC11	74LS367				510003030
IC12	74LS132				510002980
IC13	74LS10				510002870
IC14	74180				510004110
TR1	2N2904A				300551670
PL1	25-way Plug				352325040
SK1	16-pin DIL socket				300584860
SK2	16-pin DIL socket				300584860
SW1	4-pole DIL switch				375000550
SW2	4-pole DIL switch				375000550



PCB 35: Component Layout

GENERAL INFORMATION

The 70755 conforms to the IEC TC66 (Byte-serial, Bit-parallel) Highway specification in the following categories:

SH1	(Source Handshake)
AH1	(Acceptor Handshake)
T5	(Basic Talker, Serial Poll, Talk Only Mode, Unaddressed if MLA)
L3	(Listen only mode, Unaddressed if MTA)
TEØ	(No extended talker capability)
LEØ	(No extended listener capability)
SR1	(Service Request)
RL1	(Remote Local)
PPØ	(No Parallel Poll)
DC1	(Device Clear)
DT1	(Device Trigger)
CØ	(Not a Controller)

Power requirements: derived from 7075 dvm (5V, <1·1A)

Operating Temperature: 0°C to +50°C

Storage Temperature: −30°C to +70°C

Maximum Relative Humidity: 70% at +40°C

Dimensions: 89 x 266 x60mm (approx)

Weight: 0.88kg

APPENDIX

CONTENTS

CALIBRATION COVER 70759D

INTRODUCTION

In order to achieve the greatest accuracy during a calibration it is essential that the operating temperatures affecting circuit components are as near as possible to those experienced within the instrument case during normal operation.

The calibration cover 70759D enhances the calibration accuracy by allowing access for adjustments whilst the instrument is functioning under normal working conditions.

GENERAL DESCRIPTION

The Calibration cover is basically a normal instrument top cover with holes drilled in convenient positions allowing access to the potentiometers. Fig. A1, shows the calibration cover with the access holes and the relevant potentiometers.

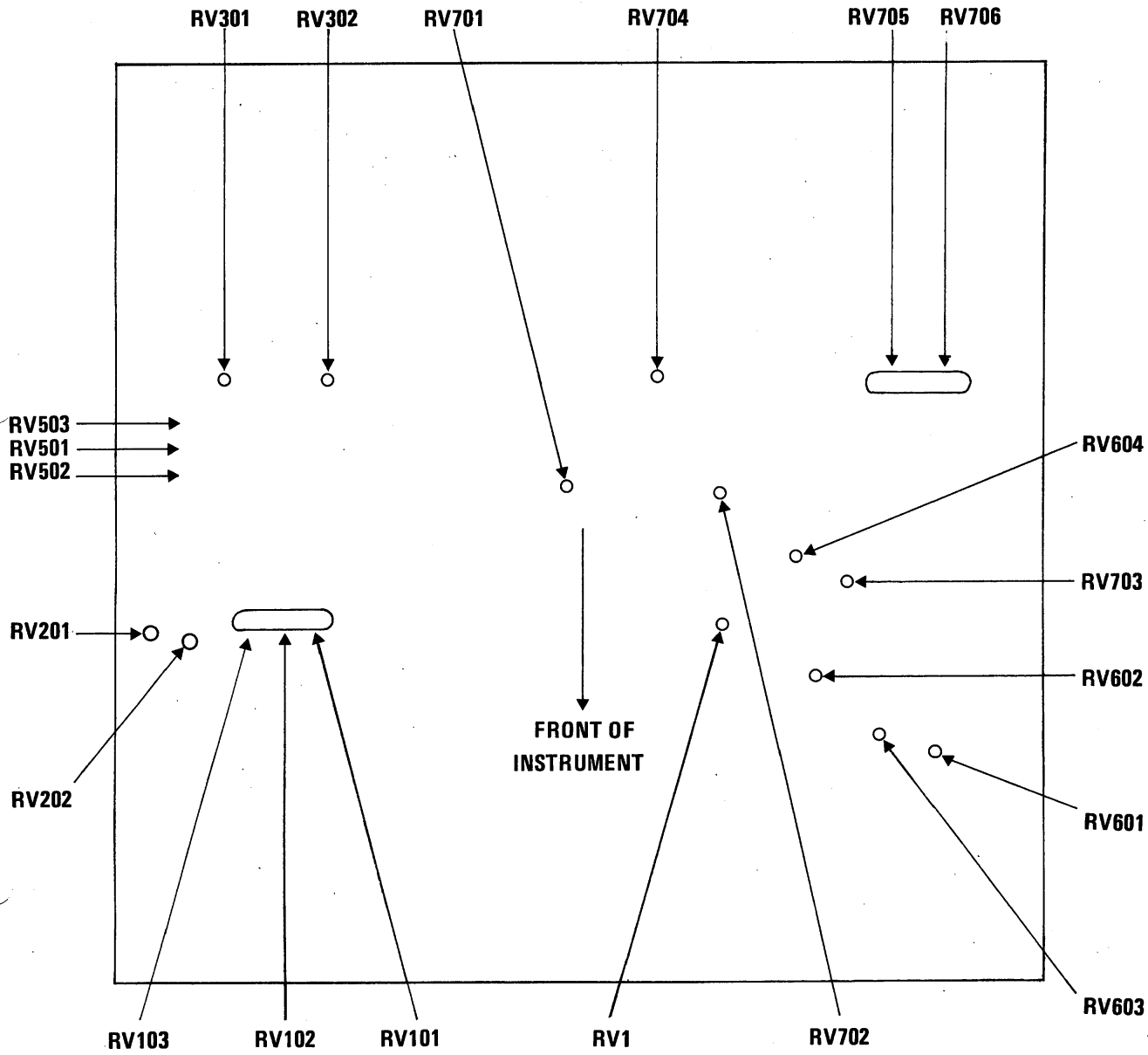


FIG. A1 View of Calibration Cover showing potentiometer access holes.