SECTION 5 Servicing

INTRODUCTION

Sections 5-8 contain Technical Information and are written primarily to meet the needs of the Service engineer. A detailed treatment of the principles of operation is not included but the descriptive text accompanying each circuit diagram is sufficient to enable the reader to understand the purpose of the circuit and its effect on its input(s). To facilitate fault diagnosis attention is drawn to special features of circuits, together with any precautions necessary when carrying out checks.

PRESENTATION OF INFORMATION

The circuit diagrams (Section 6) are arranged to fold out clear to the right, the functional description appearing on the facing left hand page. Similarly the pcb layout and notation diagrams will fold out clear to the left, where possible arranged to immediately precede the relevant text. Hence immediate cross reference can be made between the circuit and the component layout diagram.

Signal paths are indicated by bold lines, arrows being used where necessary to indicate the direction of functional flow. In general this is from left to right, feedback paths flowing from right to left. To prevent ambiguity however and where space is limited, this convention has not been followed rigidly.

COMPONENT IDENTIFICATION

In addition to the pcb layout diagrams, line drawings and/or clear photographs are reproduced in the manual to facilitate rapid identification of components during diagnostic checks.

The component numbers on each diagram are particular to that pcb only – thus each board will have, for example, an R1. Identification is by reference to the Parts List in Section 7.

On two major circuit boards the component numbering has been coded, a prefix digit being used to differentiate between components of the several functions carried on those boards. Thus R201 indicates R1 in the circuit coded '2'.
(This is explained in greater detail in the circuit descriptions.)

POWER RAILS

These are represented by short, detached bars annotated to show the nominal voltage. Several separate bars, annotated with the same voltage, may appear on a diagram. These of course are electrically connected to a common rail derived from the Power Supply circuits.

Zero volts may be either Supply 0V or one of six separate Signal 0V lines. Signal 'earth' rails are annotated Sig 0V1 to Sig 0V6, these being commoned at a star point. They should not be joined at any time during servicing.

Note that voltages specified on the circuit diagrams are in all cases nominal values, the actual value being dependent upon the load offered to the supply by the specific circuit. Inconsistencies between actual measured values and those quoted should not, therefore, be regarded with suspicion without considering other symptoms of possible unserviceability.

ELECTRICAL CONNECTIONS

Scotchflex ribbon connectors are generally used for pcb interconnections, though in some instances Berg - type pins/sockets have been used where pcb's are mounted in the same vertical plane. The latter are marked 'B', followed by a number.

It is important to ensure correct mating of all inter-board connections after any servicing operation.

SPLIT PADS

These are used to provide a means of isolating various parts of the circuit for fault diagnosis and, in some instances, to permit alteration of circuit parameters for a particular operating need. They are simply bridged with solder, open circuit being effected by removing the solder. It should be noted that excessive heat applied during this operation could damage the solder track – a small, low wattage iron should be used.

TEST POINTS

A further aid to rapid circuit check-out is the provision of test pins. These are indicated on the circuit diagrams and clearly marked on the pcb's.

TEST KIT 70759C

To provide access to certain circuit areas when servicing the instrument 'live', extension connectors have been assembled into a kit which can be ordered as an Optional Accessory.

CAUTION Ohms Guard

Before commencing any Servicing the instrument should be inspected to determine whether an Ohms Guard modification has been embodied. Serious permanent damage can be caused by an inadvertent short circuit of the Ohms Guard line to earth/signal low.

FLOATING CIRCUITS

As much of the instrument's electronic circuitry is floating with respect to Supply Earth, it is recommended that an isolating transformer is used for all servicing work within this voltmeter.

PRINCIPLES OF OPERATION

The 7075 dvm employs an A/D converter which converts the input voltage to a time analogue, which in turn is split into discrete, equal-length time units. These are counted and the result displayed as a numerical indication of the measured quantity.

The V to t converter produces a pulse train, the pulse width being variable and proportional to the magnitude of the input signal. The pulses gate the output of a fixed frequency clock into a counter, over a time period which can be chosen by the user. At the end of the time period the total accumulated in the counter is a measure of the input during that time. An averaging (integrating) technique is used whereby the total count is divided by the number of gating-pulses used. The average thus obtained is displayed as a direct reading of the measured quantity.

Statistically, the larger the sample the truer will be the average. This reasoning has been applied in the 7075, in that the integration time (the measurement period) can be varied by the user. At a fast reading rate the measurement period is very short and the average obtained is correct to, say, 2 decimal places. Increasing the measurement period provides a much truer average the resolution is increased to much smaller sub-divisions.

Since the total count is much larger when operating at the longer integration times, the counter requires more capacity. This results in an increase in scale length and it follows that the display sensitivity is improved hand-in-hand with the increased measurement resolution.

FUNCTIONAL DESCRIPTION

7075 can conveniently be regarded as consisting of four major functional sub-divisions. Reference to the Block Diagram (Diag 5.0) will identify those as:

1. the SIGNAL CONDITIONING section.
2. the A/D CONVERTER.
3. the DIGITAL section.
4. the POWER SUPPLY.

Considering the overall functioning of the instrument, an input is processed by the Signal Conditioning circuits which change all measured functions into a dc voltage, scaled to a level suitable for further processing. Input protection, reference and guard circuits are included in this sub-division.

The correctly scaled dc signal is converted to a train of digital pulses by the A/D Converter, these pulses being used to gate the output of a Clock circuit.

Control of the measurement conversion and timing of the control sequences are two important parts of the Digital section. It also contains the counters which accumulate the gated clock-pulses, the multiplexer and memory circuits and the display drivers. The decoded counter output ultimately provides drive currents to light the appropriate Display elements.

All necessary operating power for the analogue circuits and logic levels for the digital circuits are provided by the Power Supply. Also derived from this section of circuitry is the synchronising waveform for the mains-locked clock.

SIGNAL CONDITIONING

Regardless of what measurement is being made the Voltmeter is only capable of measuring dc volts, hence all other quantities require to be converted into a dc level. Once converted, the input signal is applied to an amplifier, the gain of which is determined by the range on which the instrument is operating. It is the output of this amplifier which is compared with the instrument's reference, both being applied to the A/D Converter.

A/D CONVERTER

The analogue input, changed to a dc voltage level and correctly scaled, is converted to digital form by a circuit which produces a pulse train, the width of the pulses being proportional to the magnitude of the input. This conversion technique is known as Voltage-to-time conversion - the method employed being a variant in which the "time" is in fact the difference between two distinct time periods. It is this time-differential which is used to control the number of clock pulses finally accumulated in an up/down counter in the Digital circuits.

DIGITAL SECTION

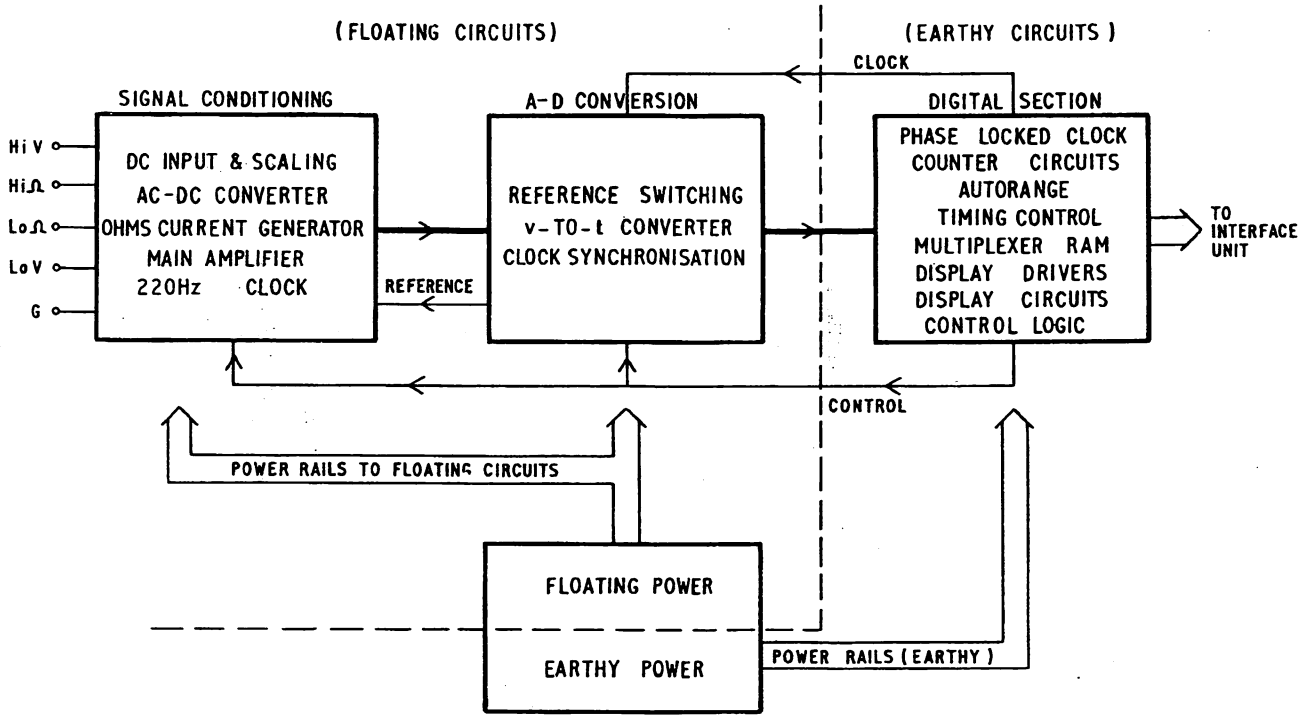
The heart of this section is the clock which produces the pulses which will be counted to digitally measure the applied signal. The clock pulses are gated into a counter stage by the V-to-t converter output pulse train. Two counters are used, the main one being concerned with the measurement function proper while a small, 3 × 9's counter gives a fast indication of range overload and initiates an autorange action. A further, timing counter determines the counting (or integrating) period.

The up/down (7 × 9's) counter output is multiplexed into the random-access memory (RAM) via a zero blanking circuit. Under the control of the sequence timing circuit the RAM is accessed, outputs being applied to the display interface to generate display drive signals.

POWER SUPPLY

The power supply consists of a switching regulator driving a 25kHz invertor to provide the main supply rails. Thus no mains transformer is used and voltage tappings are not required. A small transformer is included to provide the reference frequency for the mains locked clock.

It should be noted that parts of the power supply are floating with respect to supply earth. The use of an isolating transformer is essential when carrying out checks on the floating circuits.


(FLOATING CIRCUITS)
(EARTHY CIRCUITS)
CLOCK
SIGNAL CONDITIONING
A-D CONVERSION
DIGITAL SECTION
Hi V
Hi Ω
Lo Ω
Lo V
G
DC INPUT & SCALING
AC-DC CONVERTER
OHMS CURRENT GENERATOR
MAIN AMPLIFIER
220Hz CLOCK
REFERENCE
REFERENCE SWITCHING
v-TO-t CONVERTER
CLOCK SYNCHRONISATION
PHASE LOCKED CLOCK
COUNTER CIRCUITS
AUTORANGE
TIMING CONTROL
MULTIPLEXER RAM
DISPLAY DRIVERS
DISPLAY CIRCUITS
CONTROL LOGIC
TO INTERFACE UNIT
CONTROL
POWER RAILS TO FLOATING CIRCUITS
FLOATING POWER
EARTHY POWER
POWER RAILS (EARTHY)

Diag 5.0

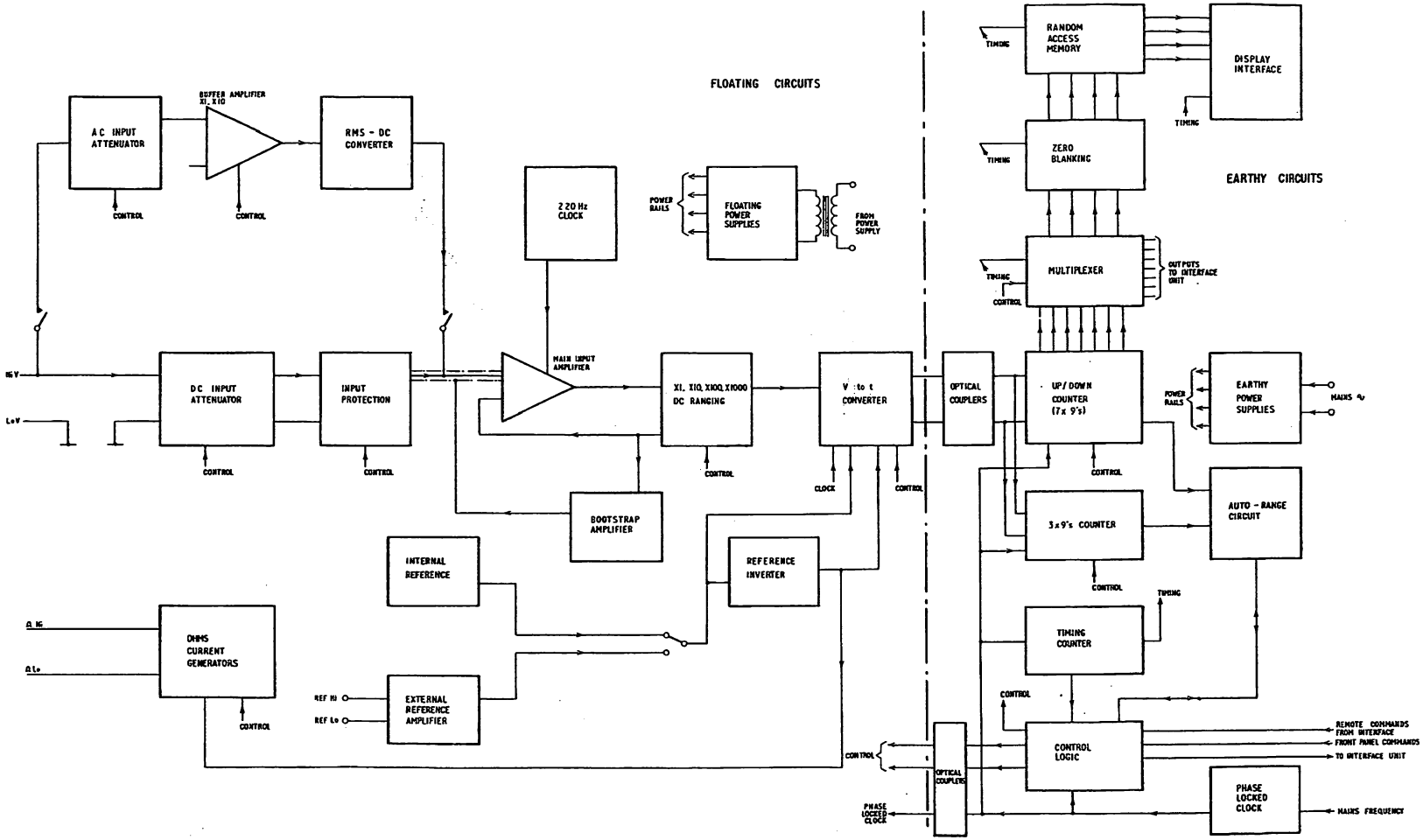
SECTION 6 Circuit Descriptions

This section provides the Servicing engineer with information concerning the function of the instrument's circuits, the treatment being one of defining the *effect* of each circuit on the input(s) applied to it. In the main the descriptions follow a signal path through the circuit board, diversions from the flow being examined as they become relevant to the signal. When considering the digital circuits, however, the descriptive text is concerned more with sequences and parallel logic activities. In these instances a flow treatment is inappropriate.

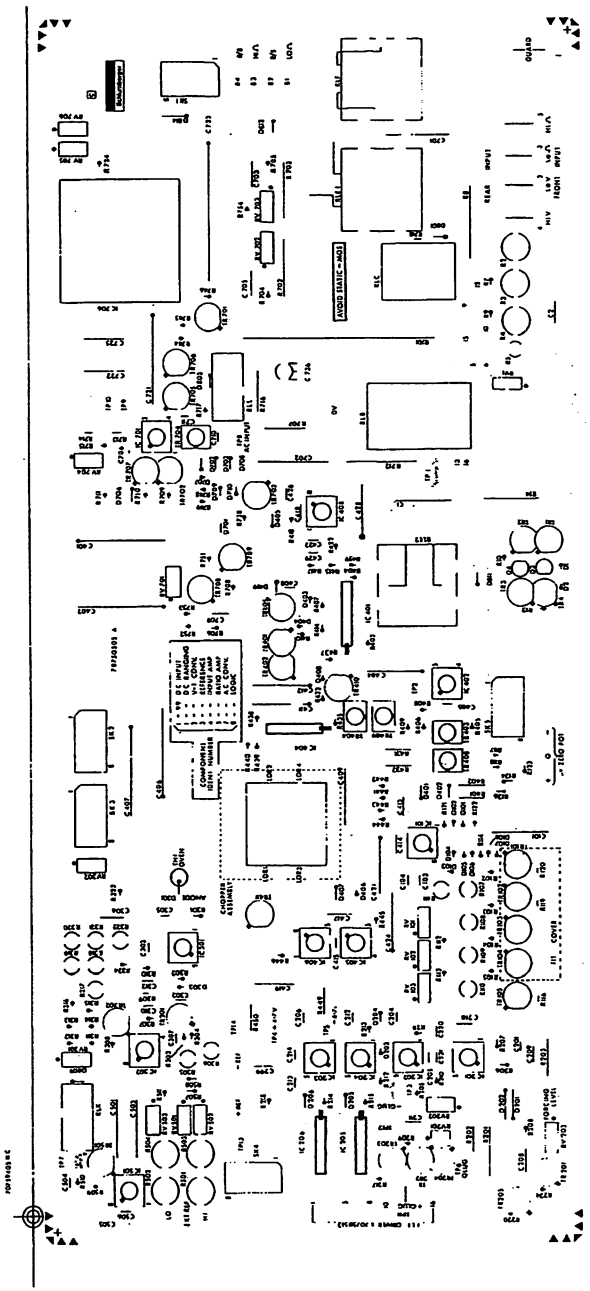
INTRODUCTION

The Block Schematic Diagram (Diag 6.1) illustrates the functional layout of the instrument. The diagram can be seen to be an expansion of that in Diag 5.0 and while it's primary function is that of affording an overall appreciation of the instrument, it also provides the reader with a pictorial index to the ensuing circuit descriptions

Block Schematic Diag. 6.1 →



Block Schematic Diag. 6.1



PCB 5 Notations

DC INPUT (Diag 6.2)

The purpose of these circuits is to provide initial conditioning of the input signal and to protect the Input Amplifier (Diag 6.3) against voltage overloads.

INPUT ATTENUATOR

The instrument can accept inputs up to 14V without attenuation, this circuit providing the necessary attenuation on the top two ranges. For inputs below 14V RLB is energised, relay drive being derived from pcb 6. The signal path is thus via R8 only. Above 14V RLB is de-energised providing 1:100 attenuation of the input signal, adjusted by RV1.
C2, R7 and R9 are spark suppression components.
The output from this stage can be monitored at Test Point 1.

INPUT PROTECTION

Despite the use of an Input Attenuator. large input swings could still occur, sufficient to overdrive the Input Amplifier. The Input Protection circuit provides an extra safeguard, limiting the signal line excursions to approximately 17V on the 10V and 1000V ranges.

On all other ranges the output from this circuit is limited to approximately 1.7V, Zeners D1, D2 being shunted by TR3, TR4.

LED's D3, D4 are used as normal diodes in this circuit. However they can provide a useful clue to an engineer if a persistent overload indication is being investigated.

AC AND Ω

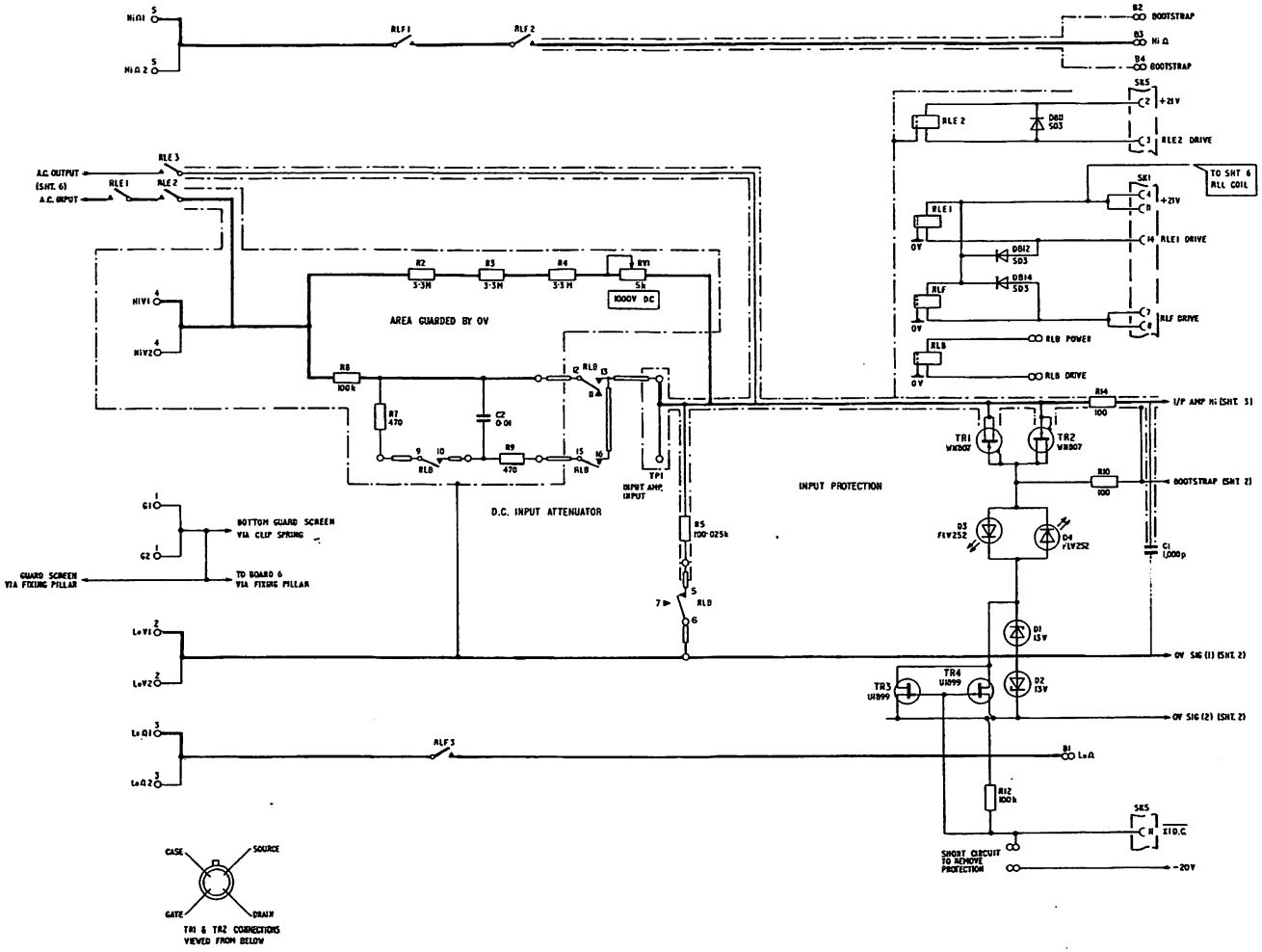
This circuit provides partial conditioning for the output from the AC/DC Converter, via RLE contacts, Input Protection being identical to that described above.

The Ohms Converter inputs are also to be found within this section of circuit, RLF providing the necessary switching.

BOOTSTRAP

Note the guard afforded to much of this circuit by the Bootstrap line. The output of a voltage follower (BOOTSTRAP AMPLIFIER, Diag. 6.4) provides local voltage 'guard', supplementing the effect of the main instrument Guard. Bootstrap potential is always that of the input to the main Input Amplifier.

← PCB 5 Notations



DC Input Diag. 6.2 pcb 5 (sheet 1)

INPUT AMPLIFIER (Diag 6.3)

All input signals, however derived, are applied to this circuit, the last in the signal conditioning chain. In conjunction with the DC RANGING circuit (Diag 6.4) the signals are scaled to a level suitable for processing by the A/D converter. The circuit is "area" coded 4.

MAIN AMPLIFIER

This is the amplifying element proper, the output from the circuits on Diag 6.2 being applied to a differential amplifier, which in turn feeds the operational amplifiers, IC's 402 and 408.

The gain of this operational amplifier is determined by the range resistors shown on Diag 6.4 .

DRIFT CORRECTION

The function of the remaining circuits illustrated is that of correcting differential amplifier drift caused by temperature variations. The drift errors, being no more than a few μ volts, are amplified in a Chopper Amplifier stage, the chopping being performed opto-electronically at 220Hz. LDR's 1 to 4 are light dependent resistors forming the Modulator. The amplified error is demodulated, the same 220Hz waveform (derived from pcb 6) driving the Demodulator. After passing through the Filter the drift correction potential is applied to one side of the differential amplifier output (IC 401).

DC RANGING (Diag 6.4)

The gain of the main Input Amplifier (Diag 6.3) is controlled by the scaling resistor network in this circuit, which also provides an additional measure of Input Amplifier protection, relative to Bootstrap. The circuit is "area" coded 1.

DC RANGING

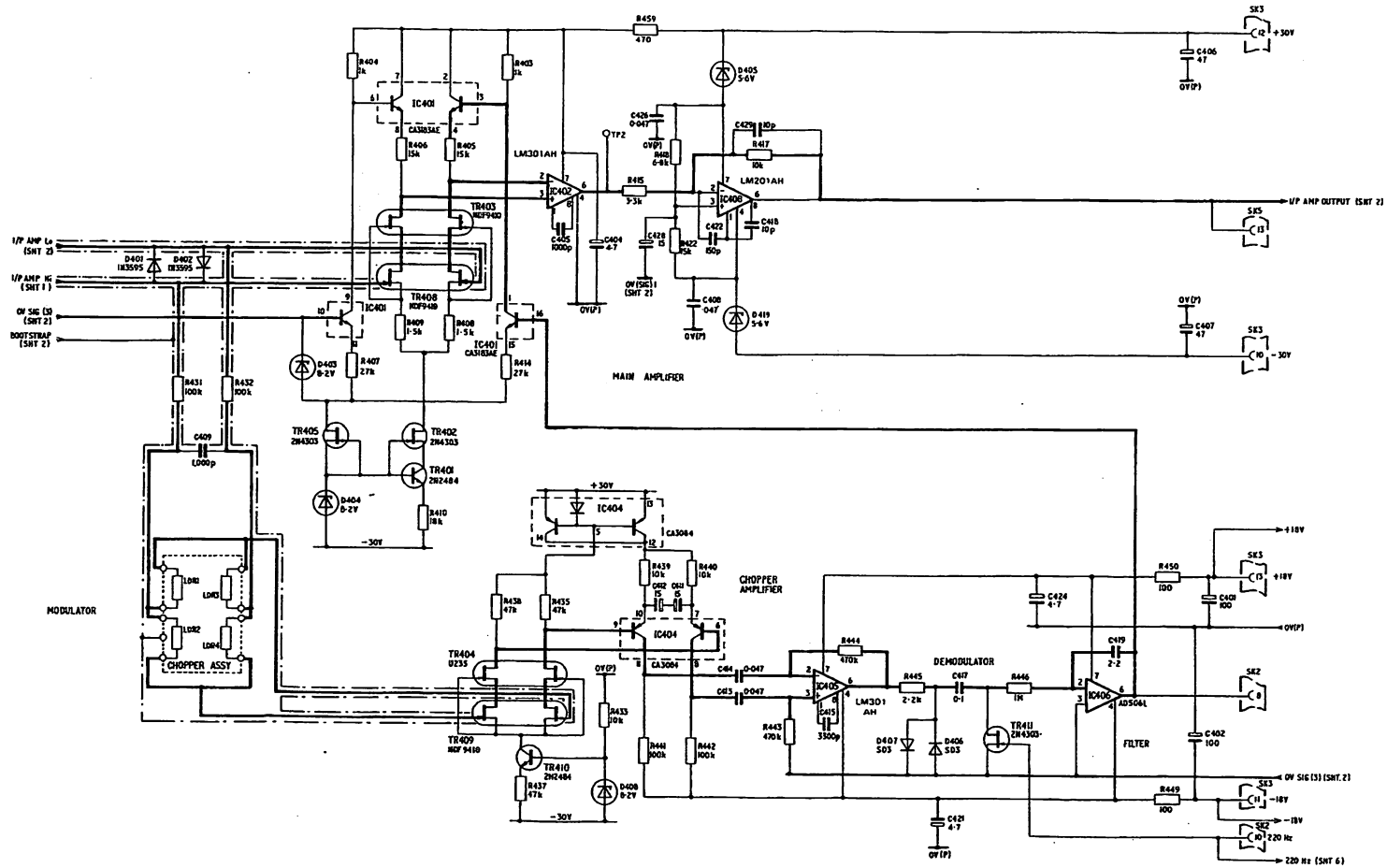
The FET switches TR's 101 to 104 are switched on by ranging signals derived from the DC Decoder on pcb 6. Thus the amplifier gain is determined by one of the matched set of 4 resistors R107 to R110. (Note that R111 completes the matched set).

BOOTSTRAP AMPLIFIER

IC101 is a low output impedance unity gain voltage follower producing an output which faithfully follows the input to the Input Amplifier. Its function in this circuit is to provide a rapid means of switching off FET's TR101 to 104. As mentioned earlier, Bootstrap also affords additional input guarding throughout the Input circuits.

PROTECTION

The Input Protection circuit shown in Diag 6.2 was concerned with protection relative to Signal 0V. The circuit shown here provides protection relative to the Bootstrap line.



Input Amplifier Diag. 6.3 pcb 5 (sheet 3)

V to t CONVERTER (Diag 6.5)

This circuit performs Analogue to Digital conversion, the applied voltage being converted to time periods which are used to gate the output of a Clock circuit. The circuit is clock synchronised to ensure that the pulses in the "pulse train" start and finish exactly on a clock edge. This section of pcb 5 is "area" coded 1.

INTEGRATOR

A continuously running Dynamic Integrator is driven between preset limits by a 1kHz forcing waveform, to produce a symmetrical triangular waveform output.

LEVEL DETECTOR

Compares the excursions of the Integrator output with reference levels, switching Integrator reference potentials which maintain the closed loop action of the Integrator. This system can be regarded as having pulse-width modulated feedback — the pulse width varying in proportion to the input signal applied to the instrument.

REF. SWITCHES

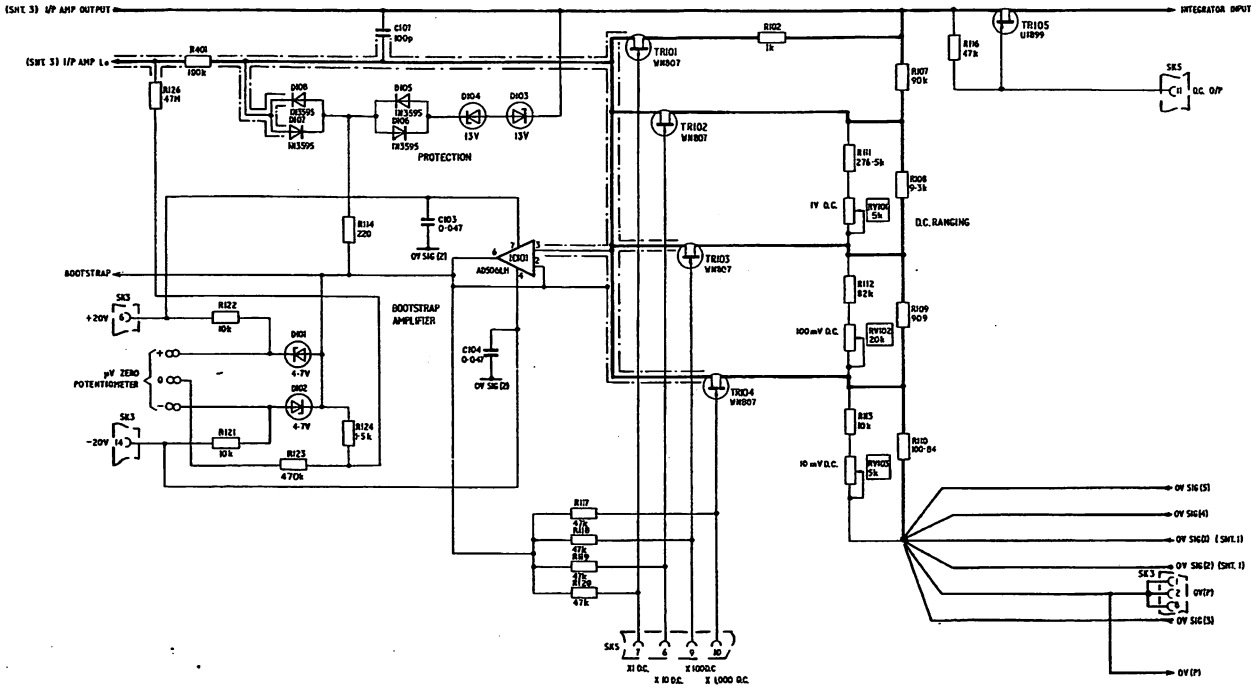
Controlled by the Level Detector via the FET Driver, these switches apply one of two reference potentials, or Sig. 0V to the "virtual earth" of the Integrator. The cut-on/cut-off of the FET switches is determined by the polarity of the input (dc) and its magnitude. The voltage across R202 can be represented by a train of positive and negative pulses, running at 1kHz, the pulse width being variable with voltmeter input.

CLOCK SYNC.

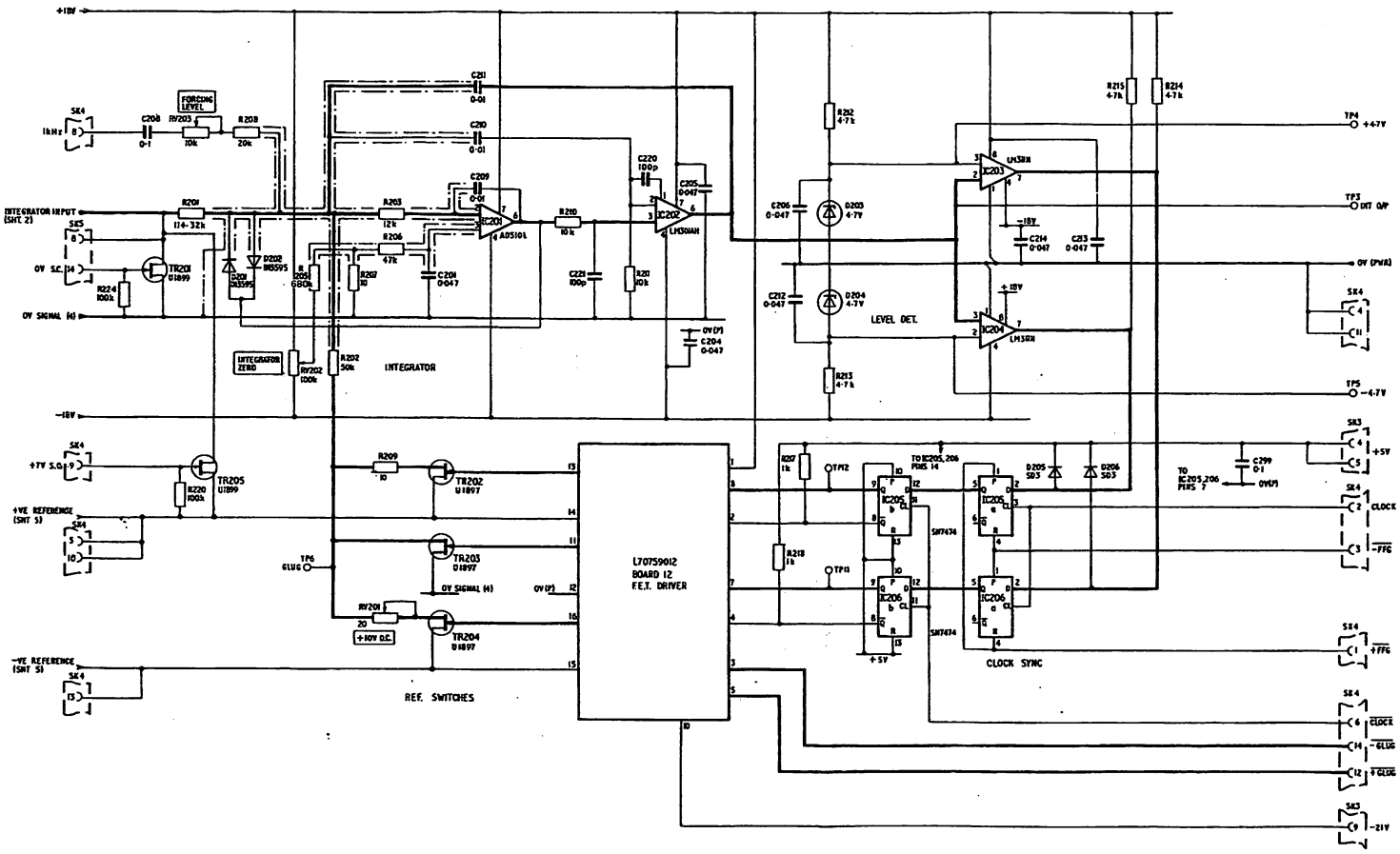
Synchronisation of the feedback waveform with the Clock is achieved by this section of the circuit.

FET DRIVER

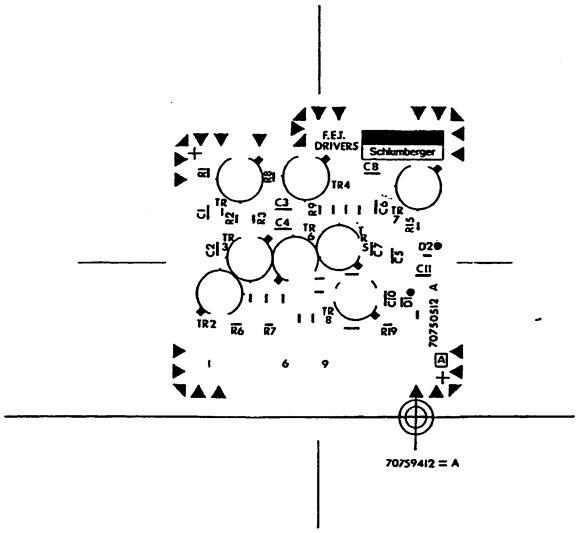
The circuit carried on pcb 12 is described overleaf.



DC Ranging Diag. 6.4 pcb 5 (sheet 2)



V to t Convertor Diag. 6.5 pcb 5 (sheet 4)



PCB 12 Notations

FET DRIVERS (Diag 6.6)

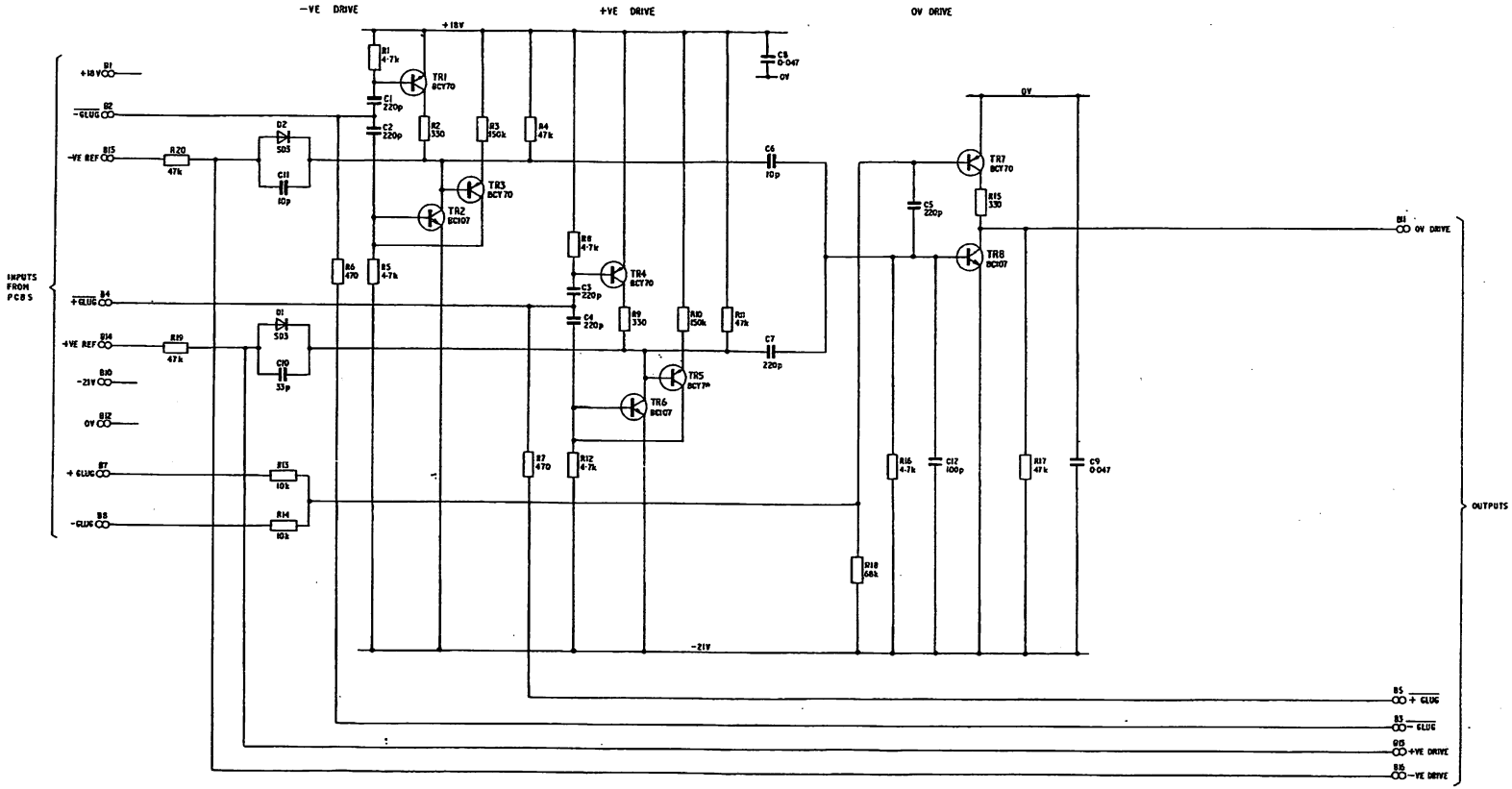
The circuit illustrated, though forming part of the reference switching arrangement on Diag 6.5, is carried on a separate plug-in card, pcb 12. Interconnection with board 5 is via Berg-type horizontal sockets, the mating pins being mounted vertically on board 5.

The FET Drivers provide fast switching of the reference potentials and 0V, the circuit configuration ensuring rapid transition from one switch state to the other. TR3, TR5 perform a 'latching' function for the ON state of their associate switches. In the case of the 0V switch both ON and OFF states are latched by the inputs on pins B7, B8. Pins B6, B9 are not used.

GLUG

Within this manual the reader will find many signal annotations which include the word "Glug". The word may be abbreviated to the letter 'G', as in FG (*forced* glug), FFG (*forced forced* glug) etc. The term is used as a convenient alternative to the cumbersome title "Quantum of Charge" (i.e. V x t) and should be treated merely as an identifier label, facilitating circuit tracing.

← PCB 12 Notations



Fet Drivers Diag. 6.6 pcb 12

AC CONVERSION (Diag 6.7)

Diag. 6.7 illustrates the circuits concerned with processing an alternating input to produce an equivalent dc level. The dc thus obtained is further conditioned as described in earlier pages under "DC". This circuit is "area" coded 7 on pcb 5.

AC ATTENUATOR

Three alternative signal paths provide attenuation as follows:

On the 1000V range	1 : 1000	via R701, R702, RLL
On the 10V, 100V ranges	1 : 100	via R701, TR701
Other ranges	no attenuation	via RLC

The output from this stage is thereby scaled to a maximum of 1V. Relay drive for RLC and RLL is derived from the AC DECODER circuit (FLOATING LOGIC pcb 6), as is the signal $\overline{\text{AC ATTEN}}$. Potentiometers RV702, RV703 provide attenuator adjustment for the 10V and 1000V ranges while C736 is adjusted to balance the attenuator for 100V at input frequencies above 10kHz.

BUFFER

The Buffer Amplifier has a dual role, that of isolating the input from the low input impedance of the Converter and of providing amplification of small input signals from the attenuator. Buffer gain is switched between unity and X10 by TR's 705, 706, R704 controlling the gain at 100mV.

AC SCALING SUMMARY

Nominal Range	Attenuation			Buffer gain	
	1 : 1000	1 : 100	1 : 1	X1	X10
100mV	–	–	√	–	√
1V	–	–	√	√	–
10V	–	√	–	–	√
100V	–	√	–	√	–
1000V	√	–	–	√	–

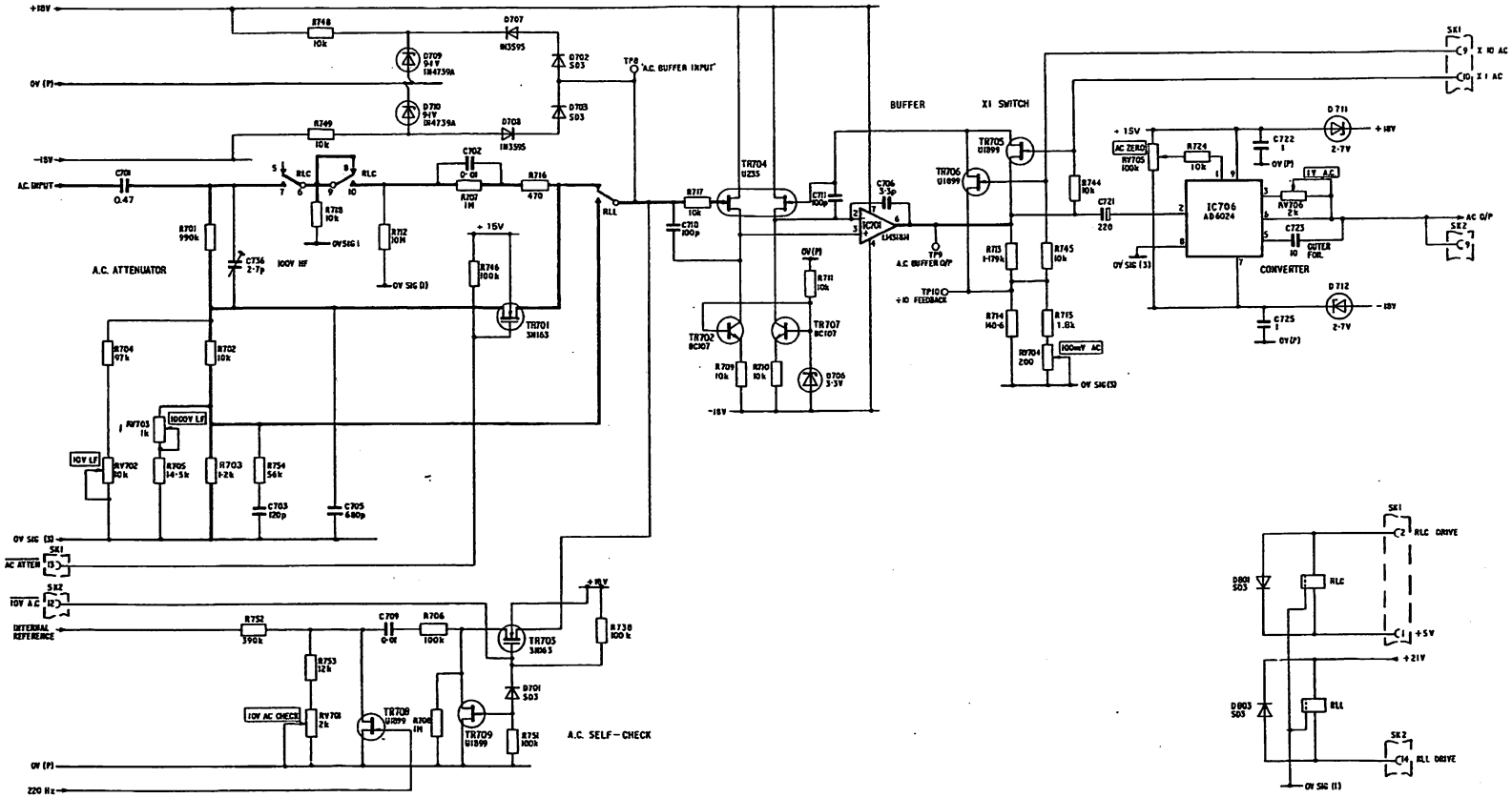
CONVERTER

IC706 with its associated components performs the conversion of the rms of the ac to a dc level.

Zero adjustment is provided by RV705, the 1V output potentiometer being RV706.

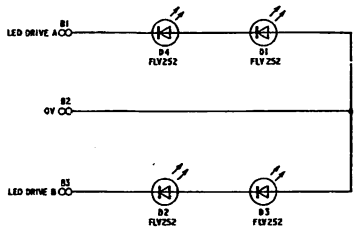
SELF CHECK

The voltmeter internal reference is chopped at 220Hz and applied as a 100mV ac "reference" to the Buffer, via the switch TR709, TR703. The 1V signal thus obtained is scaled to give a Self Check display of 10V.

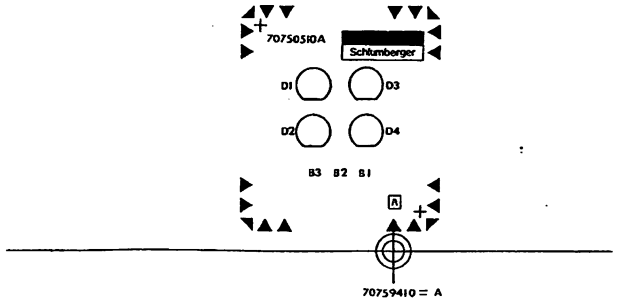


AVOID STATIC M.O.S.

AC Conversion Diag. 6.7 pcb 5 (sheet 6)



PCB 10 Circuit Diagram



PCB 10 Notations

RESISTANCE (Diag 6.8)

Resistance measurement with the 7075 is accomplished by measuring the voltage developed across the unknown resistor by virtue of a known current passing through it. The major function of the section of Board 6 illustrated is that of generating the necessary current. The circuit is "area" coded 6.

CURRENT GENERATORS

The instrument's negative reference is utilised to determine a current which, in it's turn, produces a reference potential relative to the +30V rail — divided down across R602, R604 (a matched set). This potential defines the Hi Current, the value of which depends on the position of reed switches as follows:

RLH 1 closed	1mA	(10Ω to 10kΩ)
RLG 1 closed	10μA	(100kΩ to 1MΩ)
Both reeds open	1μA	(10MΩ)

The Lo Current generator provides the necessary current sink to give effective 4 - terminal measurement, potentials arising from lead resistances being nullified. The second contacts of reeds RLG, RLH perform a similar function to those outlined for RLG1, Hl above.

Link A across R603 is set as required during factory calibration. IC's 601 to 603, unity gain amplifiers are used in this configuration as voltage followers. High voltage (up to 300V) protection is given by D606, R610 and TR's 605 and 606.

Note that the Hi Current circuits are guarded relative to the potential developed across R604, Bootstrap providing the remaining guard potential.

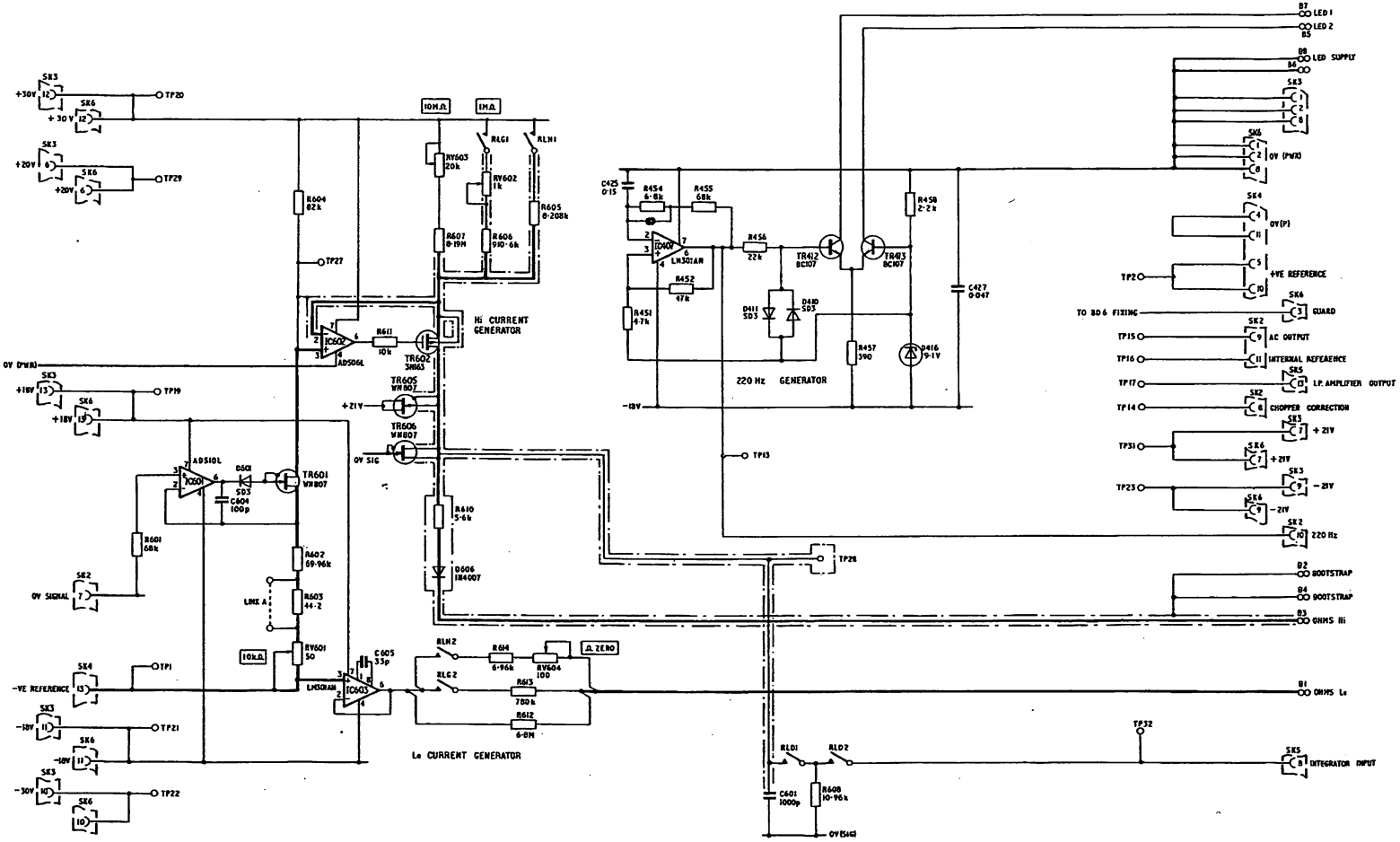
SELF CHECK

The 1mA current through R608 in parallel with the input resistance of the Integrator produces 10V for the nominal Self Check 10kΩ display. Control is via RLD.

CHOPPER DRIVE

Also illustrated in Diag 6.8 is the 220Hz Generator (area code 4) which produces the chopping waveform used in the Input Amplifier circuit (Diag 6.3). Outputs are taken via Berg pins 5 and 7 to the LED's forming part of the opto-electronic Chopper Modulator (Diag 6.3). A further output feeds the Demodulator in the same circuit area of pcb 5. A link is provided across R454 to permit a small adjustment of the nominal 220Hz, if the oscillator frequency is found to be a harmonic of the supply frequency.

← PCB 10 Notations and Circuit Diagram



Resistance Diag. 6.8 pcb 6 (sheet 1)

REFERENCE (Diag 6.9)

The voltmeter's reference potentials are generated in the circuits illustrated, which are "area" coded 3 on Board 5. The other circuit, coded 5, processes the External Reference associated with RATIO operation.

INTERNAL REFERENCE

Zener D301 defines the +ve Reference at +9V above the potential of the inverting input of IC301. The zener current is that through R301 derived from the Inverter. The junction of the matched pair R321 R322 is at −2V, regulated by the action of IC301, TR301. Thus the emitter of TR301 is held at +7V, which is used as the +ve Reference.

The network R311 through R320, with RV301, is used during calibration to take out zener tolerances and thus accurately define the +7V.

REFERENCE INVERTER

The system is stabilised by using an inverted version of the +ve reference as the current source for D301. A closed loop is thus formed, producing −7V at TR302 emitter for use as the −ve Reference.

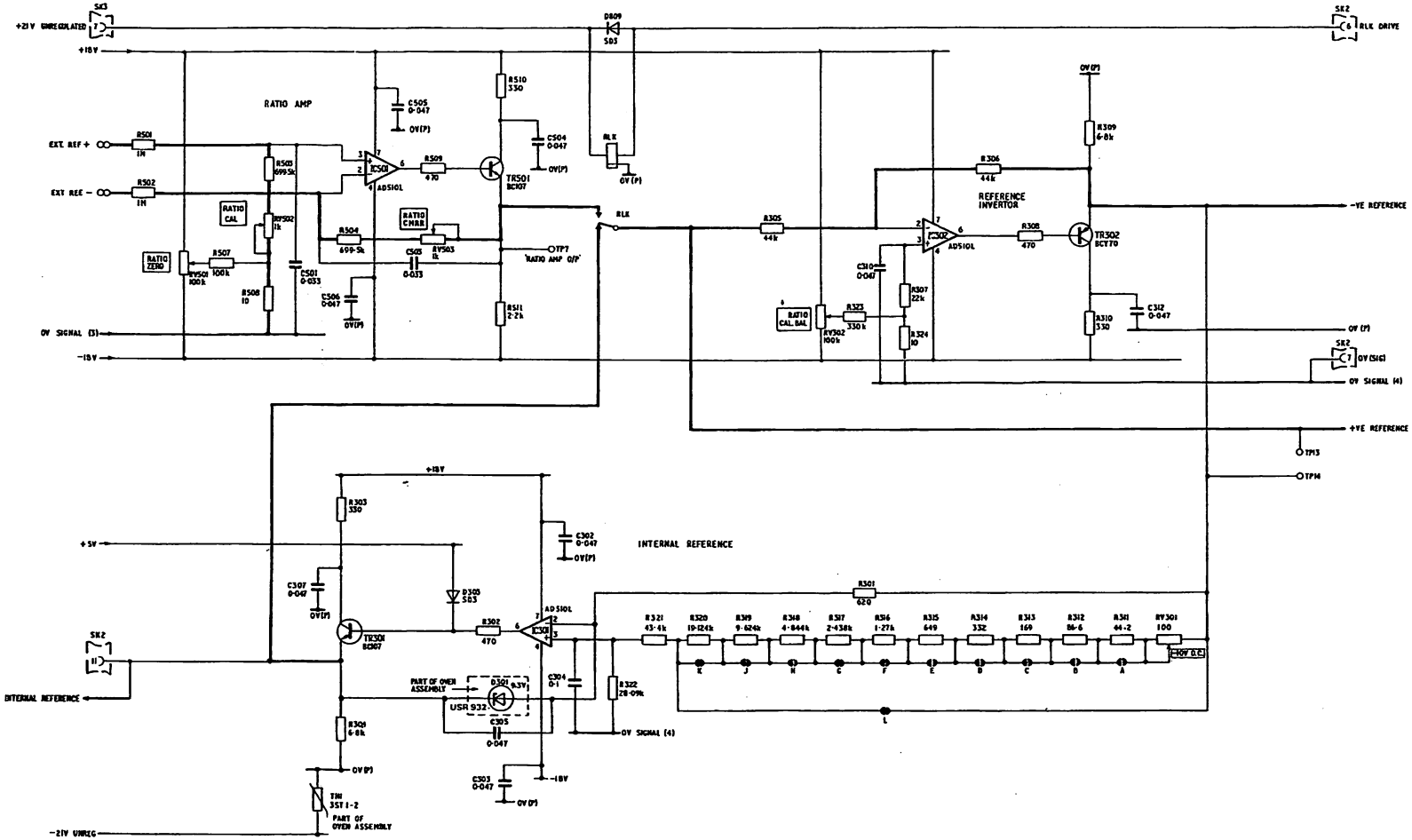
The circuits described, once set up, are very stable and independent of variations of the 18V rails. However under certain circumstances it would be possible for latching to occur in the wrong direction. D303 prevents this by holding TR301 base above +5V.

RATIO AMP

An external reference is fed to the Inverter via IC501, TR501 and the changeover relay RLK. This replaces the Internal Reference with the user's choice of reference potential for RATIO measurement.

RV503 corrects for Common Mode errors between Ratio Hi and Ratio Lo, RV502 setting the output of IC501/TR501. Offsets in the IC are taken out by RV501.

Offsets in the amplifier IC302 are taken out by adjusting RV302, **such adjustment forming part of the RATIO calibration procedure.**



Reference Diag. 6.9 pcb 5 (sheet 5)

FLOATING LOGIC (Diag 6.10)

The main function of the area of Board 6 coded 8 is that of decoding Front Panel (and Systems Interface*) Commands associated with measurement Mode (Function) and Range. The circuits are floating with respect to supply 0V, data transfer being accomplished by means of optical couplers. The circuit coded 2 forms parts of the V - to - t Converter (Diag 6.5).

SERIAL DECODER

Data is sent at the beginning of each reading to determine the Function and the measurement Range. The state of the Serial Data lines is fed as an 8 - bit serial word to the Serial Decoder, strobed by an 8 - pulse clocking signal, Serial Strobe (Test Point 12). The resulting data is set on lines A to H of the 8 - bit shift register IC819.

NOISE REJECTOR

This binary counter circuit only produces a strobe output if the 8 - pulse clocking signal is complete. Thus spurious noise peaks are not detected as Clock pulses.

The strobe thus produced clocks the output lines of the Shift Register into a pair of 4 - bit buffer stores, IC's 814 and 815, the decoded Mode and Range data being held for the duration of the current reading.

SK8 is a test socket for use with an ATE device such as Membrain.

MODE DECODER

Apart from RATIO, which is processed directly into a drive for RLK (Diag 6.9), the binary Mode code and that for Self Check are decoded in a 4 to 16 line decoder IC802. For each of the possible input codes one of the 16 output lines is set Lo. All 16 outputs are connected, those corresponding to each measurement mode being commoned in 4 - way wired OR networks. The remaining 4 outputs specify the measurement tests of the Self Check function — shown in tabular form overleaf.

AC DECODER

IC's 803, 804 and 805 (excluding pins 5, 11 and 2, 14) provide the necessary decoding and current drive for the control of the AC signal conditioning circuits (Diag 6.7). The input on pin 12 of IC803 is the AC decode from the Mode Decoder, the other inputs being binary coded Range data from IC815.

OHMS DECODER

Control for the Ohms Converter (Diag 6.8) is derived from this circuit, the input being $\overline{\Omega}$ from the Mode Decoder and Range data in binary code from IC815.

DC DECODER

Together with part of IC805 (pins 5 and 11), this section of the circuit generates the control and drive signals for the DC Signal Conditioning circuits (Diags 6.2, 6.3, 6.4). $\overline{DC}$ and binary coded Range data are the inputs, derived from IC802 and IC815 respectively.

*see Section 9 of this manual.

SELF TEST (Diag 6.10)

Test	IC802 Pin No.	Decoded/Processed by	Range/Mode Selection	Control Signal Output	Effective on Diagram
7V dc	5	IC813(b), IC805		7V SC	6.5
			D804, IC808	DC O/P	6.4
0V	1	IC811(d), IC808		0V SC	6.5
			D813, IC808	DC O/P	6.4
10V ac	14	IC805		10V AC	6.7
			IC811(b), IC812(e).	RLE/2 DRIVE	6.2
			IC809(b), IC811(c), IC808, IC807.	X10 DC (Note 1).	6.7
10kΩ	9	IC810(c)		RLD DRIVE	6.8
			D805, IC808	DC O/P	6.4
			IC810(c), D815	RLH DRIVE (Note 2)	6.8
Display	— (Note 3)	—	—	—	—

Notes

1. This control signal selects the correct scaling factor for the test ac.

2. RLH is energised to provide a measurement current of 1mA.

3. Self Check Test No. 5 is not decoded on this board. The Control Signal LAMP TEST, derived from the Self Check logic on pcb 3, is connected directly to pcb 2. The decode is equivalent to Test 1 (code 00).

INTEGRATOR CONTROL (Diag. 6.10)

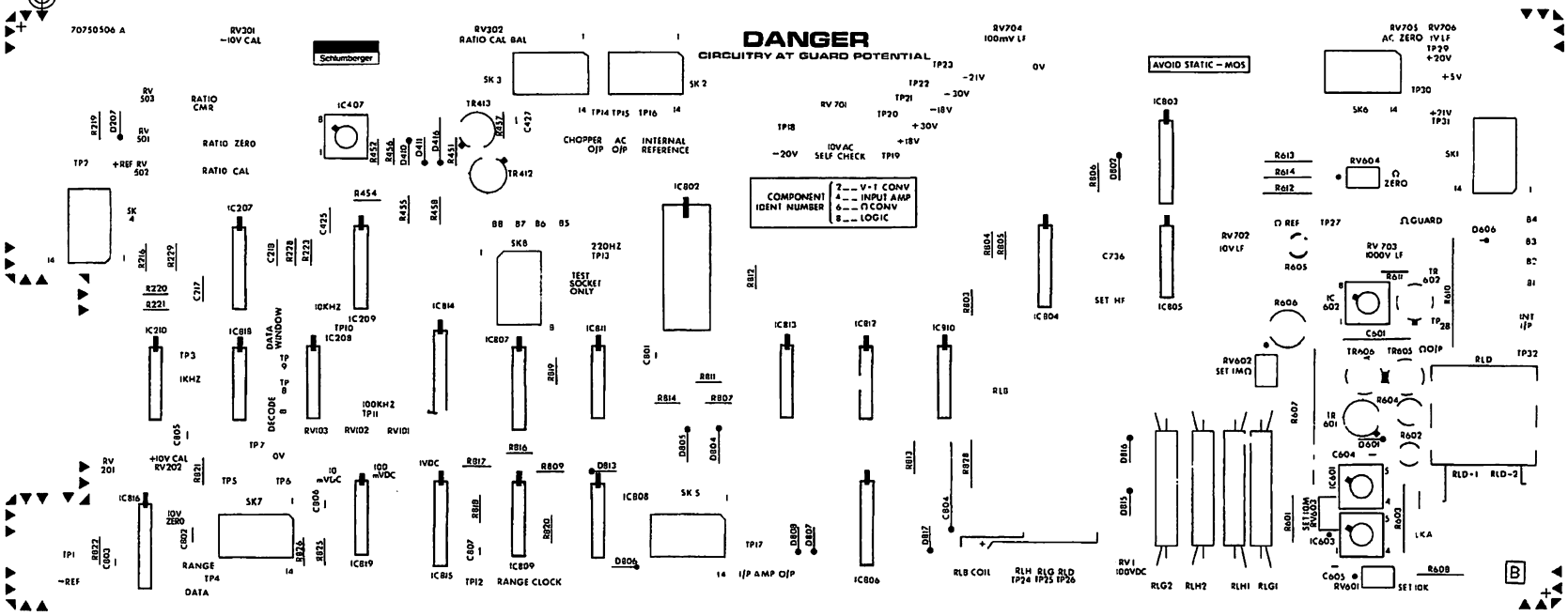
The Integrator Control logic, "area" coded 2, provides controlling waveforms for the dynamic integrator described earlier (V - to - t CONVERTER, Diag 6.5). A floating circuit, the inputs to it are made via optical couplers.

INTEGRATOR CONTROL

Clock pulses are processed by IC209, the three sections of which provide ÷ 16, ÷ 10, ÷ 10 to the input 1.6MHz. The resulting square wave at 1kHz is the Forcing Waveform (FW) controlling the ramp up and down of the Integrator (Diag 6.5). D207 limits the positive excursions of FW to +10V.

The 1kHz signal is further processed by IC207(a) and (b) to produce two pulses, each coincident with an edge of FW. The pulses, +FFG AND −FFG, are utilised in the Clock Sync circuit of the V - to - t Converter (Diag 6.5).

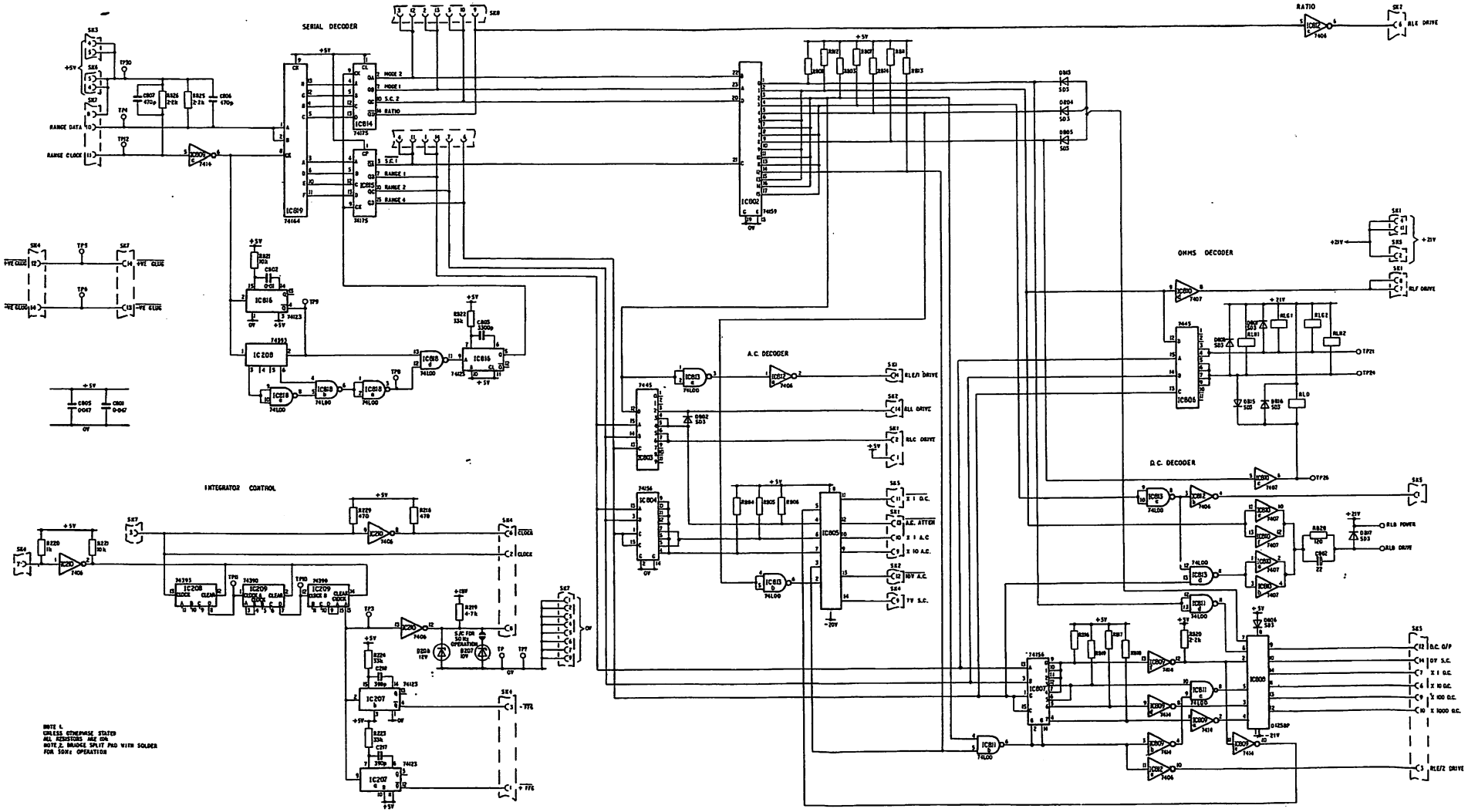
PCB 6 Notations ⟶



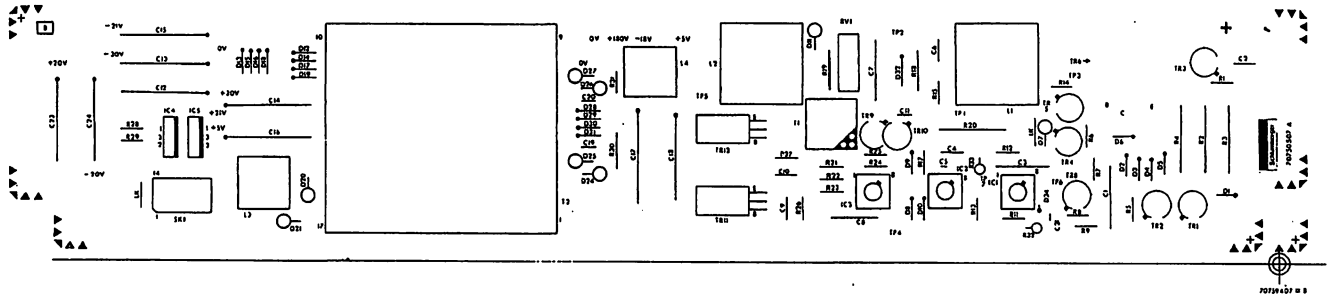
THIS BOARD MUST BE SILK SCREENED
WITH YELLOW PAINT.

PCB 6 Notations

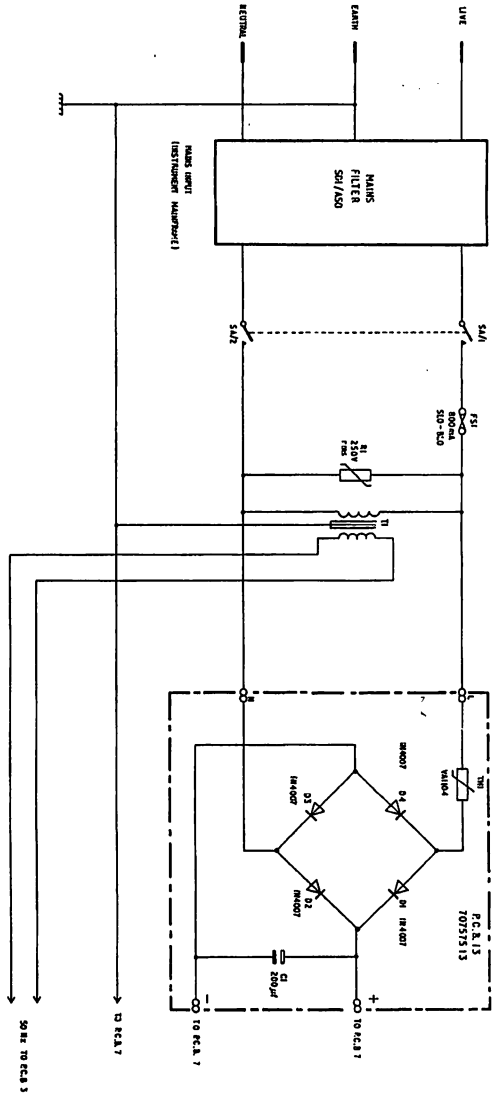
PJL/7075/3



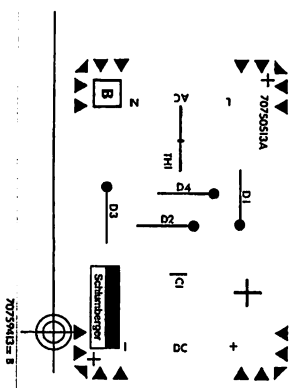
Floating Logic Diag 6.10 pcb 6 (sheet 2)



PCB 7 Notations



Mainframe Diag. 6.11



PCB 13 Notations

POWER SUPPLY (Diag 6.12)

The instrument's power rails are derived from the circuits on the facing page and that shown overleaf.

Applied directly, without the use of a mains transformer, the supply voltage is roughly rectified by the circuit on pcb 13 (Diag 6.11) before being converted to a regulated dc by a Switched Regulator circuit. The dc thus obtained is again converted to a stable ac by means of an Inverter stage, the output of which feeds the primary of a transformer.

The transformer secondary winding and it's associated conventional rectifier circuits are shown on (Diag 6.13).

START UP

When the instrument is switched ON this circuit produces an initial supply for the remaining circuits. The current through TR3 is controlled by that through TR1, which is itself dependent on TR2. The base level for D4, D5 is determined by TR2 which conducts reducing TR3 conduction when the potential across the zeners exceeds their combined nominal limit. The circuit thus operates in a closed current loop maintaining the junction of D5, R4 at +30V derived from the mains input.

VOLTAGE REGULATOR

After the initial current surge the circuit described above settles very rapidly. The Voltage Regulator then takes control to re-define the +30V rail and switch-off the Start Up circuit. A series transistor, TR6, is switched on/off at 30kHz by the output of oscillator IC1 via TR8, TR5. The mains supply is therefore pulsed by TR6 before being smoothed by choke L1. The mark/space ratio of the switching 30kHz is controlled by the output of comparator IC2, determining the ON/OFF time of TR6 and thus the regulated voltage level. RV1 adjusts the comparator 'sample' to set the output of the regulator to +70V.

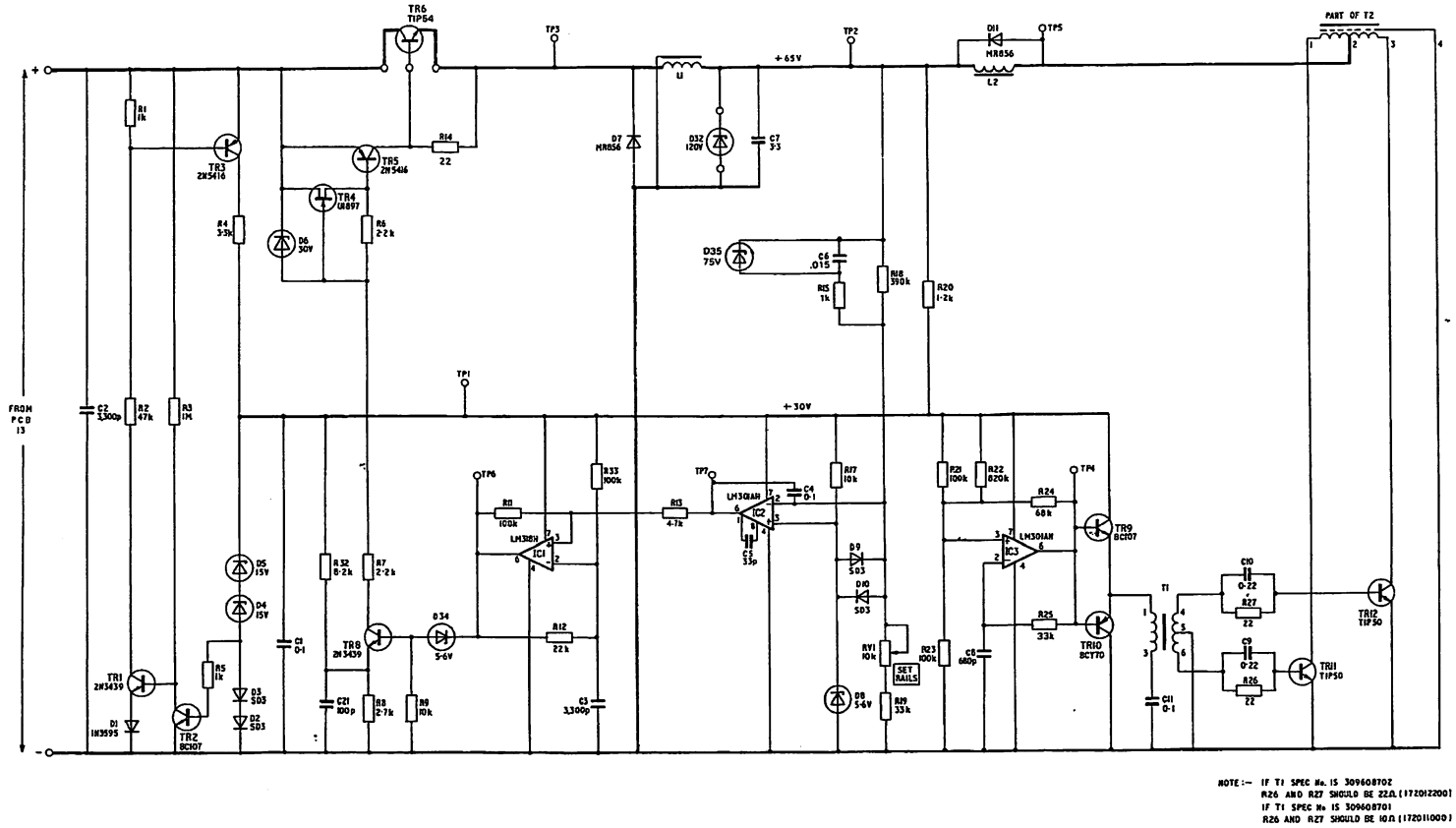
The current through R20 now defines the +30V rail and, via D5, D4, it causes the now redundant Start Up circuit to be turned off.

Note that mains ripple is eliminated by the high switching speed of IC's 1 and 2.

INVERTER

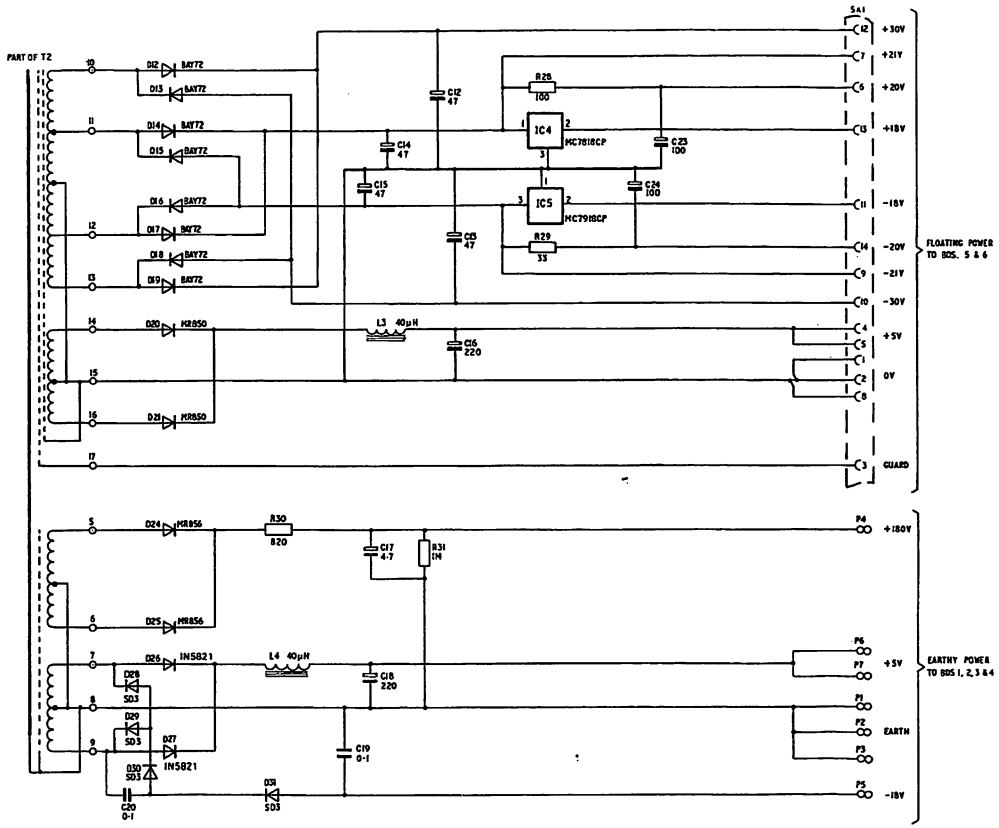
IC3 is connected as an oscillator, switching the common emitter of TR9, TR10 between +30V and the neutral rail, at approximately 20kHz. The square switching waveform, stepped down by transformer T1 causes TR11, TR12 to alternately turn on and off. Thus the primary winding of T2, centre fed by the regulated +70V rail, produces an alternating current which is independent of mains supply voltage and frequency. This "supply" is used in the rectifier circuits which follow.

← **Diag. 6.11. PCB 7 and PCB 13 Notations**



NOTE :— IF T1 SPEC No. IS 30960870Z
R26 AND R27 SHOULD BE 22Ω. (17201220Ω)
IF T1 SPEC No IS 30960870Ⅰ
R26 AND R27 SHOULD BE 10Ω. (17201100Ω)

Power Supply Diag. 6.12 pcb 7 (sheet 1)



Rectification Diag. 6.13 pcb 7 (sheet 2)

RECTIFICATION (Diag. 6.13)

T2 secondary windings provide the rectifier current required to power the various dc rails used within the voltmeter.

IC4, IC5 are used to regulate the floating positive/negative 18V rails.

D27 to D30 act in a voltage trebler circuit from the earthy +5V winding to give a nominal −18V on P5. This rail supplies the keep-alive electrode of the display tubes.

The anodes of the display elements are fed with +180V, output on P4.

Note that terminal 17 of transformer T2 is at Guard potential and should NOT be connected to 0V, nor to Supply Earth.

WARNING – FLOATING SUPPLIES

For safety always use an isolating transformer.

← Diag. 6.13

DIGITAL

This part of section 6 covers those circuits which convert the pulses generated in the A/D converter into a digital count, which after further processing is used to drive the display.

The Block Schematic Diagram (Diag 6.14) illustrates the functional layout of the digital section, which for convenience, can be considered as having 3 sub-sections:

1) **Counters and Memory (Diag 6.15, 6.16)**
2) **The Control Logic (Diag 6.17, 6.18)**
3) **The Display, Display Drive and Phase Locked clock (Diag 6.19, 6.20).**

COUNTERS AND MEMORY

This sub-section is illustrated on two sheets, Diag 6.15 and 6.16, and comprises the counter chain with its associated input circuits, the data transfer Multiplexer and the Random Access Memory (RAM) including the necessary Read/Write logic. The Timing Counter, together with the organisational logic associated with the formatting of the geographical display is shown on Diag 6.16.

THE CONTROL LOGIC

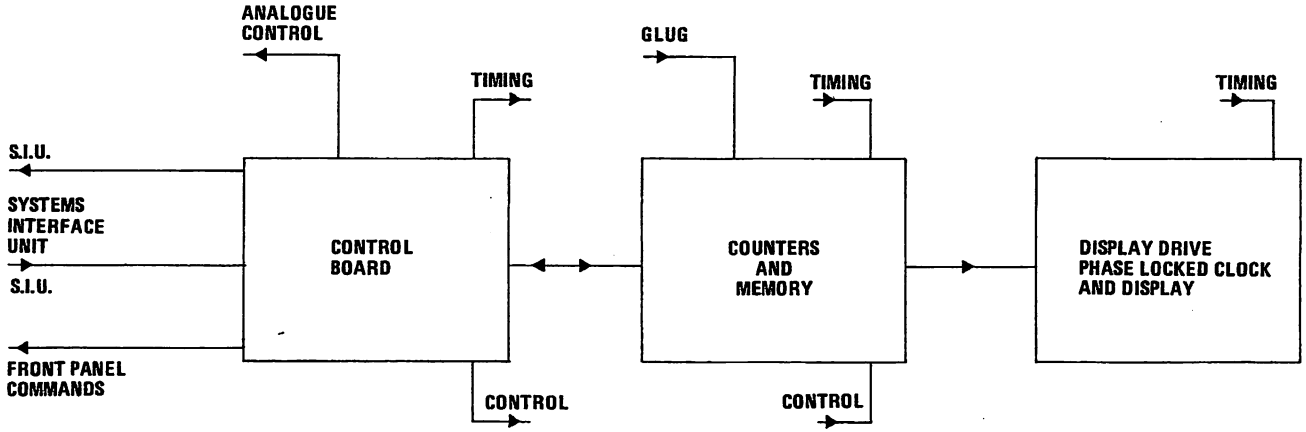
This board controls the other logic boards and the floating circuitry. Shown on Diag 6.17 are the Main Control, the Range Control logic and Self Control logic circuits, the "State" Counter and its decoder.

On Diag 6.18 are the Opto-Couplers, Autorange circuits and Display Flashing logic.

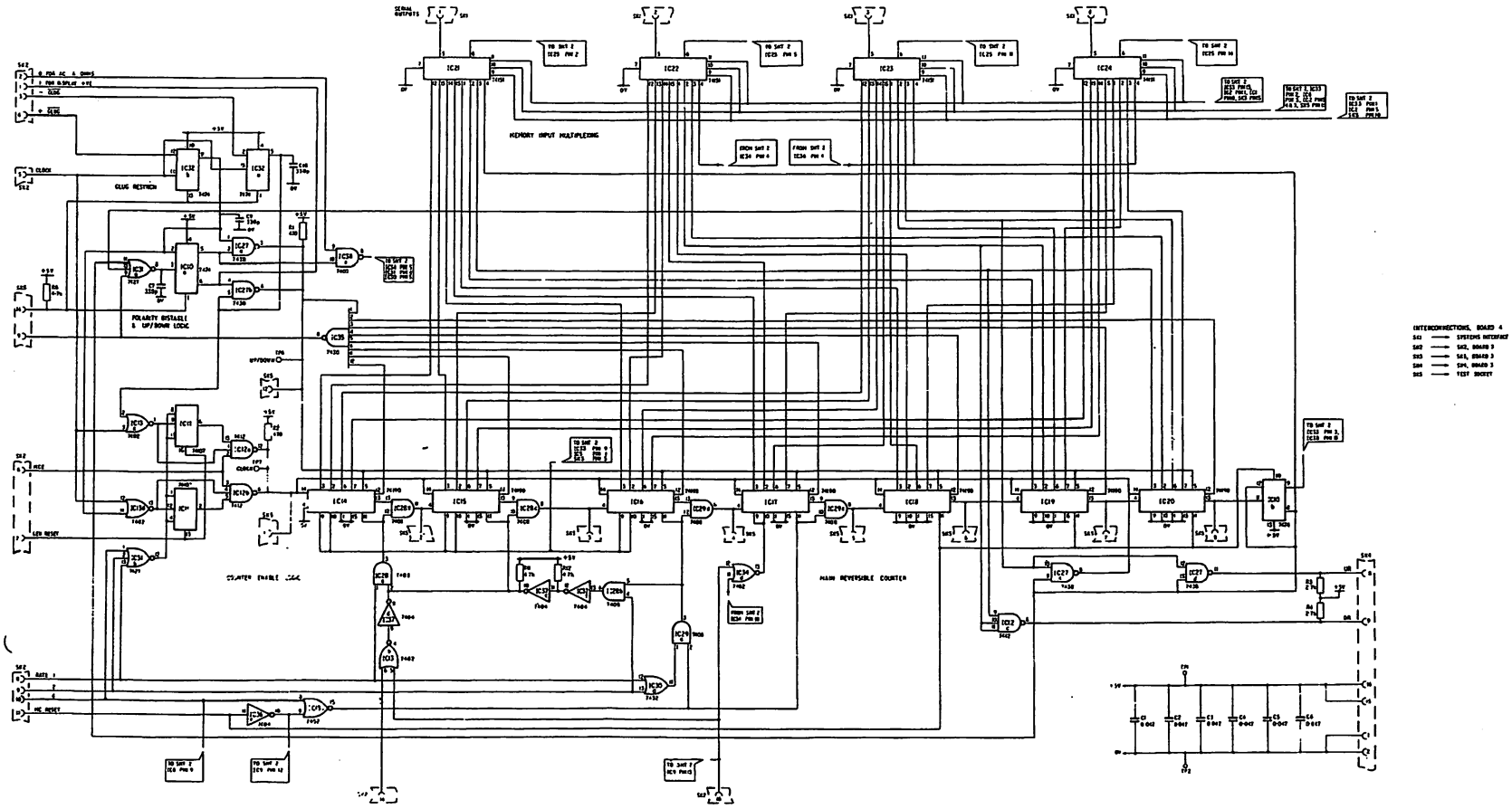
THE DISPLAY, DISPLAY DRIVE AND PHASE LOCKED CLOCK

The Display Drive and Phase Locked Clock are illustrated on Diag 6.19. In this sub-section the BCD information is decoded and presented to the display, which has 12 decade windows to enable the visual information to be positioned correctly relative to the fixed decimal point Diag 6.20.

Diag. 6.14 ——▶



Block Schematic Diag. 6.14



Counters and Memory Diag. 6.15 pcb 4 (sheet 2)

COUNTERS AND MEMORY

GLUG RESYNCH (Diag 6.15)

The output from the A/D converter is a pulse train pair. The pulse trains are labelled + GLUG and – GLUG, and are transferred from the floating circuits via optical couplers. To restore synchronization the signals are gated with Clock in the dual flip-flop IC32. The input to pins 1 and 13 is for test purposes only.

COUNTER ENABLE LOGIC

Provided Main Counter Enable (MCE) SK2 pin 6 is present the resynchronized $\overline{+GLUG}$, $-\overline{GLUG}$ signals are permitted to gate Clock pulses through IC13, IC12 into the counter chain. The indirect path for each half of IC13, via IC11, provides the ÷ 2 function necessary when the instrument is operating at 20ms (4 x 9's) integration time. IC31b inputs all low.

POLARITY BISTABLE & UP/DOWN LOGIC

The direction of count is governed by two factors. Essentially $\overline{+GLUG}$ will drive the counter in one direction, $-\overline{GLUG}$ causing the count to reverse. However, if at any time the counter content is being decremented through zero, gate IC35 will detect underflow and force a reversal via IC31a and IC10a. Thus the effect of the GLUG-lines on pin 5 of each counter element is reversed. The labelled polarity of the inputs at SK2 Pins 3 and 4 is not in itself significant to the direction of count, the counter content at all times being the modulus of the input value irrespective of sign. The need for a minus sign is detected by IC38 Pin 10, and depends on the final state of IC10a. The gate is inhibited in the AC or OHMS mode. The input on SK2 pin 14 blanks decades 6 and 7 (see Fig. 6.1) during STAT period when AC is selected. (Maximum AC mode displayed scale length is 5 x 9's).

MAIN REVERSIBLE COUNTER

IC14 to IC20 plus IC10b form the 7½ decade counter chain, IC20 being the most significant "9" while IC10b can only assume a 1 or 0. The counter operates in BCD, pin 13 of each element providing the "ripple" enable to the next decade. Elements IC17, 16, 15 and 14 are capable of being held at zero by the Rate lines (SK2 Pins 8, 9 and 10) when low, so that unwanted decades are inhibited for the shorter scale lengths. Main Counter Reset ($\overline{MCR}$) generated by the Process Control circuits, provides the zero resetting on pin 11 of the counter elements at the end of each conversion.

SCALE LENGTH

For operation as a 7 x 9's instrument the complete counter is used. The coded inputs on SK2 pins 8, 9 and 10 are decoded to provide progressive inhibition of the least significant decades as the Integration time is changed. (Pin 11 set low on each IC in turn). This is illustrated in the following table:-

RATE	SCALE LENGTH	COUNTER ELEMENTS INHIBITED
10s	7 x 9's	–
1s	6 x 9's	IC14
100ms	5 x 9's	IC14, IC15
20ms	4 x 9's	IC14, IC15, IC16
1ms	3 x 9's	IC14, IC15, IC16, IC17

← Diag. 6.15

MEMORY INPUT MULTIPLEXING

Parallel to Serial Conversion is performed by IC's 21 to 24 inclusive. The outputs on Pin 6 of each being determined by the state of the select lines feeding pins 9, 10 and 11 of each converter element. The counter content is fed in serial BCD form to the data selector (IC25) on Diag 6.16

DATA SELECTOR (Diag 6.16)

IC25 a 4 x 2 line-to-1 line data selector completes the multiplexing of the Counter data into the Random Access Memory (RAM).

Control of the selector is the clock ÷ 128 output from IC2 which when low selects the counter data and when high selects the organisational data. Memory load addresses are generated by the range counter code from pcb3, fed in on SK3 pins 9, 10, 11 and 12 via IC5 when STAT is high (SK3 pin 5). The output from IC33 pin 8 determines the operation of the "RAM". When low, memory load occurs. When high, Read is selected. The 16 load pulses (during STAT) are derived from the timing counter and phased with the 16 selected input words.

DISPLAY SECONDARY ORGANISATION

The function of these elements (IC's 29, 30, 31, 33, 34, 36 and 38) is to test for certain conditions which determine what type of secondary display is necessary.

The conditions tested are:-

1) Address of word to be loaded - display digit.
2) The presence or absence of a 1 as the most significant measurement digit.
3) The operation on 3 x 9's scale length (10mΩ range) – trailing zero restoration.
4) The need for a minus sign.
5) The need for extra leading zeros in certain cases – low ranges.
6) Autorange mode – affects leading zero blanking and minus sign.

The display calls for the generation of 16 words of data, of which 12 are actually visible display information. The words are presented in two groups of 8, the first group being derived from the counter chain BCD data. The second, being generated from the Display Secondary Organisation, fills in the gaps, as it were generating all the necessary blanks and extra zero's required and in some instances, a minus sign. For convenience in the explanatory text which follows, the display windows are identified by the numbers 0 to 11, reading from left to right.

DISPLAY WINDOWS

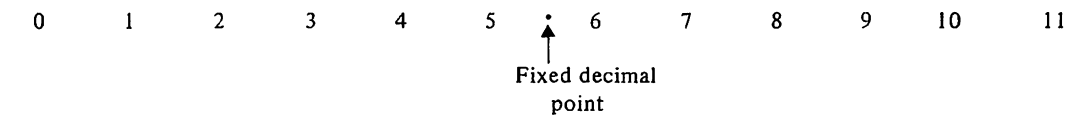


Fig 6.1

MINUS SIGN

The need for a minus sign is detected in the Polarity Bistable on Diag 6.15 . This is applied as a low on pin 5 of IC34 (Diag 6.16) . The second input to IC34 will be low if IC33b inputs are all high, i.e. Autorange is true, the msd of the measurement data is a zero and the word being scanned is not that for display windows 5, 6 or 7. This would normally generate a 'blank required' signal on IC36 pin 4, but the presence of a 'minus sign required' signal on IC34 pin 4 will override the blank. This also determines whether a zero, blank or –ve sign is displayed before the most significant 9.

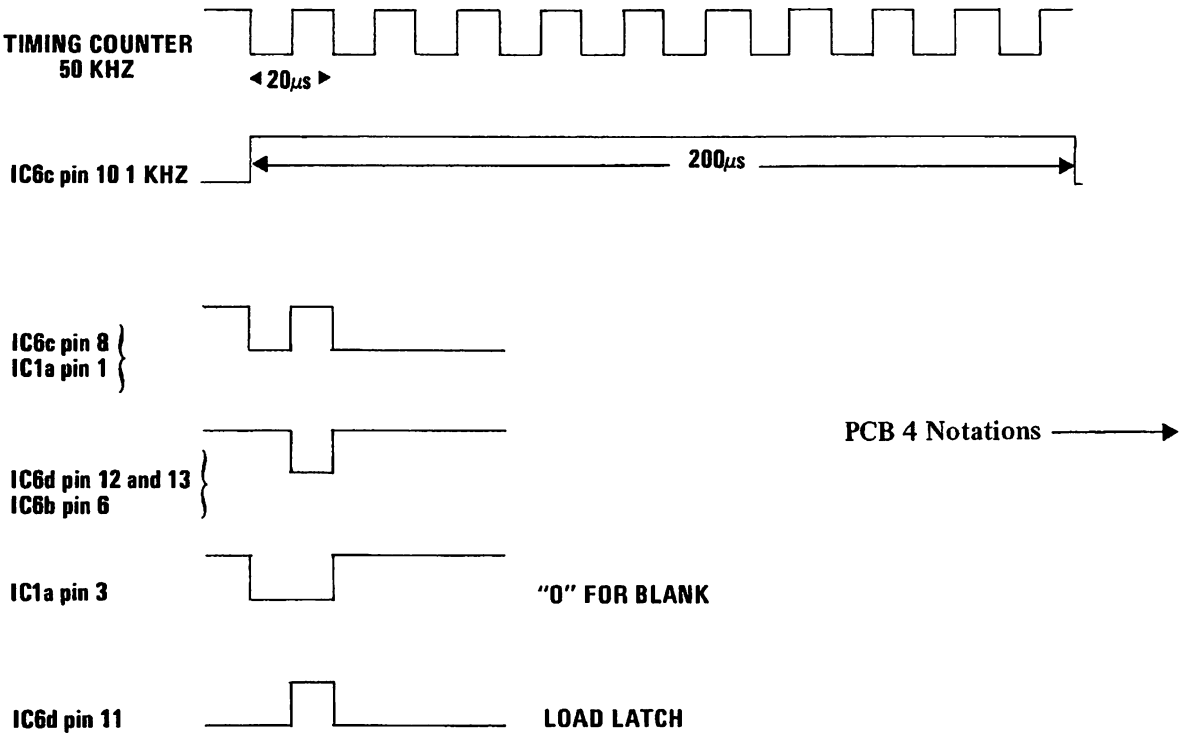
If the m.s.d. of the measurement data is not zero but 1, the minus sign for a negative quantity is normally needed one place further left than the previously described case. The element involved is IC29b whose output will be high. Additionally the memory address being loaded is address 7 i.e. the last to be loaded of secondary organisation. The high on pin 6 of IC29b will set IC25 output pins all low, which will cause the memory to output 1.1.1.1., which is the minus sign code.

There is a further special case requiring a secondary organisation minus sign, necessitated by the convention of preceding a fractional number with a zero before the decimal point. The display organisation normally inserts a minus sign before the m.s.d. of the displayed value, which for the 100mV and 10mV ranges would be position 5 or 6. Since this would result in, for example, (on the 100mV range), a display of "−.414", it is necessary to force a zero into position 5 and re-insert the minus sign in position 4. IC38 pin 3 goes low when position 4 word is being scanned enabling IC30 pin 4 to allow a minus sign if required, to force IC25 pin 6 to a low. Similar logic determines the position of Blanks in the display entered by the inverted codes on IC25 pins 13 and 10.

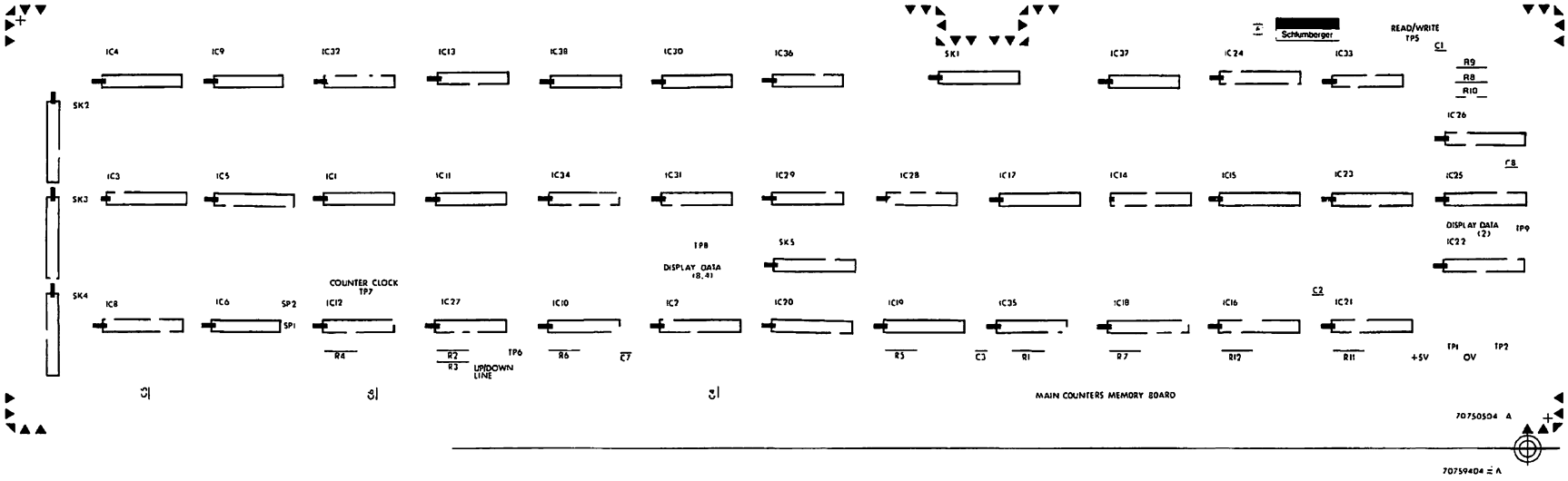
When the instrument is operating on the 10MΩ range at the 3 x 9's scale length, the input on IC34d pin 11 in conjunction with STAT from pcb 3 forces IC17 to register a zero for display in the decade window immediately preceding the decimal point i.e. position 5.

MEMORY DISPLAY MODE

The data previously loaded into memory are output to the display circuits under the control of the display scanner (IC1). The timing counter 50kHz output is gated via IC6b (pin 6) with a 1kHz pulse train, both pulse trains derived from the timing counter divider stages, the resulting gate pulse on IC6c pin 8 is used to enable the scanner (the address lines being pins 3, 4, 5, 6) accessing the two "words" needed for the digit pair to be displayed. The scan is such that no two digit pairs are ever addressed in sequence (bits 8 and 2 being transposed for this purpose)
IC6d pin 11, the inverse of IC6b pin 6 is used as a load latch for the righthand digits in the display drive circuit. When they are being latched, the selected display element pair is blanked by the low on IC1a pin 3 via SK3 pin 8.

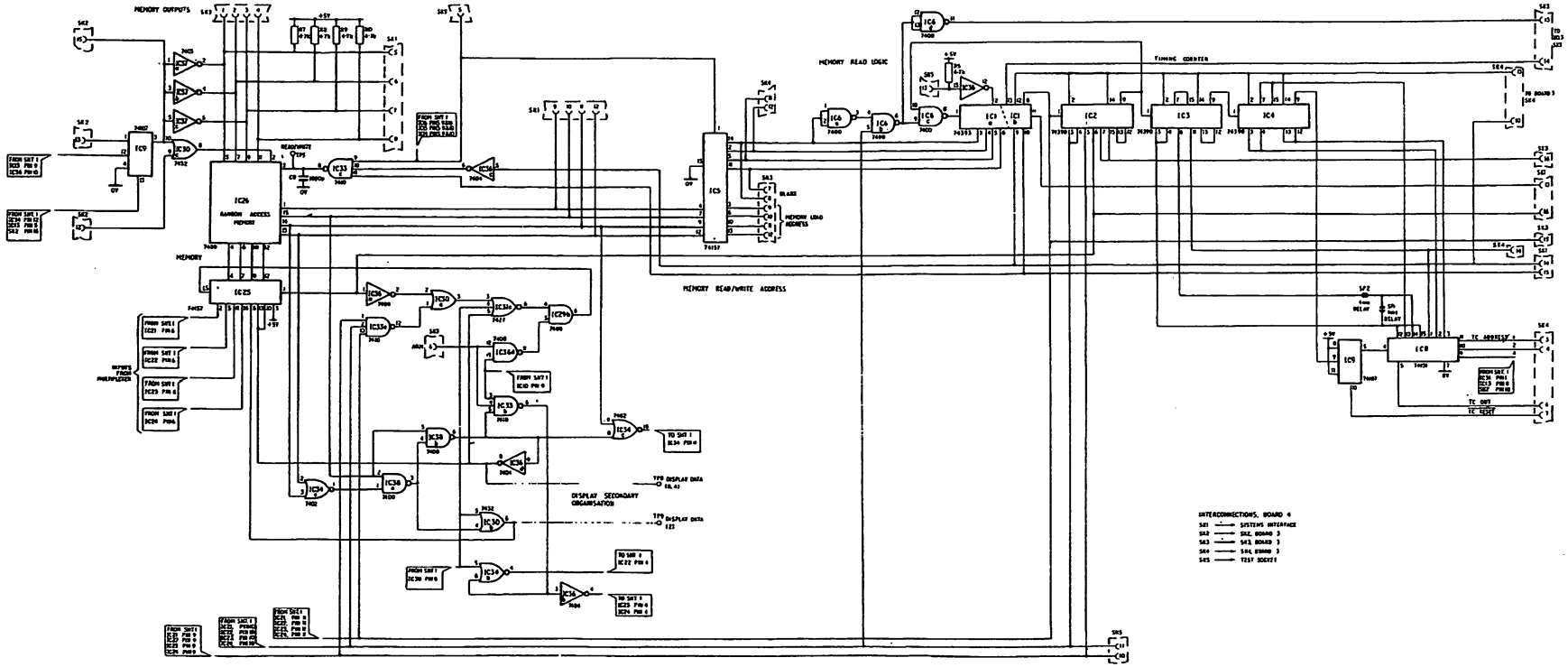


MEMORY DISPLAY MODE

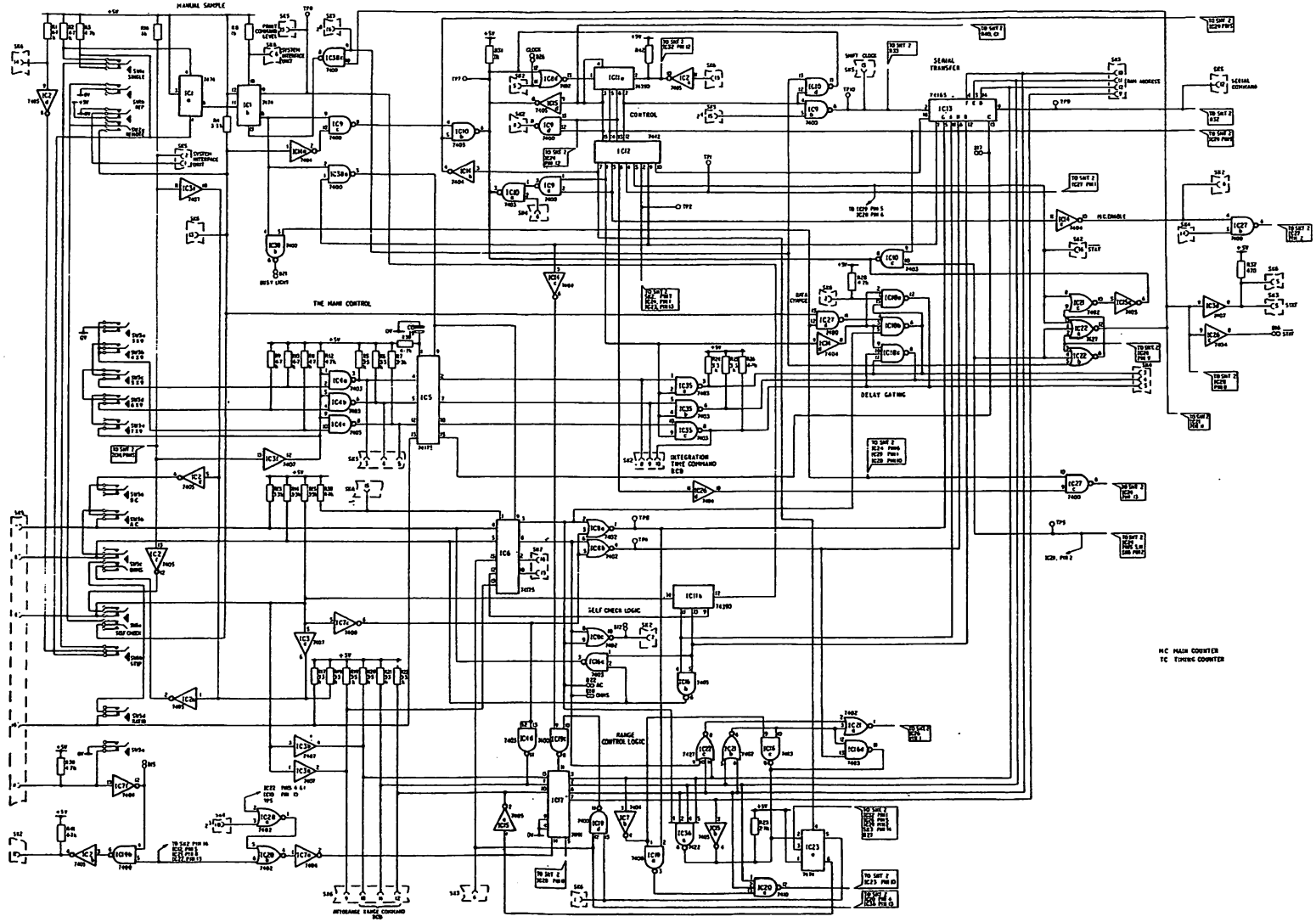


PCB 4 Notations

PJL/7075/3



Counters and Memory Diag. 6.16 pcb 4 (sheet 1)



Control Board Diag. 6.17 pcb 3 (sheet 1)

CONTROL LOGIC (Diag. 6.17, 6.18)

IC11a is the "state" counter, decoded into the 10 states by IC12. At anytime one of the10 outputs of IC12 will be low.

The states, advanced by a low at TP7 synchronously with the 1.6MHz clock are tabulated below, and described in sequence, starting at state ⑨ , the state that accepts a digitise command.

7075 CONTROL SEQUENCE

CODE		ACTION	IC12 PIN No.	TERMINATED BY
6	0110	HOLD – waits for Dig Command unless "not-in-Remote", overload or in Rep.	7	(i) CLOCK (in Rep) (ii) Overload (on Autorange) (iii) Dig Command
7	0111	LOAD – Integration & Mode latches. Range counter if not in Autorange serial transfer Shift Register	9	CLOCK
8	1000	SERIAL TRANSFER (Floating & Fan-out)	10	TIMING COUNTER
9	1001	(Not Used)	11	CLOCK
0	0000	DELAY PERIOD before Measurement Start	1	TIMING COUNTER
1	0001	RESET Autorange ccts & ÷ 2 bistable on Bd. 4	2	CLOCK
2	0010	MEASUREMENT PERIOD	3	TIMING COUNTER
3	0011	PULSE BEFORE STAT – Samples down-range system	4	CLOCK
4	0100	STAT – Memory Write Sequence Resets Dig Command & Print Command Autorange counter reset	5	TIMING COUNTER OR CLOCK (if autoranging)
5	0101	PULSE AFTER STAT – resets Main Counter resets "O/L during HOLD" bistable	6	CLOCK

OPERATION

State ⑤

State ⑥ enables IC10b pin 5. IC10b pin 4 will go high, putting a low on TP7 to advance control for a low on either IC9d pin 9 or 10. If in "REP" IC14a pin 1 will be high making IC9c pin 10 low and control will advance to state ⑦ on next clock. If in "SINGLE" sample IC14a pin 1 will be low. The system is therefore waiting for a low on IC1b pin 8 from either a remotely commanded digitise command on IC1b pin 10 or a front panel command via the anti-bounce latch IC1a from the single sample switch.

State ⑥ can also be advanced by an overload signal via IC10c – see autorange system.
State ⑧ resets range error bistable IC23a.

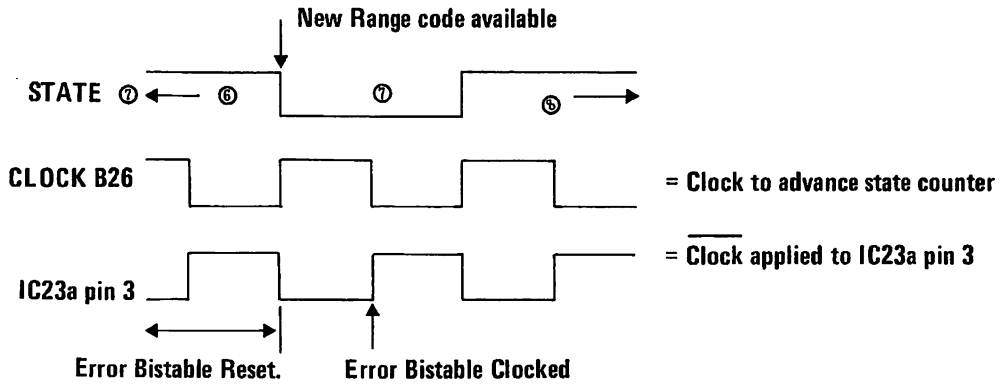
◀——— Diag. 6.17

State ⑦

Integration and Mode latches (IC5 and IC6) are loaded. If in remote these latches are already loaded via IC38a pin 2.

IC17 the range counter is loaded via IC19c pin 9 if IC19d pin 12 or IC19d pin 13 is low. IC19d pin 12 will be low if not in Autorange. IC19d pin 13 will be low if the error bistable detects an incorrect range code, putting a low on IC23a pin 5 when clocked, which corrects and resets the range counter.

When state ⑦ ends the shift register IC13 will be loaded (IC13 pin 1) with the final range and mode information. As it is an odd state (IC11a pin 3 = high) it is terminated by clock via IC15d holding TP7 low. Also it will have reset the Timing Counter via IC7d, e, and the measurement counter via IC9d.

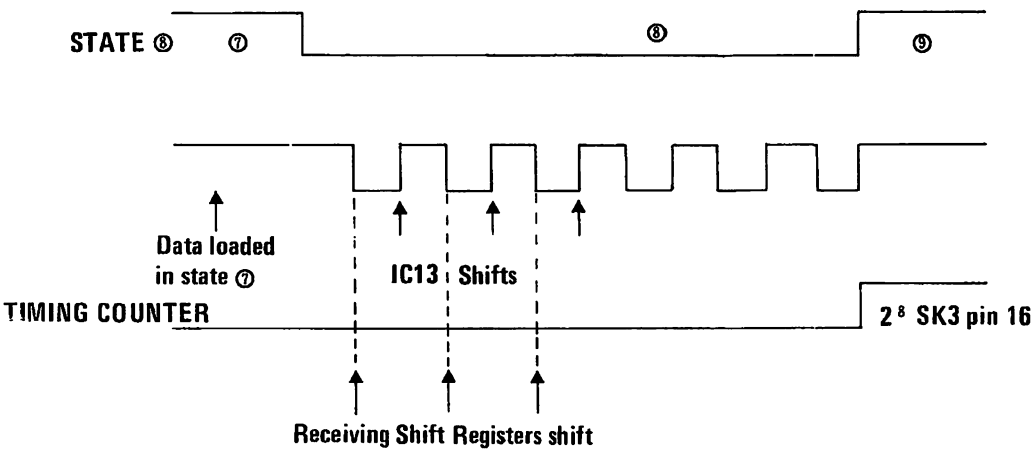


State ⑧

IC13 is now ready to transfer its information to the floating logic on board 6 via the opto-couplers IC30 and IC31 and to the systems interface unit (S.I.U.) if fitted.

IC11 pin 7 is high enabling IC9b to pass strobe pulses on SK3 pin 15 (from the 4TH output) down the timing counter chain (2^4) to the clock input; to the shift registers IC13; via SK5 pin 13 to the receiving shift register in the S.I.U. and via opto-coupler IC31 to the floating logic. IC13 pin 2 is enabled by IC12 pin 10 being at a low, and shifts on the positive edges. The receiving shift registers are arranged to shift on the negative edges to allow for data settling time.

This state is terminated by a high from the 8th output of the timing counter arriving at SK3 pin 16 enabling gate IC10d, (already enabled by IC11a pin 7), putting a low on TP7 to advance IC11a on the next clock edge.



CONTROL BOARD WAVEFORMS

State ⑨

State ⑨ is not used, clocked to state ⓪ as it is an odd state.

State ⓪

This state lasts for the time needed for analogue settling before a measurement starts. The required delays are normally 20ms unless:-

1) SIU determines no command changes since the last measurement, in which case it puts a low on IC18a pin 1 requesting a 4ms delay only.

2) AC mode and Single measurements or Autorange change – 800ms delay.

Operation 2) has priority over 1).

IC35a, b and c is disabled by state ⓪ (IC12 pin 1 low). Codes set up on SK4 pins 3, 4 and 5 by IC18a, b and c and IC27a address the output of the Timing Counter, which will go high after the required delay. This is applied to SK4 pin 6 which enables gate IC10a already set up by state ⑤ to put a low on TP7 to advance IC11a.

Codes to Timing Counter:-

	SK4/ 3	4	5
20ms	1	1	0
800ms	0	1	1
4ms	1	0	1

State ①

Resets autorange bistables IC24a, IC23b
Resets ÷ 2 bistable for 4 x 9's rate.
Resets Timing Counter via IC7d and e.
Terminated by clock as odd state.

State ②

This is the measurement period. The code for the required integration time is held in IC5 and applied to the timing counter via IC35a, b, c and SK4 pins 3, 4 and 5.

The Codes are:-

	SK4/ 3	4	5
1ms (3 x 9's)	1	1	1
20ms (4 x 9's)	1	1	0
100ms (5 x 9's)	0	1	0
1s (6 x 9's)	1	0	0
10s (7 x 9's)	0	0	0

Similar codes on SK2 pins 8, 9 and 10 select the required measurement counter length. The codes are either encoded from the front panel switches SW3a to SW3e or from the S.I.U. via SK5 pins 3, 4 and 5. In the latter case IC4 a. b. and c. are disabled by SK5 pin 2 via IC3f.

This state will be terminated by either:-

1) The "time-up" signal on SK4 pin 6 from the timing counter. IC10a enabled by state ② via IC9a
or
2) By an autorange decision via IC10c enabled by state ② or ⑥ by IC11a pin 5. (See Autoranging).

State ③

This is an odd state and so if resets the timing counter ready for state ④ . It also samples the autoranging system for a "slow-down" range decision in case this has not already been made during state ② (see autoranging).

State ④

Memory is loaded with display data measurement and status information during state ④ and the same data is sent to the S.I.U. via SK1 pins 5, 6, 7 and 8. It is normally terminated by the timing counter 8th output on SK3 pin 16 via IC22b, IC21c and IC15c, putting a low on TP7 to advance IC11a on the next clock edge.

It may be by-passed by the autoranging system placing a high on IC22b pin 4 which will inhibit STAT on IC22a pin 12 and advance IC11a immediately on the next clock pulse.

STAT normally lasts for 80μs during which time there are 16 pulses on SK4 pin 10, the 2nd output of the timing counter. These, clock the binary counter through its 16 states, starting and finishing on the same range code. The range counter is reversible and the direction is determined by IC17 pin 5. This is held low (count up) by IC28c pin 10 since IC28c pin 8, is high (STAT).

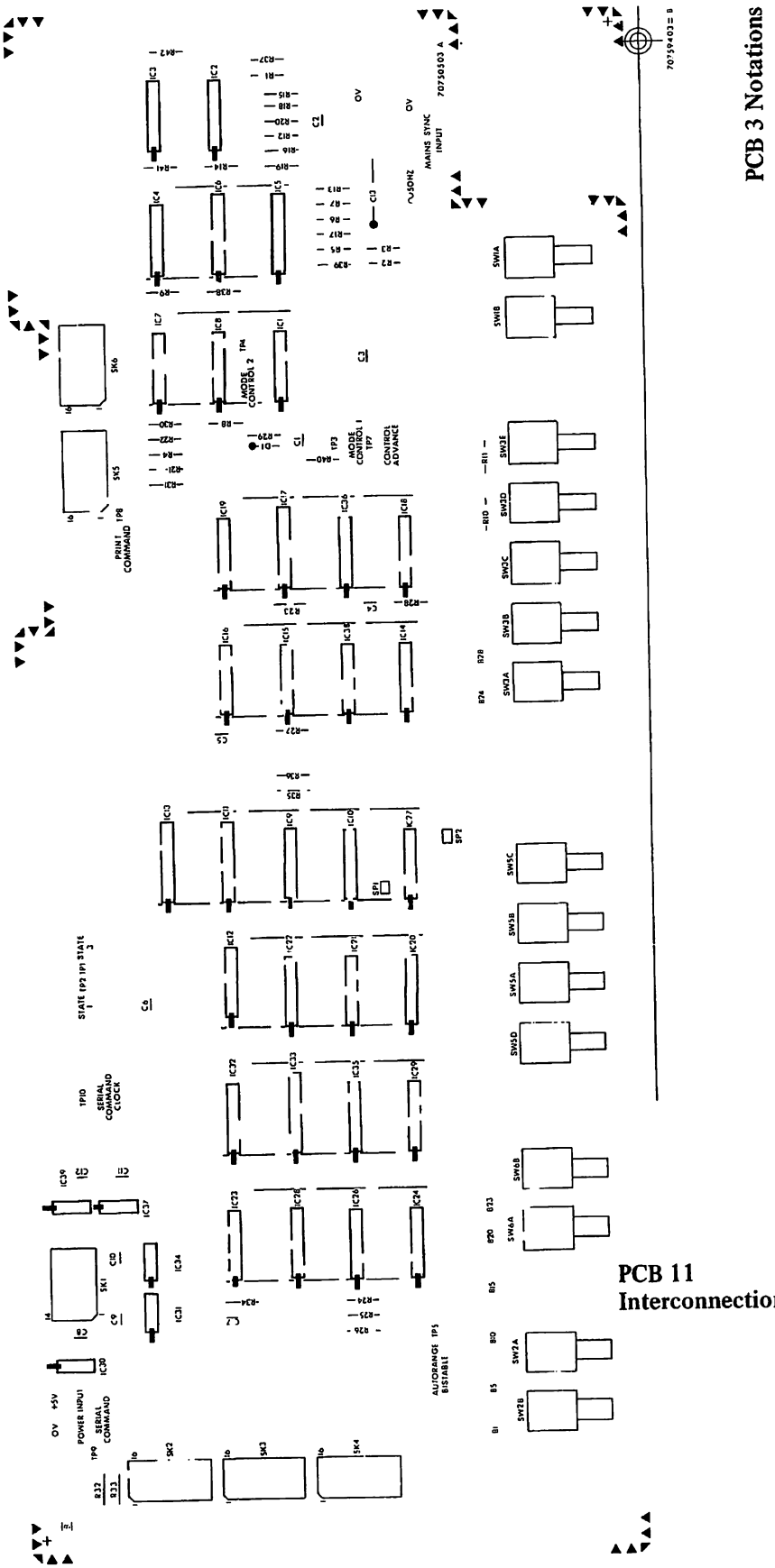
If state ④ is being by-passed by the autoranging system, IC28c pin 8 is held low by IC22a pin 1 at a high. Instead of 16 pulses there is now only one. IC28b pin 6 is low (IC12 pin 5 low in state ④). IC28a pin 2 is high and blocked, so as state ④ passes there is one pulse on IC28b pin 4 which is delivered to IC17 pin 14. This changes the range code. Clock input to IC17 while high during state ④ ensures correct direction of count.

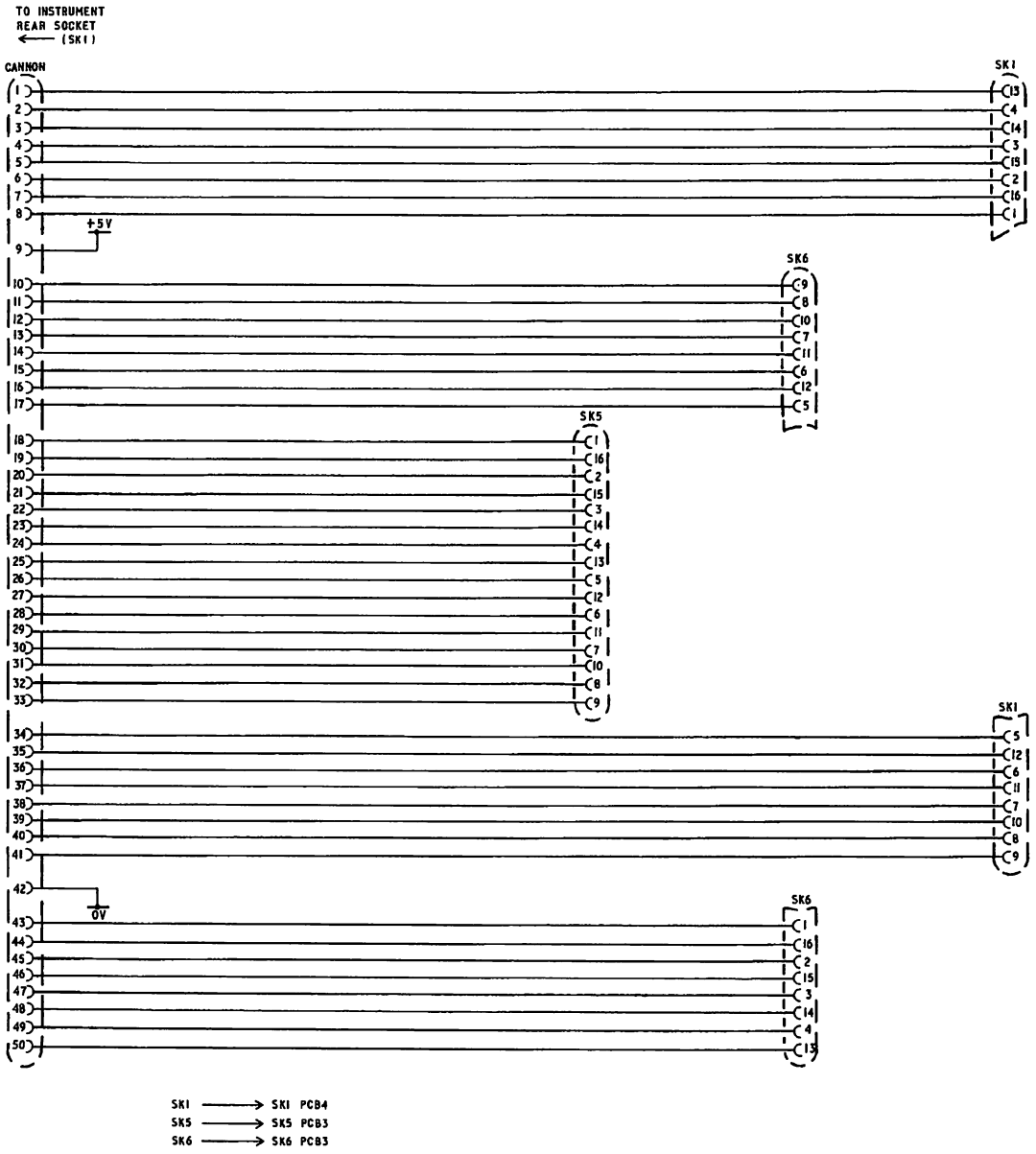
State ⑤

Resets measurement latch via IC9d.
Resets timing counter via IC7d and e.
Resets latch in autoranging system.
Terminated by clock (odd state).

State ⑥

As before.


PCB 3 Notations
PCB 11
Interconnections
MAINS SYNC INPUT
~50HZ
0V
POWER INPUT
SERIAL COMMAND
PRINT COMMAND
MODE CONTROL 2
MODE CONTROL 1
CONTROL ADVANCE
SERIAL COMMAND CLOCK
AUTORANGE BISTABLE
SK1
SK2
SK3
SK4
SK5
SK6
SW1A
SW1B
SW2A
SW2B
SW2C
SW2D
SW2E
SW3A
SW3B
SW3C
SW3D
SW3E
SW5A
SW5B
SW5C
SW5D
SW6A
SW6B



DVM TO S.I.U. INTERCONNECTION BOARD

PCB 11 Interconnections

AUTORANGING SYSTEM

IC32a, 33a and 33b are the autorange counters. Should the presence of either GLUG (IC38 pin 13 or 12 low) occur during state ② and state ⑥ IC11a pin 5 gates IC29c pin 9 enabling the autorange counters. They are reset at all other times.

During a GLUG there will be at least one transition of output (IC33a pin 9) if the GLUG is larger than the size of GLUG corresponding to the down range point.

For a steady DC input voltage to the analogue system there will be at least one GLUG larger than the critical size if the input value is greater than the down range value. This incident will clock IC23b and prevent a down range decision (see later).

Similarly for an input greater than the up range value, there will be at least one transition of output IC33b pin 11 with IC33a pin 9. This will pass through IC35d, IC26 pins 3 and 4 and IC36b pin 12 to clock IC24a, the main autorange bistable. In both cases the information is OR-ed with information from the measurement counter on board 4. Should the measurement count exceed the up range value SK4 pin 8 will go low at least once. Should the measurement count exceed the down range value SK4 pin 9 will go low at least once.

The system will therefore up-range if:-

1) Any GLUG exceeds the size equivalent to that obtained with a steady input equal to the up range value.

2) The top range for the mode has not been reached.

3) Autorange is enabled.

The system will down-range if:-

1) During the measurement or the first 20ms there are no GLUGS greater than those obtained by a steady input at the down-range point.

2) It is not already on the bottom range.

3) It is in the autorange mode.

IC24a and IC23b (the autorange and down range bistables) are reset before a measurement starts on state ① . If during a measurement, the main reversible counter output or a GLUG greater than the down range value occurs, IC15e pin 10 will go low. This will clock IC23b to prevent down ranging on the next clock IC29a pin 2, if IC24a is not already set (IC29c pin 9). If on the bottom range IC23b will be set anyway (IC23b pin 10).

The down-range bistable will be sampled by either the 20ms output from the timing counter IC26b pin 6, or state ③ (IC27a pin 1), by IC20b pin 3 to set the main bistable IC24a if autorange is true (IC20b pin 4) to start an autoranging sequence. IC24a will terminate state ② or state ⑤ if not already finished, inhibit state ④ , and increment the range counter by one during the passing of state ④ in the direction determined by IC28c pin 10. As STAT is inhibited (IC28c pin 8) the direction will be determined by whether IC23b had been clocked or not (i.e. if not clocked – down range).

An overload signal from the GLUG counter or the main counter will clock IC24a directly (providing IC23b had already been clocked up-range). State ② and ⑥ will be terminated immediately. To do this Autorange must be true (IC36b pin 13) and the top range must not have been reached (IC26a pin 1).

If an overload occurs while in state ⑥ and the system is not in remote, the main autorange bistable (IC24a) will terminate state ⑥ (subject to the usual conditions. i.e. Autorange must be true and not on the top range) and start a measurement cycle. A normal upranging sequence will follow. IC24b inhibits STAT and Print Command until the autoranging is complete. It is reset on state ⑤ if the main autorange bistable is reset.

IC27c on pcb 4 detects a count of "14" which is the range overload point, the output on SK4 pin 8 causing up-range to be actioned on pcb 3. The other output (IC27c pin 8) locks-out the clock at full scale "freezing" the counter action.

IC12c also on pcb 4 detects the "12" condition producing down-range at SK4 pin 9. Down range automatically occurs every conversion or 20ms after conversion start whichever is the shorter time, unless during that time it is inhibited by the output from IC12c.

FLASHING LOGIC

Under normal conditions IC29e and IC20c latch is reset. IC29e pin 13 detects analogue overload, IC29e, and IC20c latch. IC32b pin 8 produces a 12.5Hz pulse train which resets the latch while low causing the display to "flash" for as long as the overload persists.

To prevent flashing during auto/normal range change, a low is applied via IC20c pin 10.

To ensure that invalid readings are not displayed during memory update, a blanking pulse is applied to B16 which inhibits IC12 and IC11.

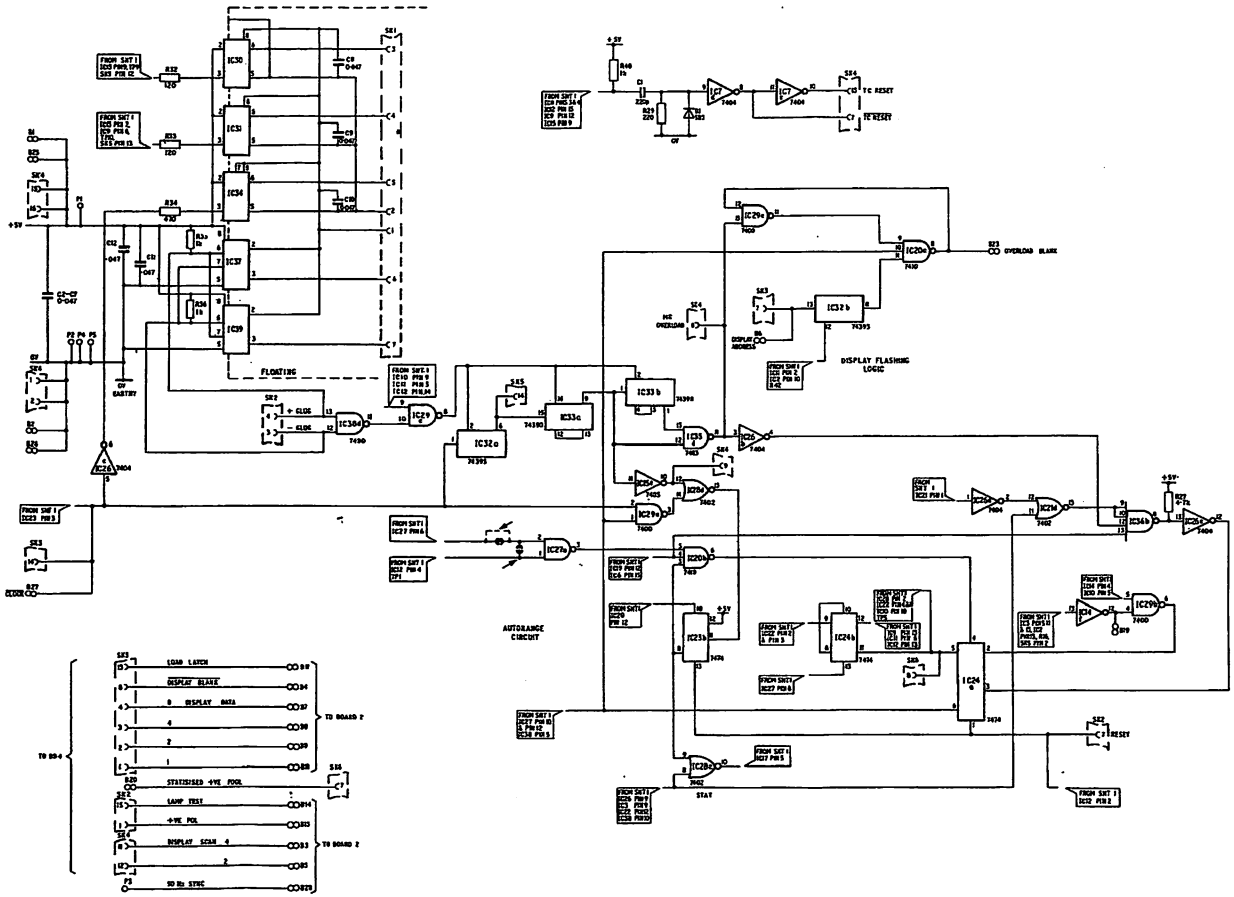
SELF CHECK LOGIC

In the instrument self check mode, the OHMS, AC and DC front panel switches are disabled (IC2f, IC2c and IC3e). Autorange is also disabled via IC3a. IC17 is set via IC3b, by range code 0 1 1. S.I.U. and fan-out are informed from IC8a pin 1 and IC8b pin 4 via IC13 pins 5 and 6. Self check codes are also sent via IC13 pin 11 and 12. The appropriate self check codes are then formed for each test.

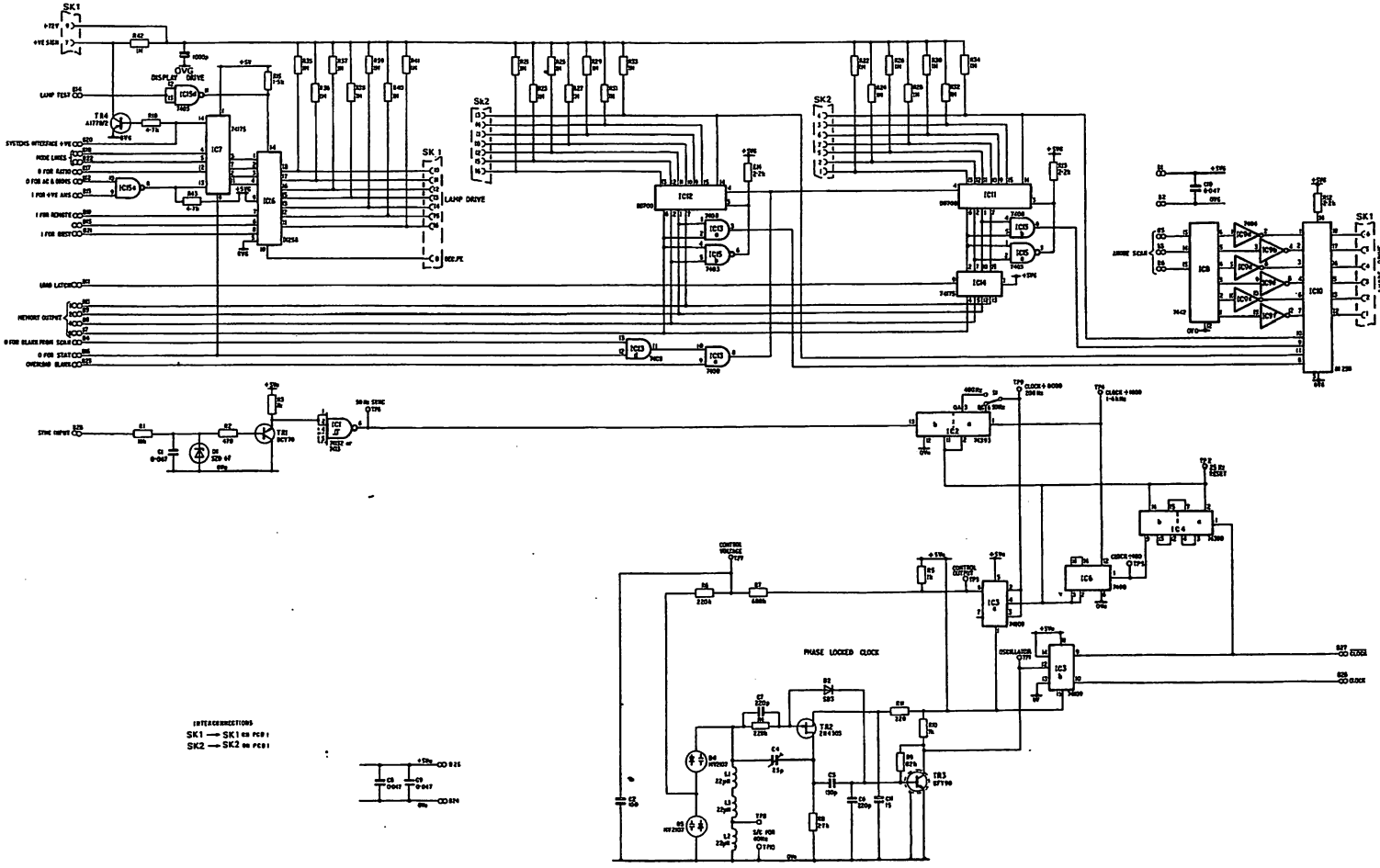
The information displayed during the self check of the instrument through its 5 sequential steps is given in section 2.

PCB 11

Enables the rear panel socket SK1 for instrument use with ATE in a systems environment.



Control Board Diag. 6.18 pcb 3 (sheet 2)



Display Drive and Phase Locked Clock Diag. 6.19 pcb 2

THE DISPLAY, DISPLAY DRIVE AND PHASE LOCKED CLOCK

PHASE LOCKED CLOCK (Diag 6.19)

A mains derived synchronising signal is shaped by R_1, C_1, D_1, and buffered by TR1 before being applied to IC1. The output from this gate is a repeatable, free from bounce, 50Hz signal but possibly of unequal mark-space ratio. IC2 divides this signal by 2 giving a 25Hz output (TP2) with an equal mark-space ratio.

The voltage controlled clock oscillator is phase locked to the mains frequency. Voltage to frequency adjustment is achieved by C4. For 50Hz operation with a control voltage of 2.2V, frequency should be 3.2 MHz. For 60Hz (TP8 connected to TP10) operation and a control voltage of 2.2V, frequency should be 3.84MHz. Frequency control is by varactor diodes D4 and D5.

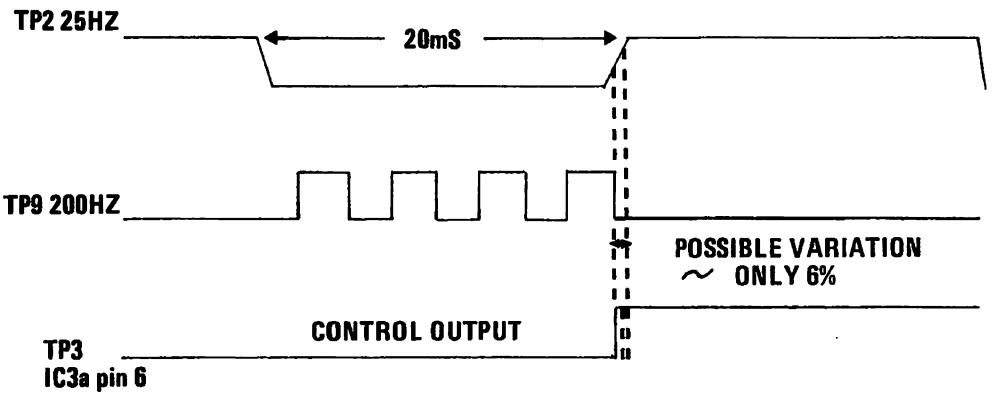
TR3 acts as a buffer, its output (TP1) is applied to the counter chain, the final output of which is 200Hz.

OPERATION

When the level of the synchronising signal (TP2) is high, the counter is held in reset; when it goes low, the chain is enabled. As it returns to the high state, IC3a is clocked and the state of the final 200Hz output is stored until the next cycle. Should the final 200Hz output be high at this instant, the clock is running too slow. Should it be low, the clock is running too fast.

A high on the control voltage tends to reduce the capacitance of D4 and D5 thereby increasing the clock frequency and vice versa. Because the possible error in frequency is 6% maximum, there is no likelihood of sampling the wrong output pulse.

The control voltage is averaged and smoothed by R7, C2 so that a gradual control is achieved. In lock the decision tends to alternate on consecutive samples giving a small slow ramping of the clock frequency. The effect of one decision is arranged to be very small, therefore the extent of the final jitter is also very small.



PHASE LOCKED CLOCK

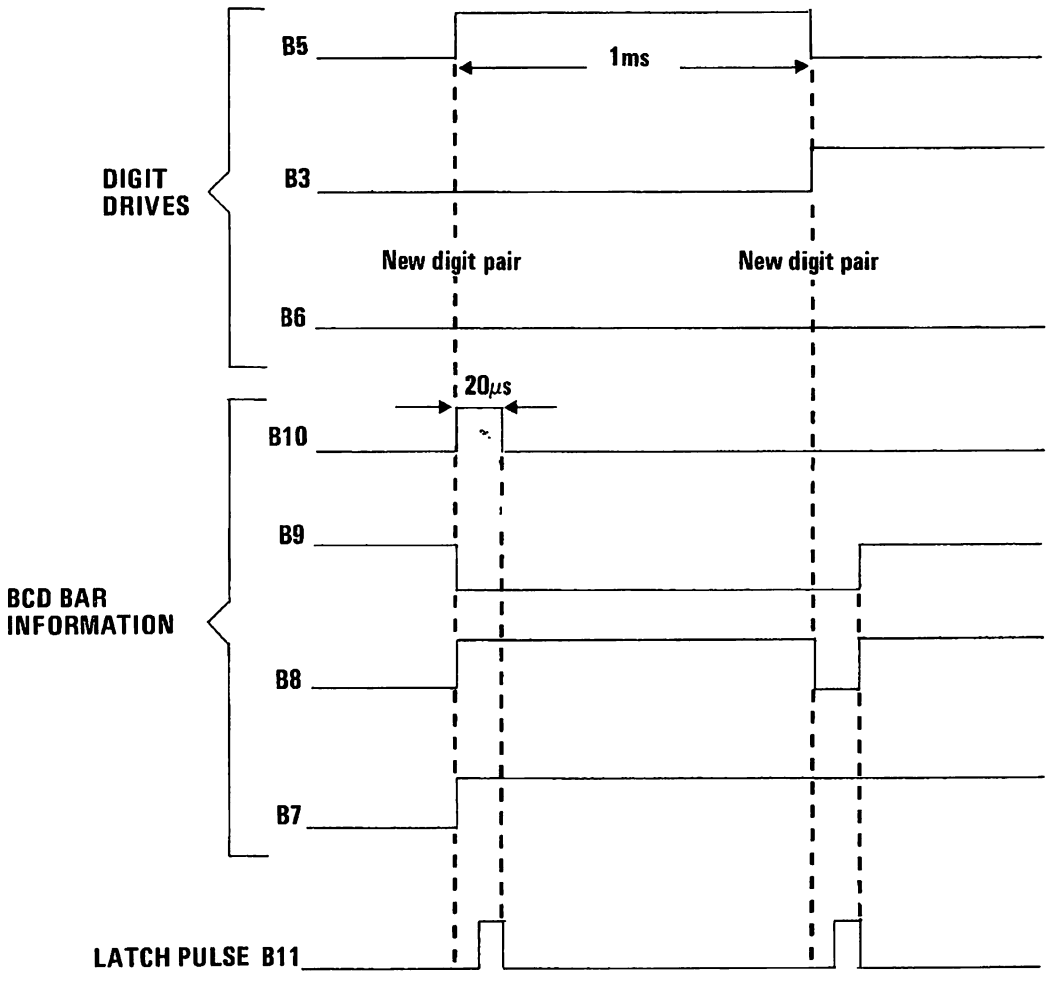
← Diag. 6.19

THE DISPLAY DRIVE

The display is multiplexed, two digits at a time on a 1 in 8 duty cycle. Digit pairs are selected by the BCD information on B5, B3 and B6, decoded by IC8 and level shifted by IC10 to the anode switches on the display board.

For each new digit pair addressed, two sets of 7 bar information are required. These appear, in BCD, on B10, B9, B8 and B7. One set of information is applied for 20μs and stored in IC14, gated by a latch pulse on B11, thence decoded by IC11, IC13b and IC15a (special codes) to drive the left hand digits.

The second set of information is applied for the remainder of the multiplex period, decoded by IC12, IC13a and IC15b driving the right hand digits.



DISPLAY DRIVE WAVEFORMS

The BCD codes are:-

Character	BCD	
0 TO 9	0 TO 9	
A	1 0 1 0	NOT USED
B	1 0 1 1	
BLANK	1 1 0 0	Generated by IC15a
	1 1 0 1	Generated by IC15b
NEGATIVE SIGN	1 1 1 0	Generated by IC13a
	1 1 1 1	Generated by IC13b

R13 and R14 program the current drive to the segments of the display. R21 to R34 clamp the unlit segments to the 75V rail.

When the information for the left hand digit is being accessed, the selected display element pair is blanked by a low applied to B4 which inhibits IC12 and IC11 for 20μs.

ANNUNCIATOR DRIVES

Information for the annunciators appears on B20, 18, 22, 17, 12, 13, 19, 15 and 21. Some lines are latched in IC7 before being applied to IC16 (level shifter). R15 programs the current drive to all the neon annunciators. A high input on B14 removes this program current and blanks the annunciators on lamp test.

Unlit annunciators are clamped to the 75V rail by R35 to R41 to ensure that leakage currents do not cause faint discharges.

THE DISPLAY (Diag 6.20)

An 11 x 9's display is used to facilitate a 7 x 9's scale length in conjunction with the fixed decimal point.

The display decades are 7 bar co-planar gas discharge type.

ANNUNCIATOR DISPLAY

V5 to V10 provide the following annunciator displays:- VOLTS, kΩ, BUSY, REMOTE, RATIO and AC.

The travelling minus sign is derived from the centre segment of each display element, the positive annunciator is not used.

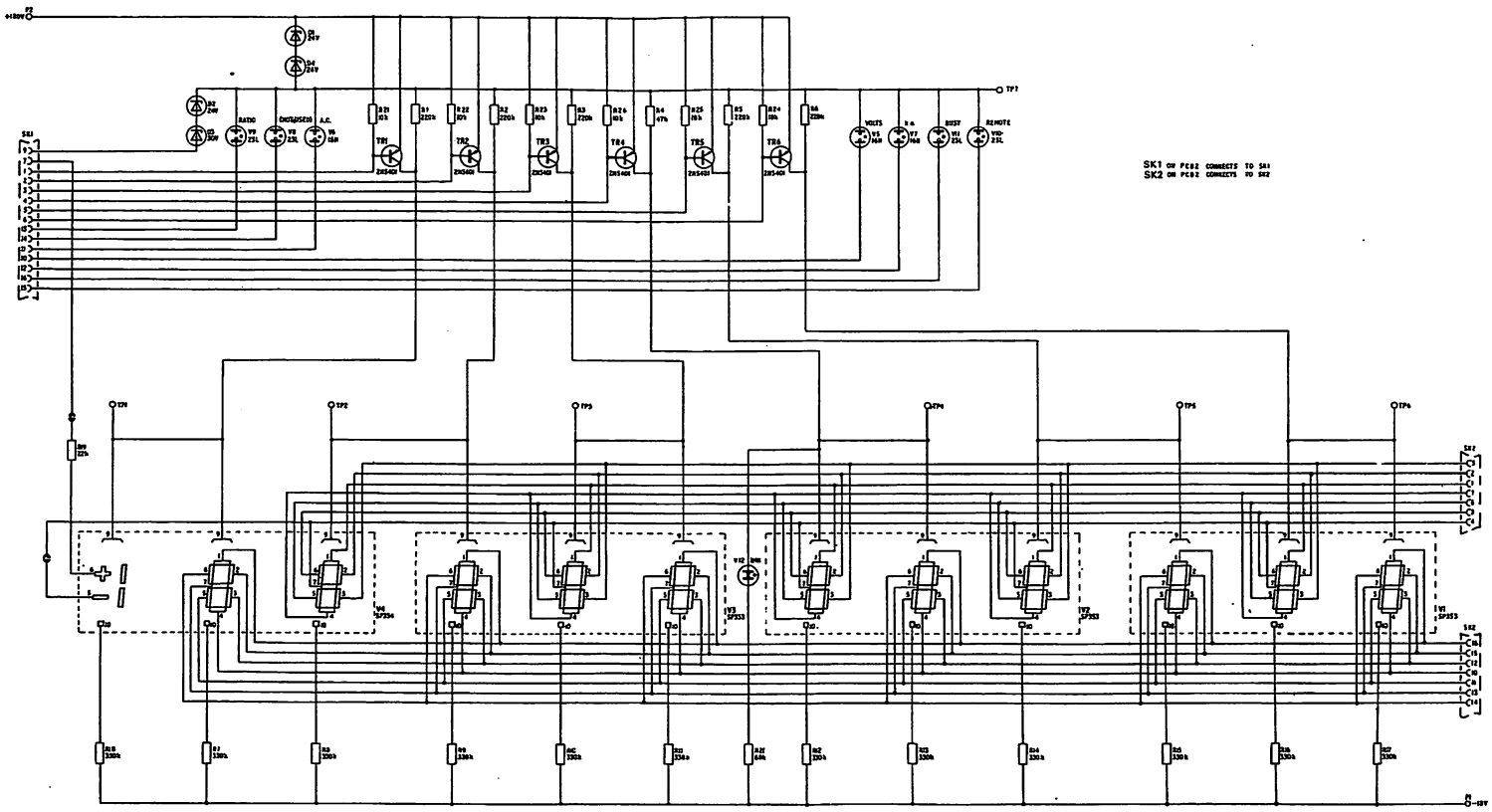
The VOLTS, kΩ, REMOTE, RATIO and AC annunciators are illuminated on selection of the appropriate function or control button.

The BUSY annunicator is illuminated during range change and on overload. When this occurs, the readings should be regarded as invalid. The annunciator is extinguished when the new range is settled upon, when the new result is displayed, and/or when the overload is removed.

The BUSY signal has the additional function of inhibiting the front panel push buttons, thus once a command has initiated a measurement, the instrument will not abort that reading.

PCB 1 Notations ⟶

PCB 1 Notations



Display Diag. 6.20 pcb 1