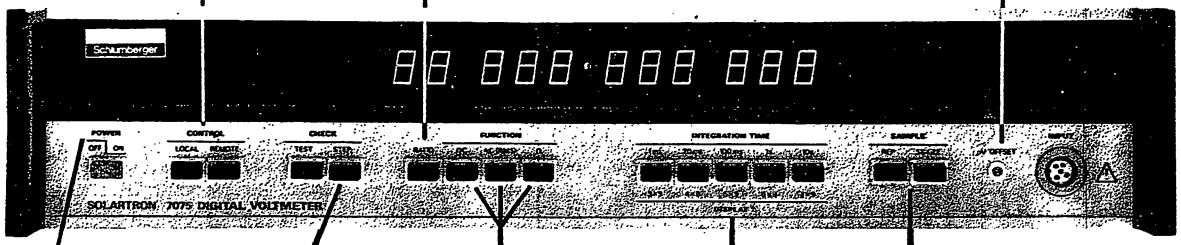
CONTROL: Permits operation by means of front panel switches, when on LOCAL; or under the control of an external system when REMOTE is selected. REMOTE has no effect in the absence of an Interface Unit. (Note 1).

RATIO: Disconnects internal reference and connects external reference applied to the rear input terminals.

μV OFFSET: Facility for offsetting the effects of externally generated emf's. Applicable on DC and Ω.



DC, AC (RMS), Ω : Used for selection of measurement mode.

REP: Display is repeatedly updated at a rate set by the selected Integration Time.

SINGLE: Display retains last commanded reading. Update occurs each time button is pressed (Note 2).

TEST: Initiates a series of self-check operations.

STEP: Progresses the test routine step-by-step.

INTEGRATION TIME: Choice of 5 scale lengths by selecting one of 5 integration periods. The longer scale lengths give greater resolution.

POWER: Push-on/push-off. Applies mains power to the instrument. No remote control facility.

NOTES

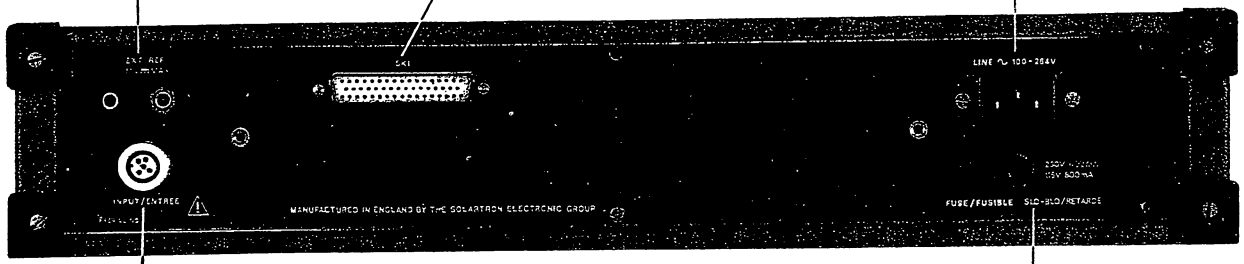
1. An external command from the Interface Unit, FRONT PANEL LOCKOUT, can be used to inhibit all front panel controls (except POWER).

2. When in SINGLE operation, changes of FUNCTION or INTEGRATION TIME will not be implemented until the SINGLE button is again pressed.

CONNECTOR SOCKET SK1 for use with Systems Interface Unit or data processing options.

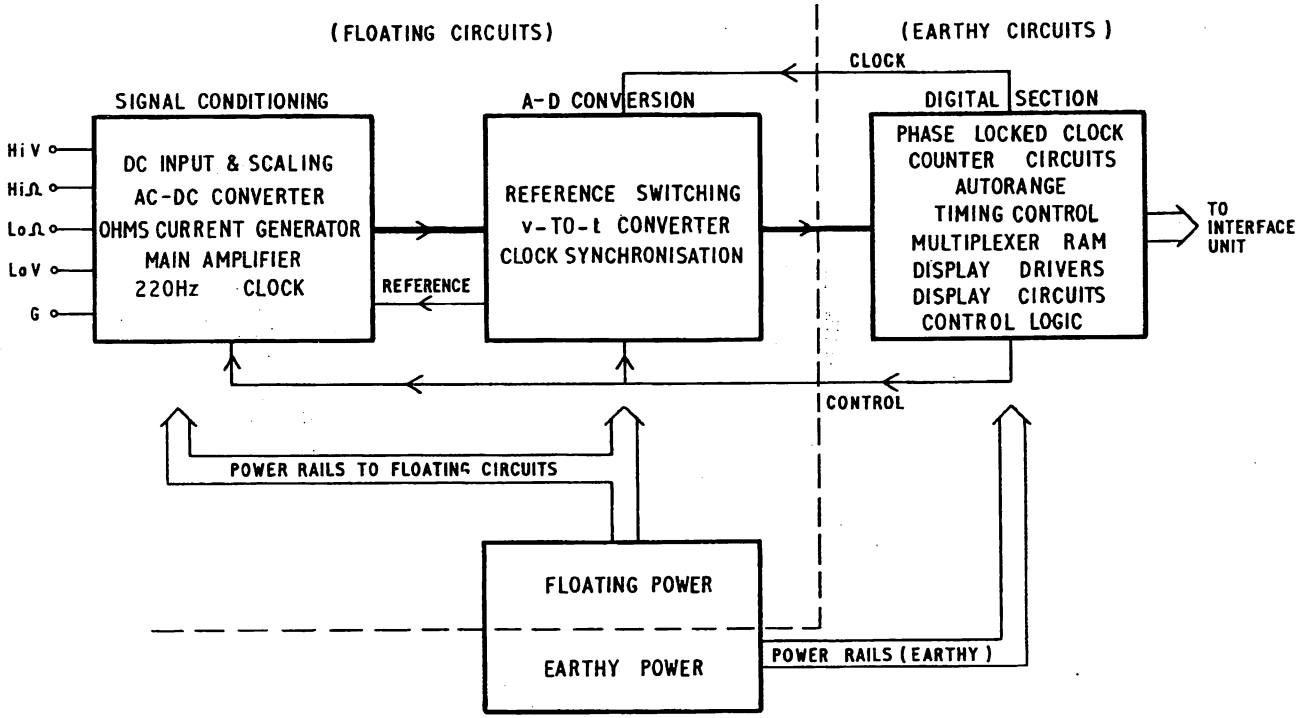
EXTERNAL REFERENCE terminals used only for RATIO measurement.

POWER INLET SOCKET. No voltage tappings are required over the stated range.

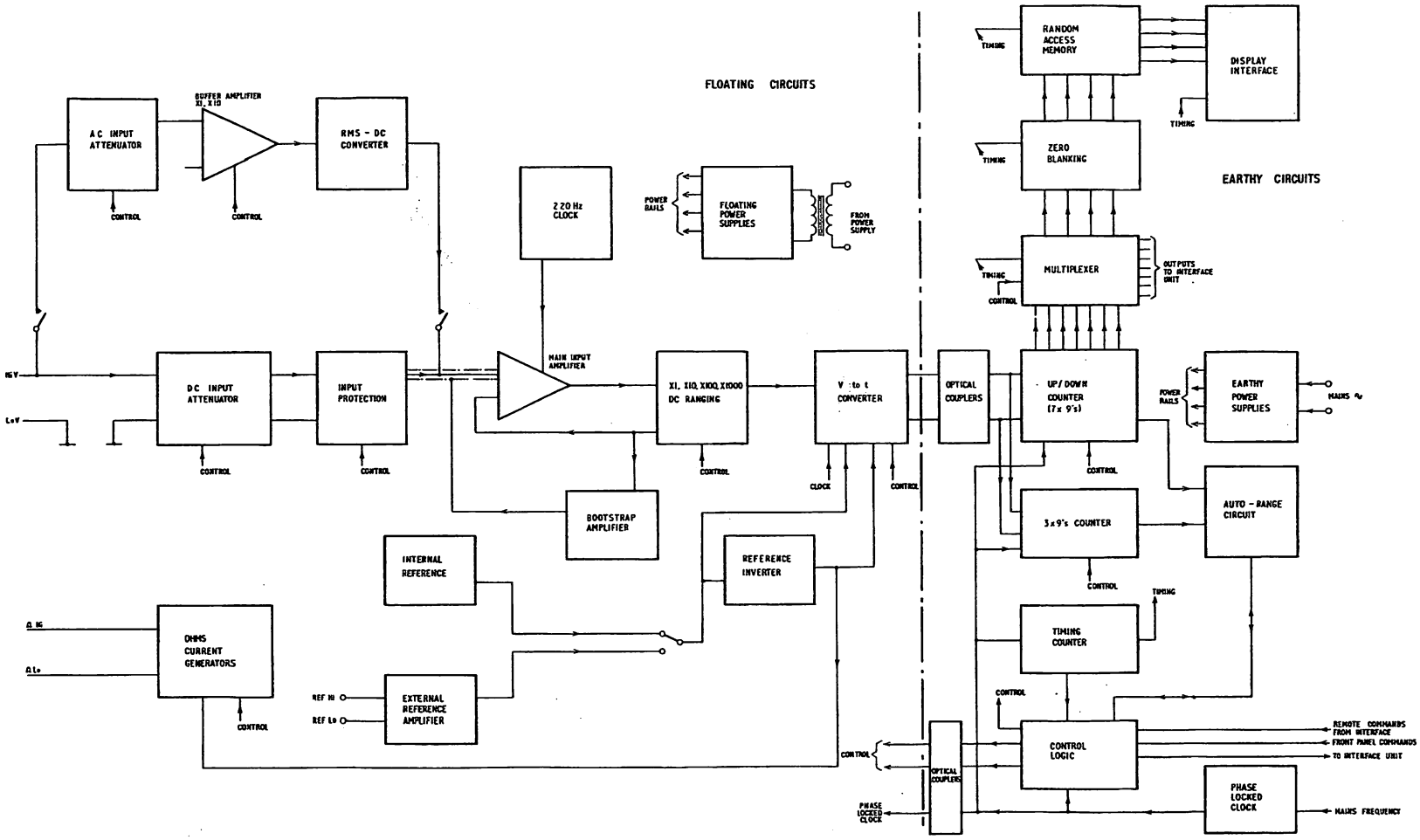


REAR INPUT SOCKET wired in parallel with normal front input.

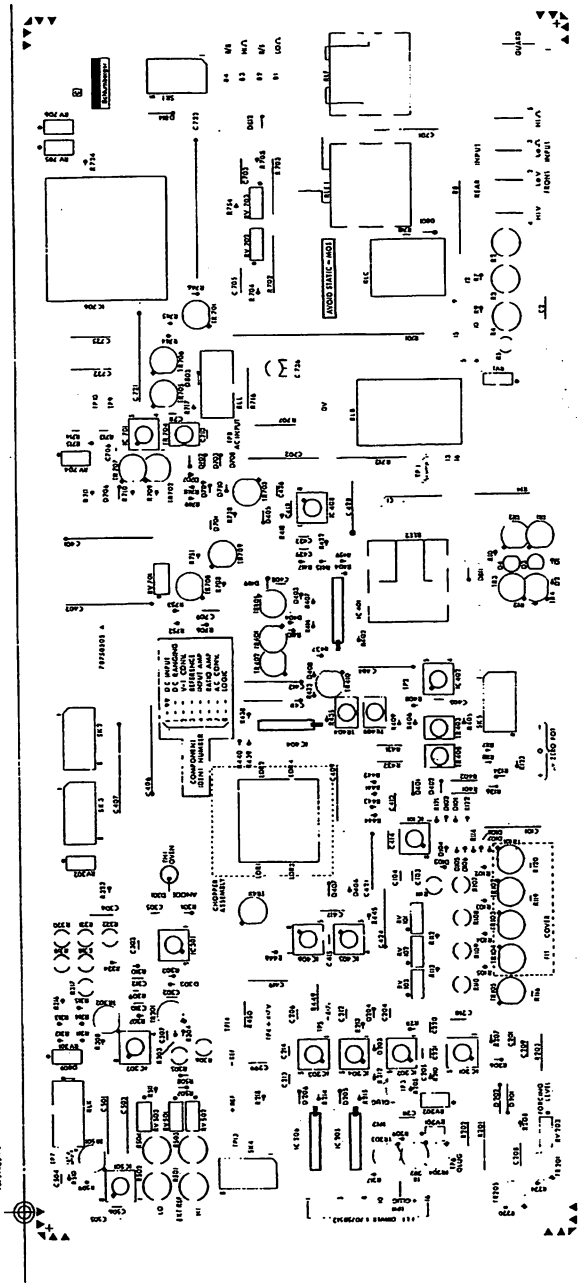
SUPPLY FUSE: 800mA value for both 115V and 230V supply voltage.


(FLOATING CIRCUITS)
(EARTHY CIRCUITS)
CLOCK
SIGNAL CONDITIONING
A-D CONVERSION
DIGITAL SECTION
Hi V
Hi Ω
Lo Ω
Lo V
G
DC INPUT & SCALING
AC-DC CONVERTER
OHMS CURRENT GENERATOR
MAIN AMPLIFIER
220Hz CLOCK
REFERENCE
REFERENCE SWITCHING
v-TO-t CONVERTER
CLOCK SYNCHRONISATION
PHASE LOCKED CLOCK
COUNTER CIRCUITS
AUTORANGE
TIMING CONTROL
MULTIPLEXER RAM
DISPLAY DRIVERS
DISPLAY CIRCUITS
CONTROL LOGIC
TO INTERFACE UNIT
CONTROL
POWER RAILS TO FLOATING CIRCUITS
FLOATING POWER
EARTHY POWER
POWER RAILS (EARTHY)

Diag 5.0



Block Schematic Diag. 6.1



PCB 5 Notations

DC INPUT (Diag 6.2)

The purpose of these circuits is to provide initial conditioning of the input signal and to protect the Input Amplifier (Diag 6.3) against voltage overloads.

INPUT ATTENUATOR

The instrument can accept inputs up to 14V without attenuation, this circuit providing the necessary attenuation on the top two ranges. For inputs below 14V RLB is energised, relay drive being derived from pcb 6. The signal path is thus via R8 only. Above 14V RLB is de-energised providing 1:100 attenuation of the input signal, adjusted by RV1.
C2, R7 and R9 are spark suppression components.
The output from this stage can be monitored at Test Point 1.

INPUT PROTECTION

Despite the use of an Input Attenuator. large input swings could still occur, sufficient to overdrive the Input Amplifier. The Input Protection circuit provides an extra safeguard, limiting the signal line excursions to approximately 17V on the 10V and 1000V ranges.

On all other ranges the output from this circuit is limited to approximately 1.7V, Zeners D1, D2 being shunted by TR3, TR4.

LED's D3, D4 are used as normal diodes in this circuit. However they can provide a useful clue to an engineer if a persistent overload indication is being investigated.

AC AND Ω

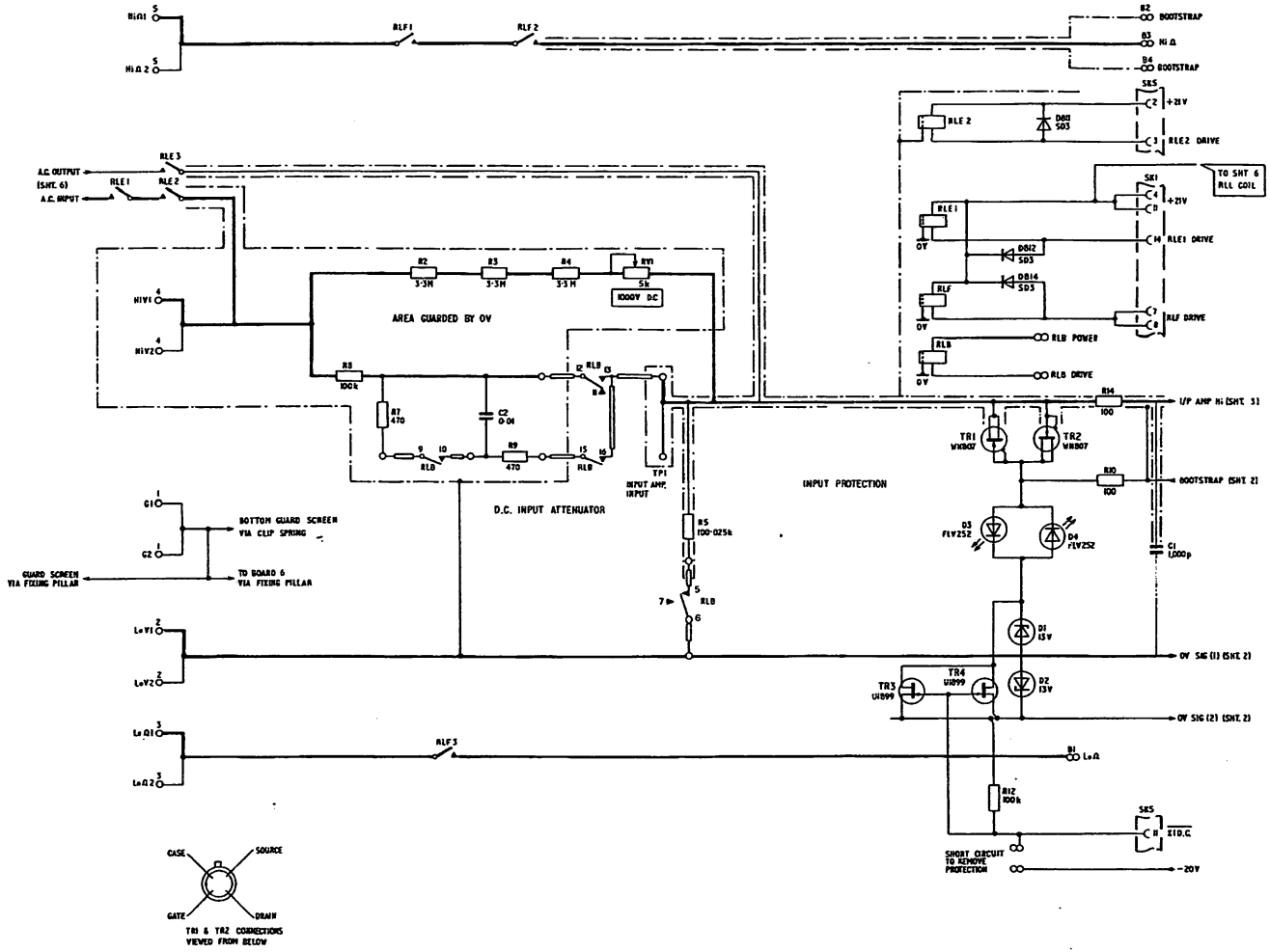
This circuit provides partial conditioning for the output from the AC/DC Converter, via RLE contacts, Input Protection being identical to that described above.

The Ohms Converter inputs are also to be found within this section of circuit, RLF providing the necessary switching.

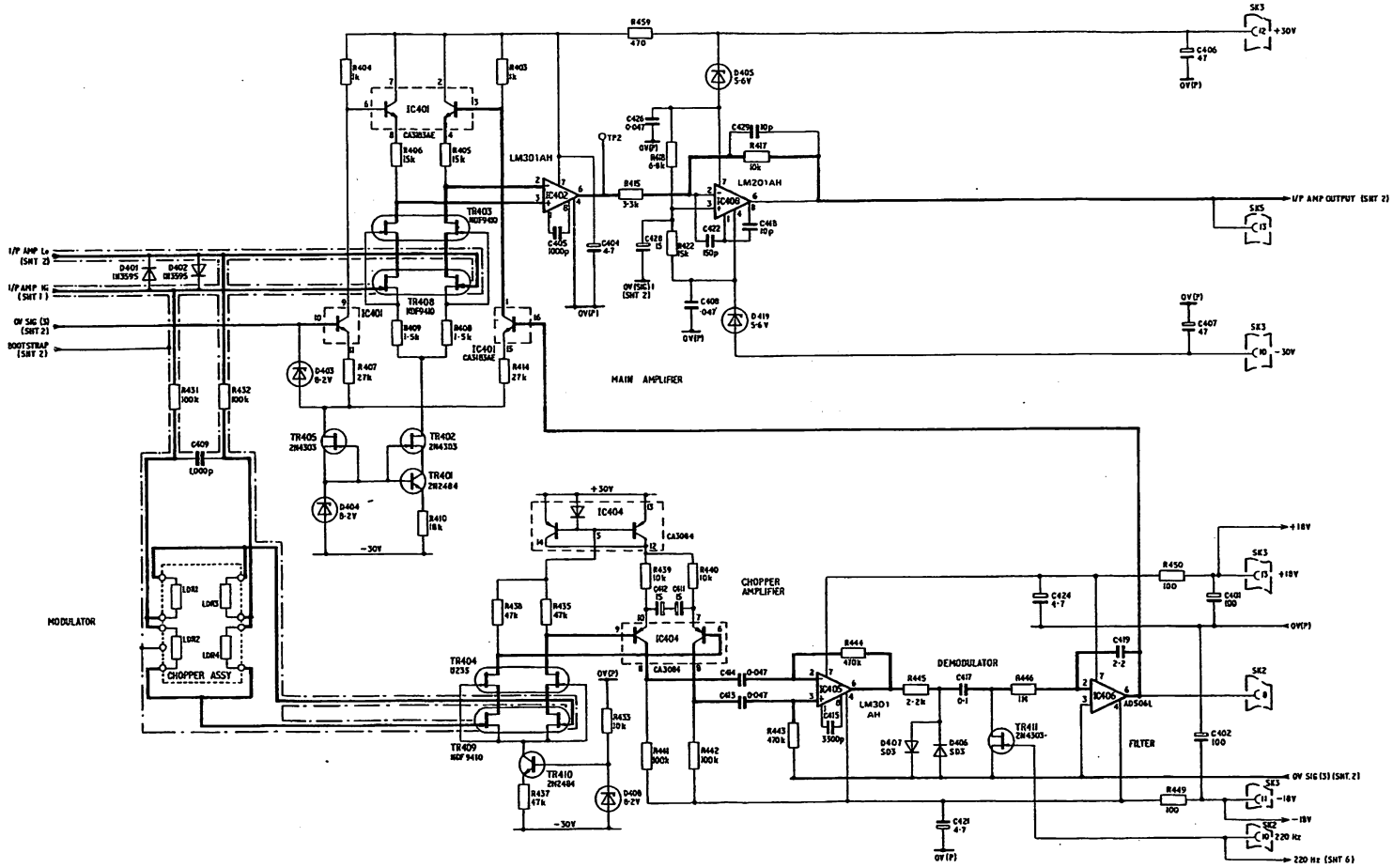
BOOTSTRAP

Note the guard afforded to much of this circuit by the Bootstrap line. The output of a voltage follower (BOOTSTRAP AMPLIFIER, Diag. 6.4) provides local voltage 'guard', supplementing the effect of the main instrument Guard. Bootstrap potential is always that of the input to the main Input Amplifier.

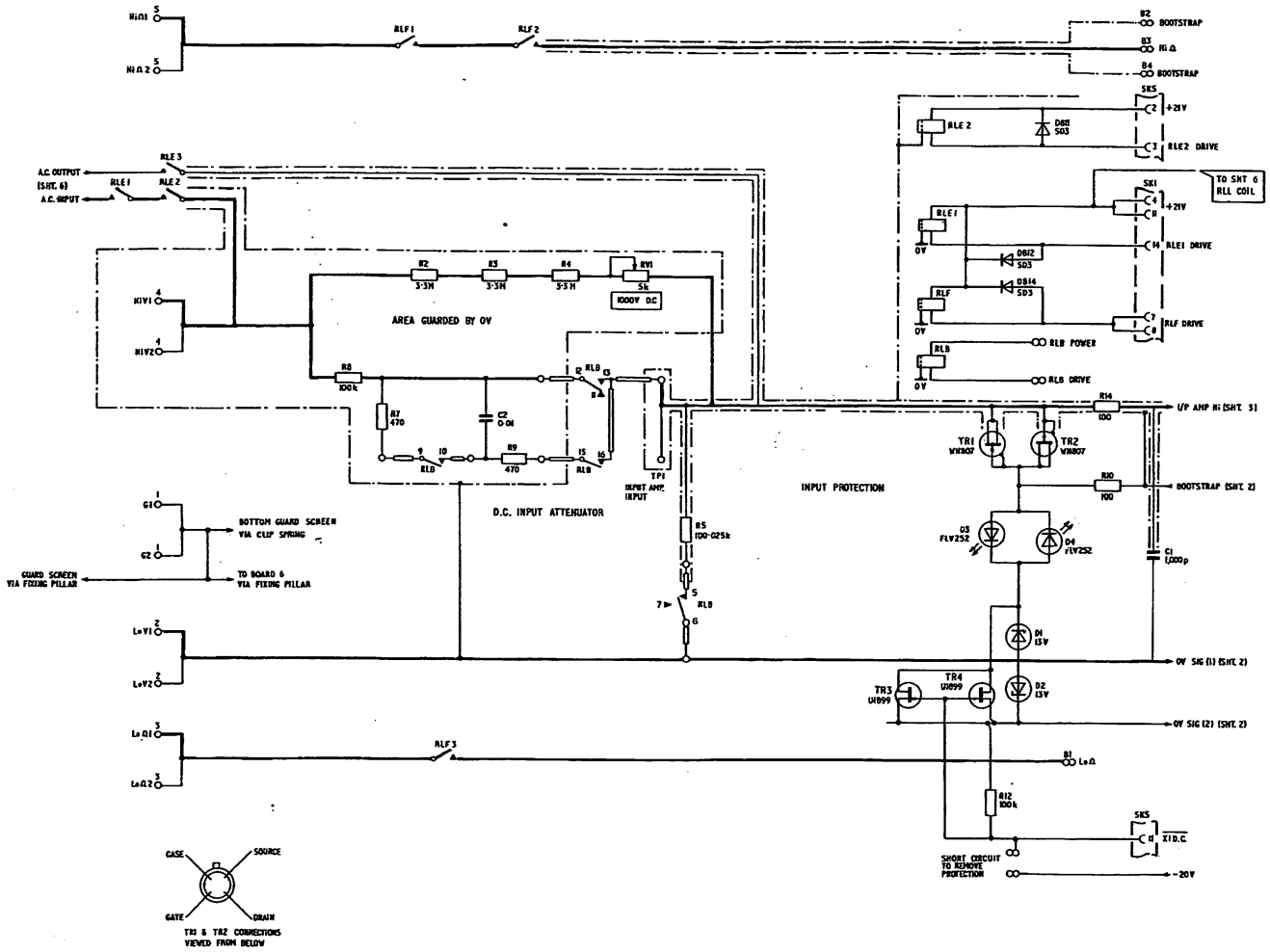
← PCB 5 Notations



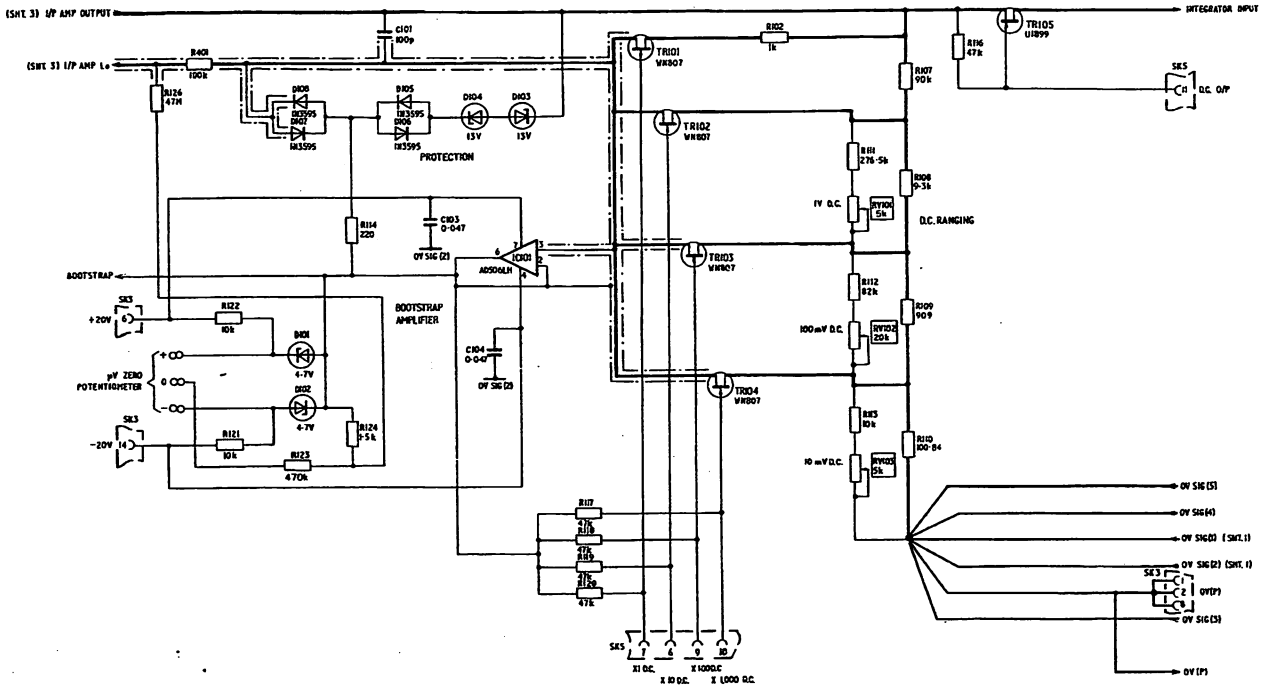
DC Input Diag. 6.2 pcb 5 (sheet 1)



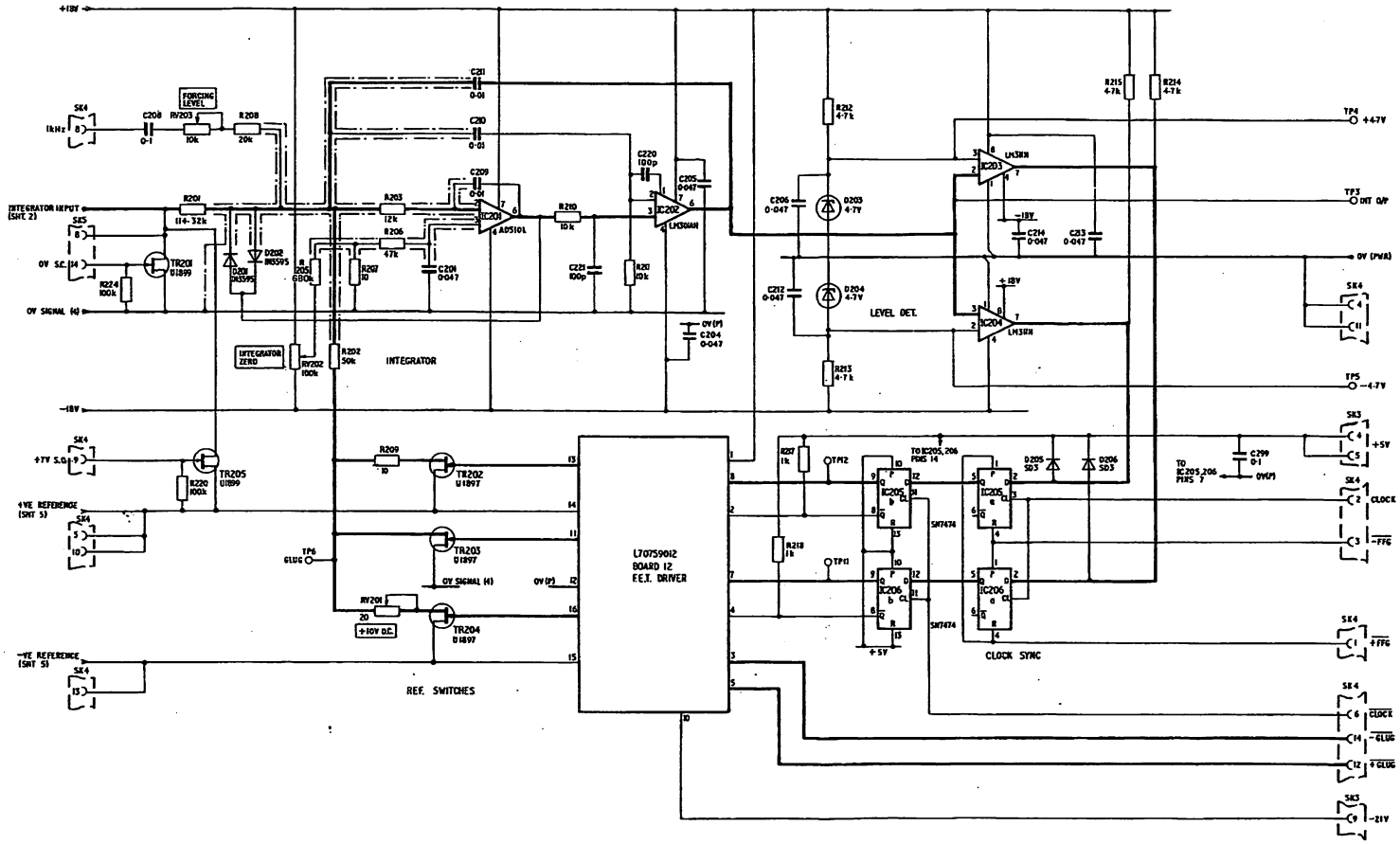
Input Amplifier Diag. 6.3 pcb 5 (sheet 3)



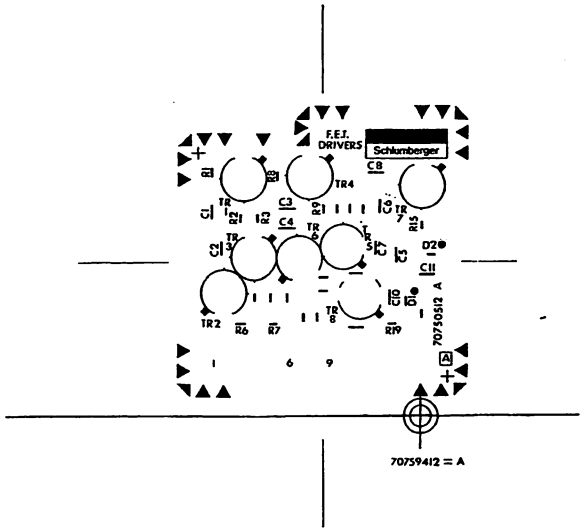
DC Input Diag. 6.2 pcb 5 (sheet 1)



DC Ranging Diag. 6.4 pcb 5 (sheet 2)



V to t Convertor Diag. 6.5 pcb 5 (sheet 4)



PCB 12 Notations

FET DRIVERS (Diag 6.6)

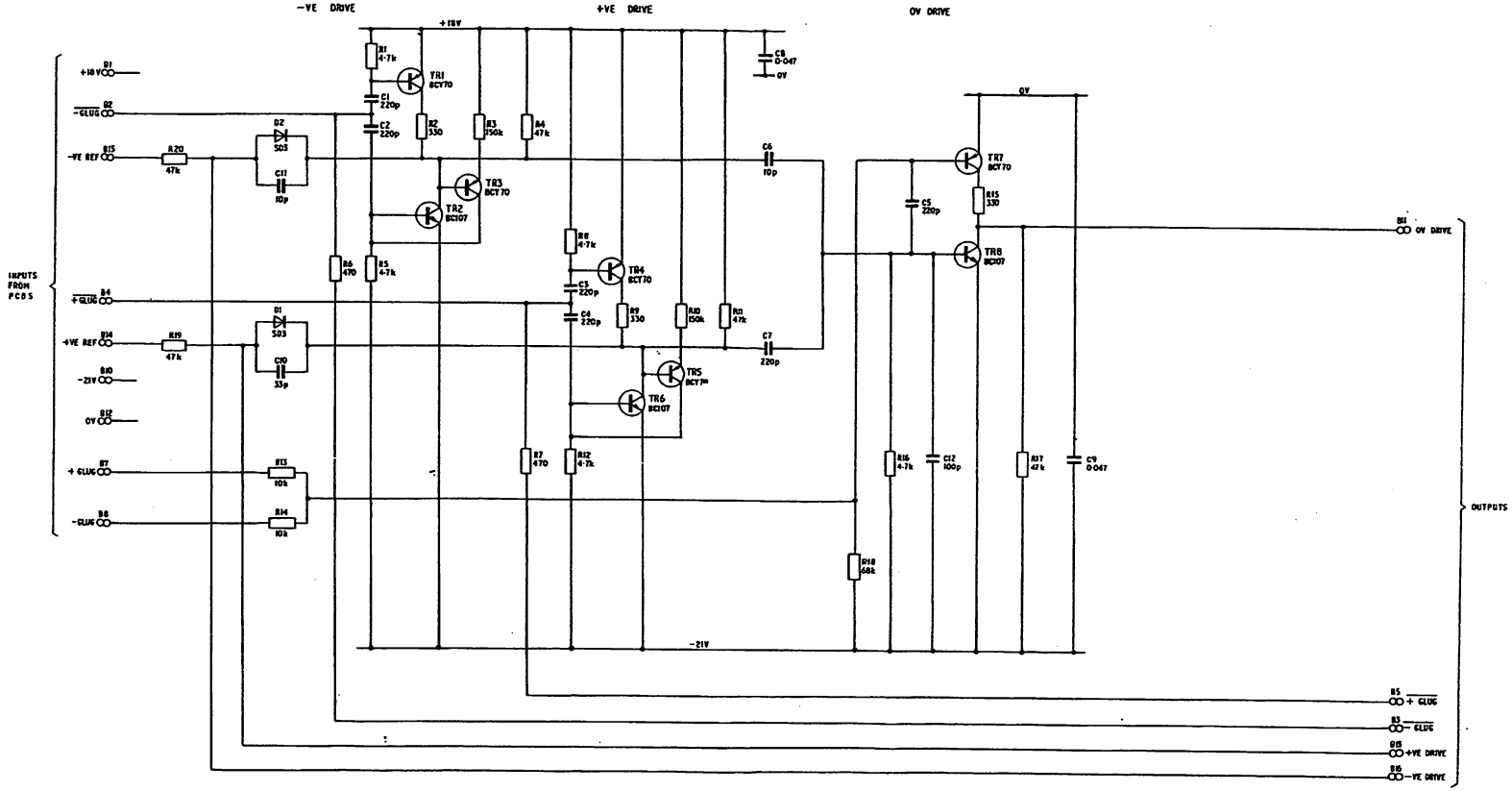
The circuit illustrated, though forming part of the reference switching arrangement on Diag 6.5, is carried on a separate plug-in card, pcb 12. Interconnection with board 5 is via Berg-type horizontal sockets, the mating pins being mounted vertically on board 5.

The FET Drivers provide fast switching of the reference potentials and 0V, the circuit configuration ensuring rapid transition from one switch state to the other. TR3, TR5 perform a 'latching' function for the ON state of their associate switches. In the case of the 0V switch both ON and OFF states are latched by the inputs on pins B7, B8. Pins B6, B9 are not used.

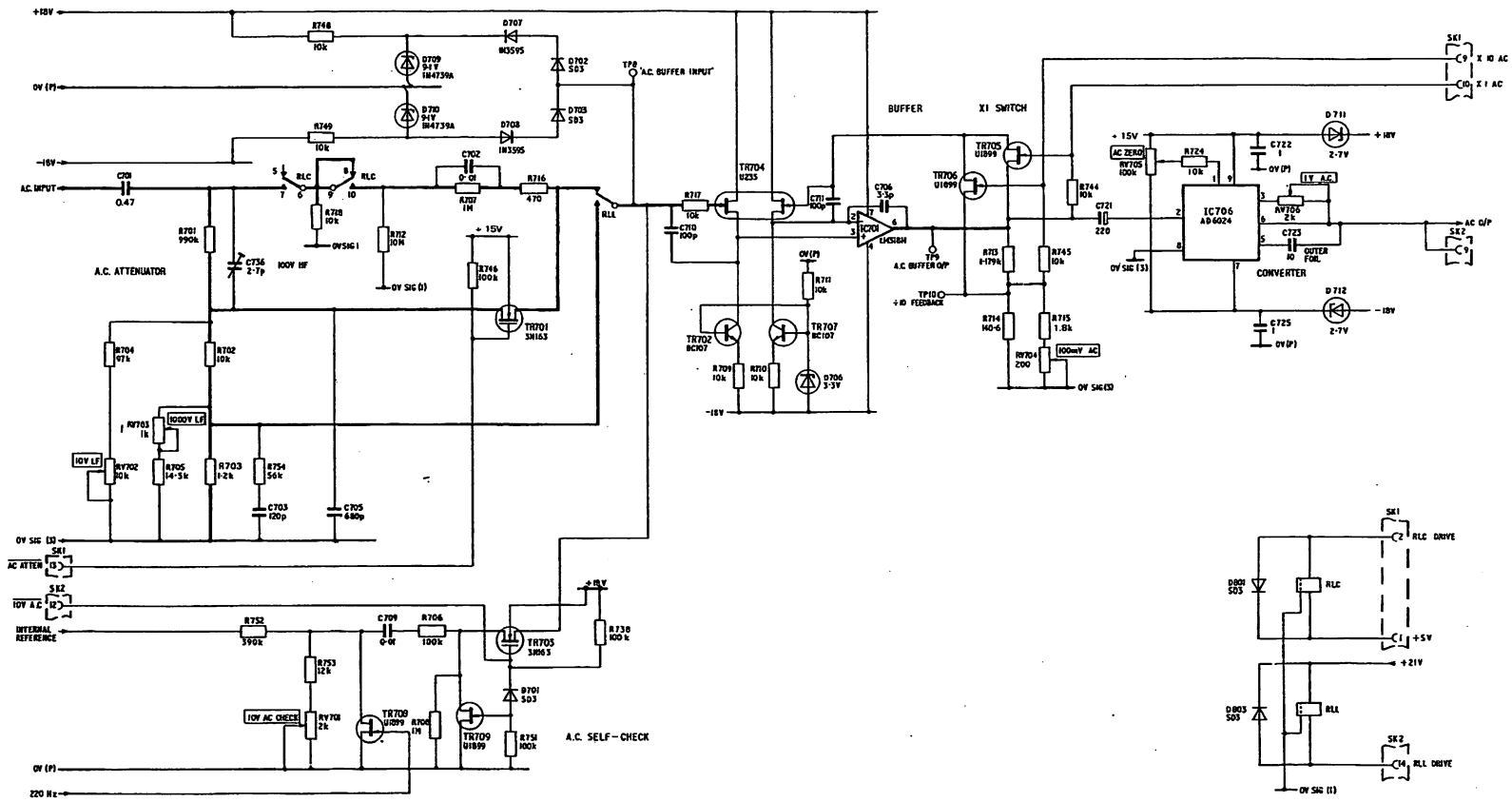
GLUG

Within this manual the reader will find many signal annotations which include the word "Glug". The word may be abbreviated to the letter 'G', as in FG (*forced* glug), FFG (*forced forced* glug) etc. The term is used as a convenient alternative to the cumbersome title "Quantum of Charge" (i.e. V x t) and should be treated merely as an identifier label, facilitating circuit tracing.

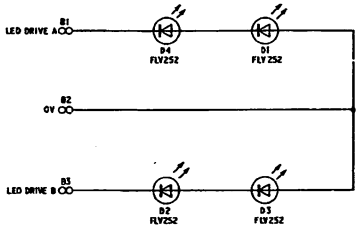
← PCB 12 Notations



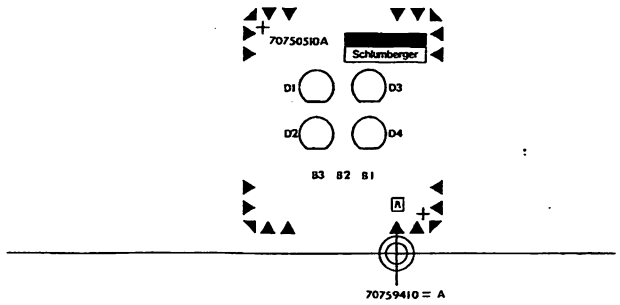
Fet Drivers Diag. 6.6 pcb 12



AC Conversion Diag. 6.7 pcb 5 (sheet 6)



PCB 10 Circuit Diagram



PCB 10 Notations

RESISTANCE (Diag 6.8)

Resistance measurement with the 7075 is accomplished by measuring the voltage developed across the unknown resistor by virtue of a known current passing through it. The major function of the section of Board 6 illustrated is that of generating the necessary current. The circuit is "area" coded 6.

CURRENT GENERATORS

The instrument's negative reference is utilised to determine a current which, in it's turn, produces a reference potential relative to the +30V rail — divided down across R602, R604 (a matched set). This potential defines the Hi Current, the value of which depends on the position of reed switches as follows:

RLH 1 closed	1mA	(10Ω to 10kΩ)
RLG 1 closed	10μA	(100kΩ to 1MΩ)
Both reeds open	1μA	(10MΩ)

The Lo Current generator provides the necessary current sink to give effective 4 - terminal measurement, potentials arising from lead resistances being nullified. The second contacts of reeds RLG, RLH perform a similar function to those outlined for RLG1, H1 above.

Link A across R603 is set as required during factory calibration. IC's 601 to 603, unity gain amplifiers are used in this configuration as voltage followers. High voltage (up to 300V) protection is given by D606, R610 and TR's 605 and 606.

Note that the Hi Current circuits are guarded relative to the potential developed across R604, Bootstrap providing the remaining guard potential.

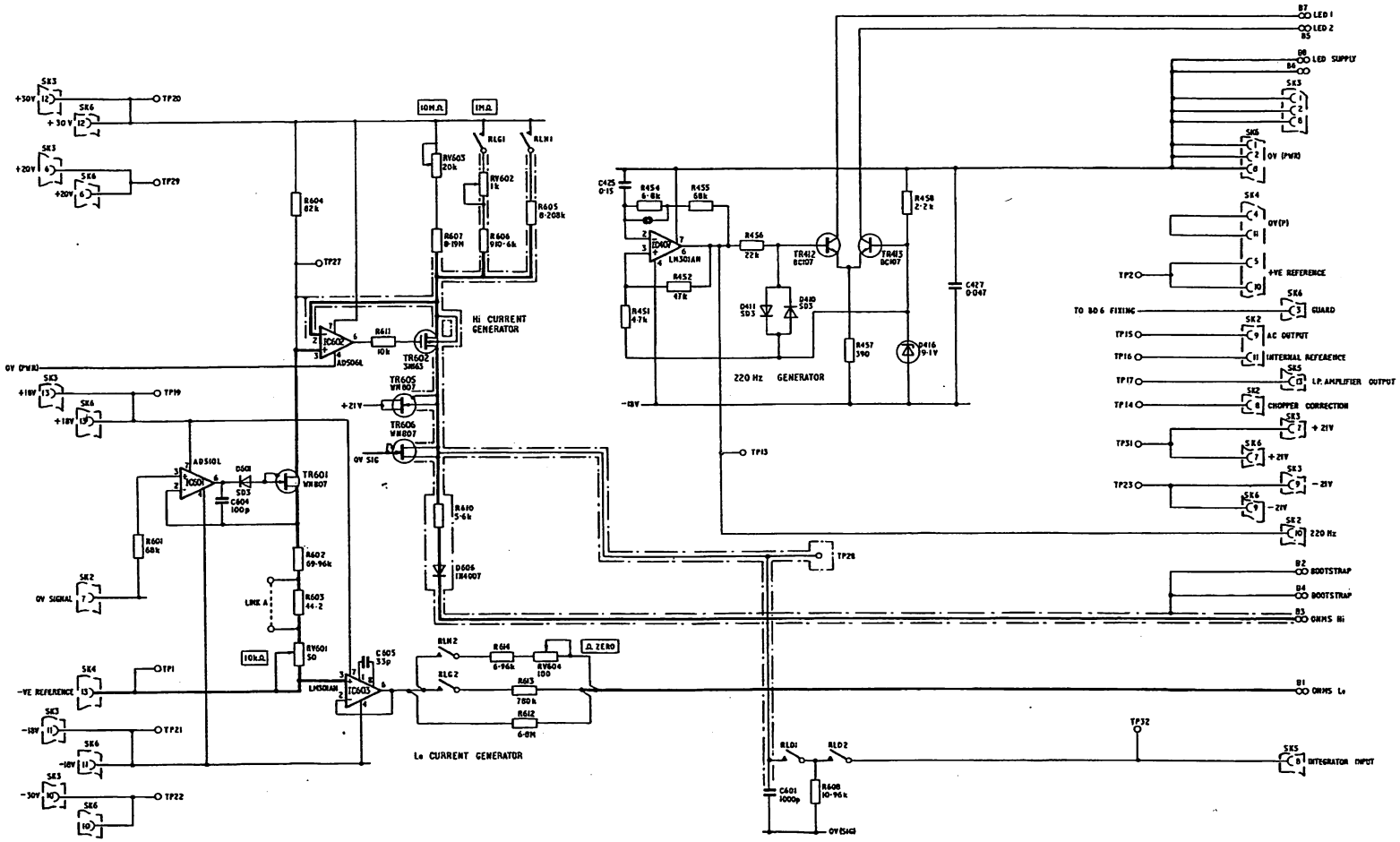
SELF CHECK

The 1mA current through R608 in parallel with the input resistance of the Integrator p[illegible] 10V for the nominal Self Check 10kΩ display. Control is via RLD.

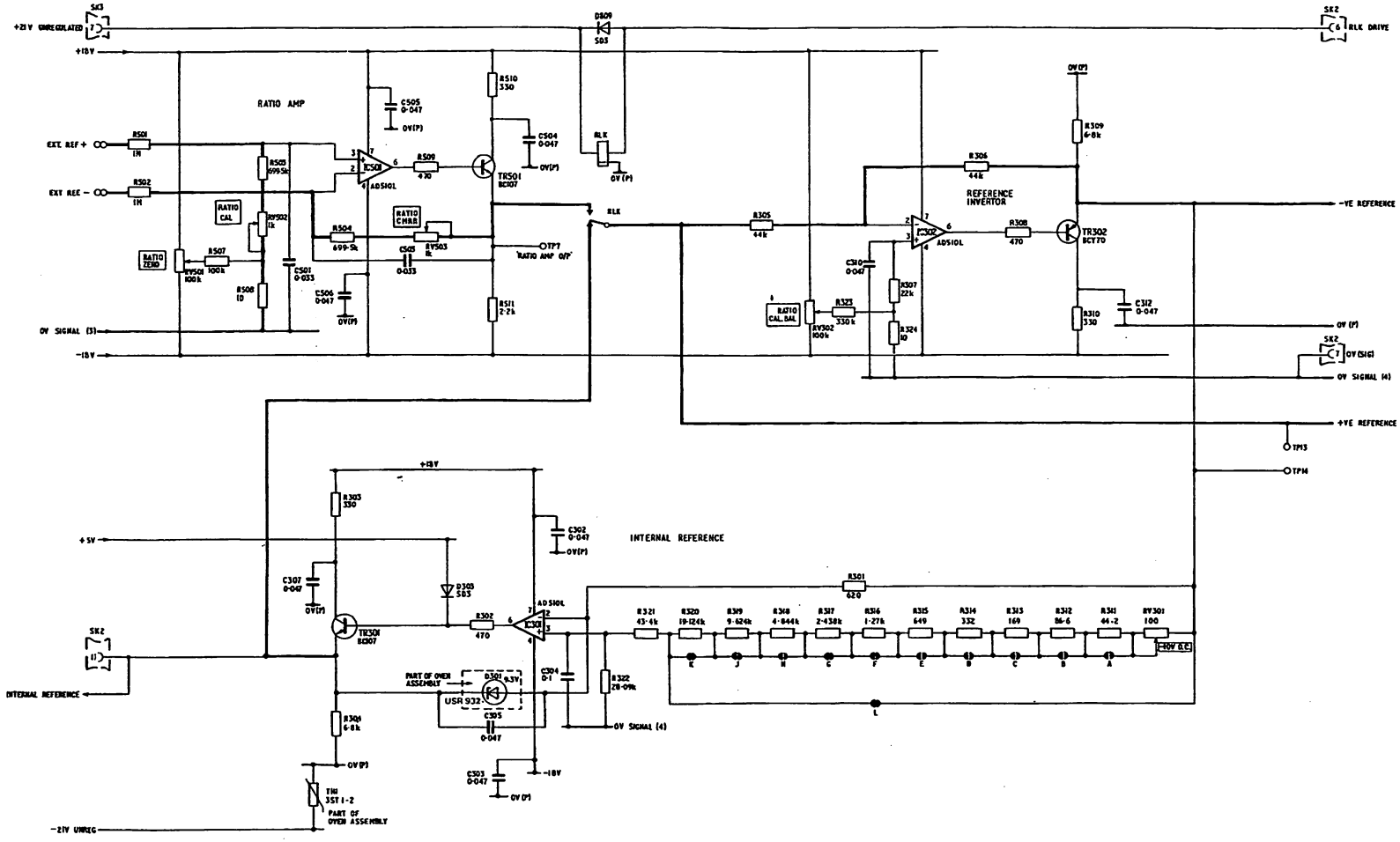
CHOPPER DRIVE

Also illustrated in Diag 6.8 is the 220Hz Generator (area code 4) which produces the chopping waveform used in the Input Amplifier circuit (Diag 6.3). Outputs are taken via Berg pins 5 and 7 to the LED's forming part of the opto-electronic Chopper Modulator (Diag 6.3). A further output feeds the Demodulator in the same circuit area of pcb 5. A link is provided across R454 to permit a small adjustment of the nominal 220Hz, if the oscillator frequency is found to be a harmonic of the supply frequency.

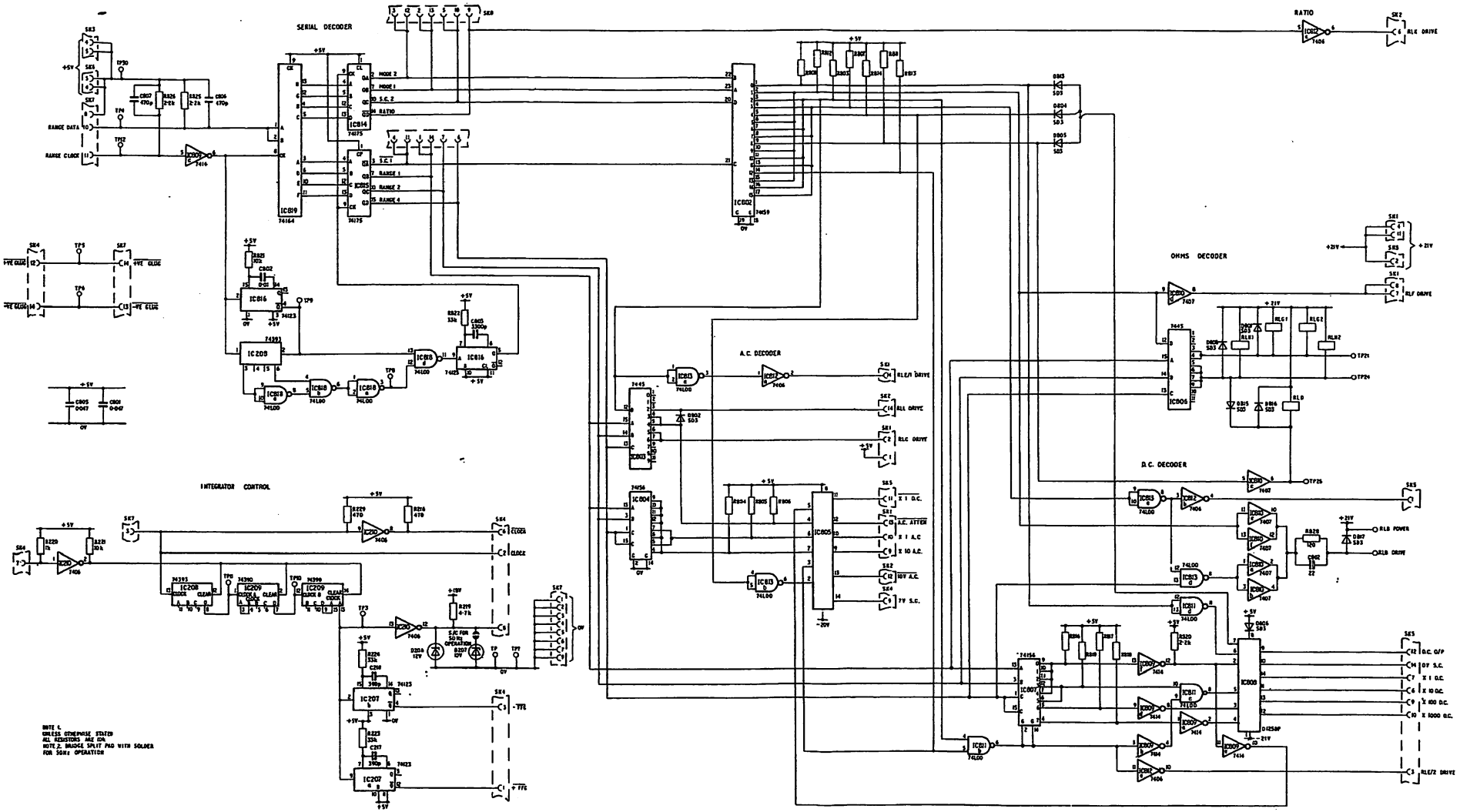
← PCB 10 Notations and Circuit Diagram



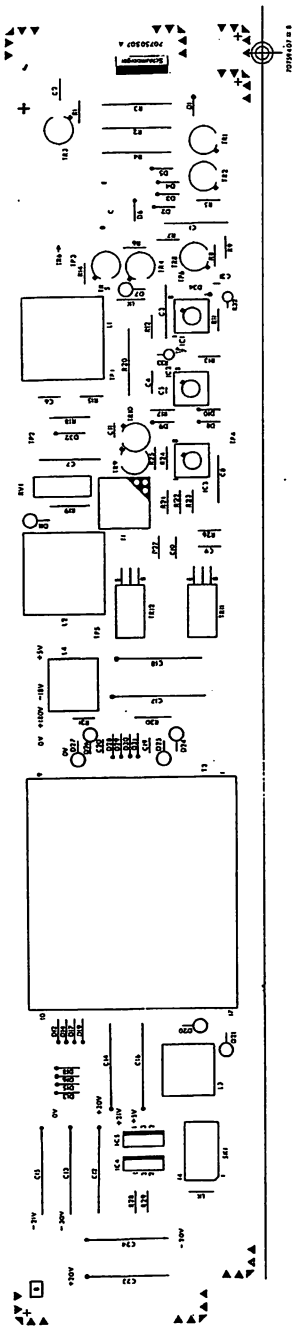
Resistance Diag. 6.8 pcb 6 (sheet 1)



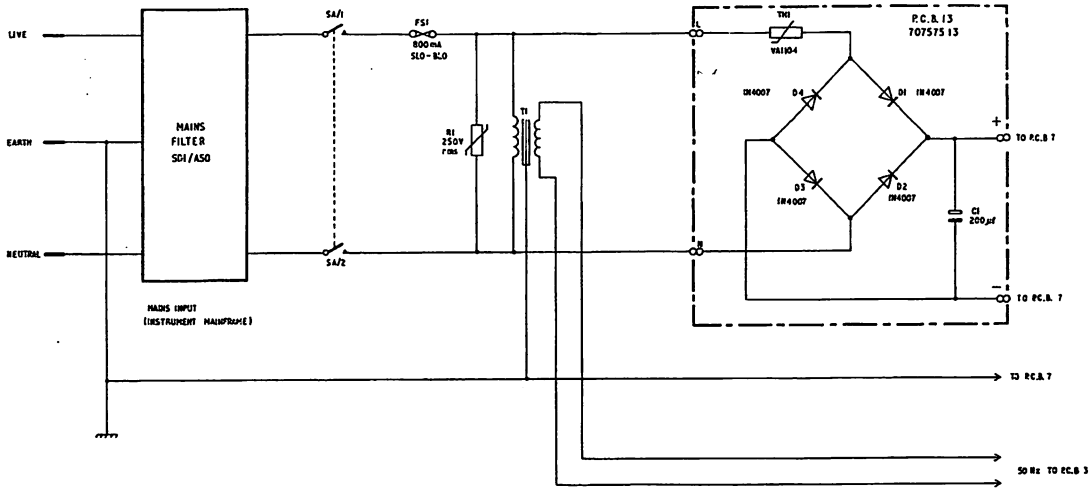
Reference Diag. 6.9 pcb 5 (sheet 5)



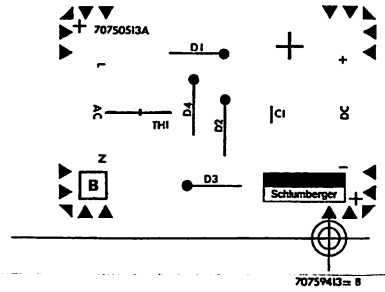
Floating Logic Diag 6.10 pcb 6 (sheet 2)



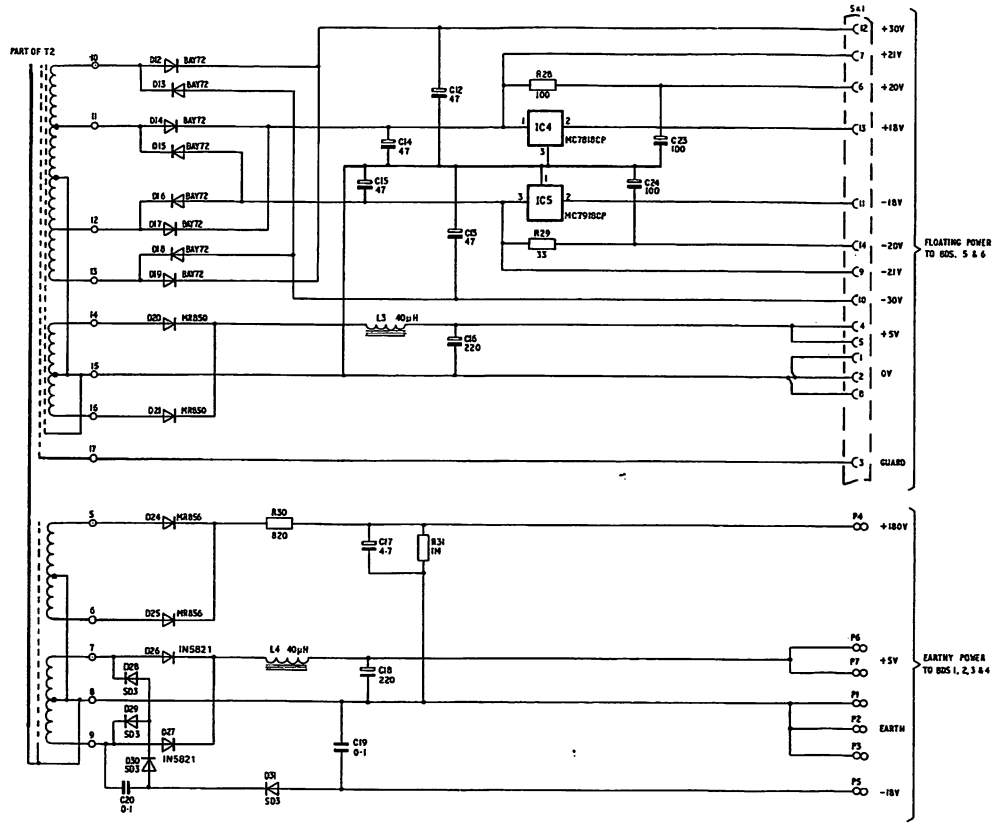
PCB 7 Notations



Mainframe Diag. 6.11



PCB 13 Notations



Rectification Diag. 6.13 pcb 7 (sheet 2)

RECTIFICATION (Diag. 6.13)

T2 secondary windings provide the rectifier current required to power the various dc rails used within the voltmeter.

IC4, IC5 are used to regulate the floating positive/negative 18V rails.

D27 to D30 act in a voltage trebler circuit from the earthy +5V winding to give a nominal −18V on P5. This rail supplies the keep-alive electrode of the display tubes.

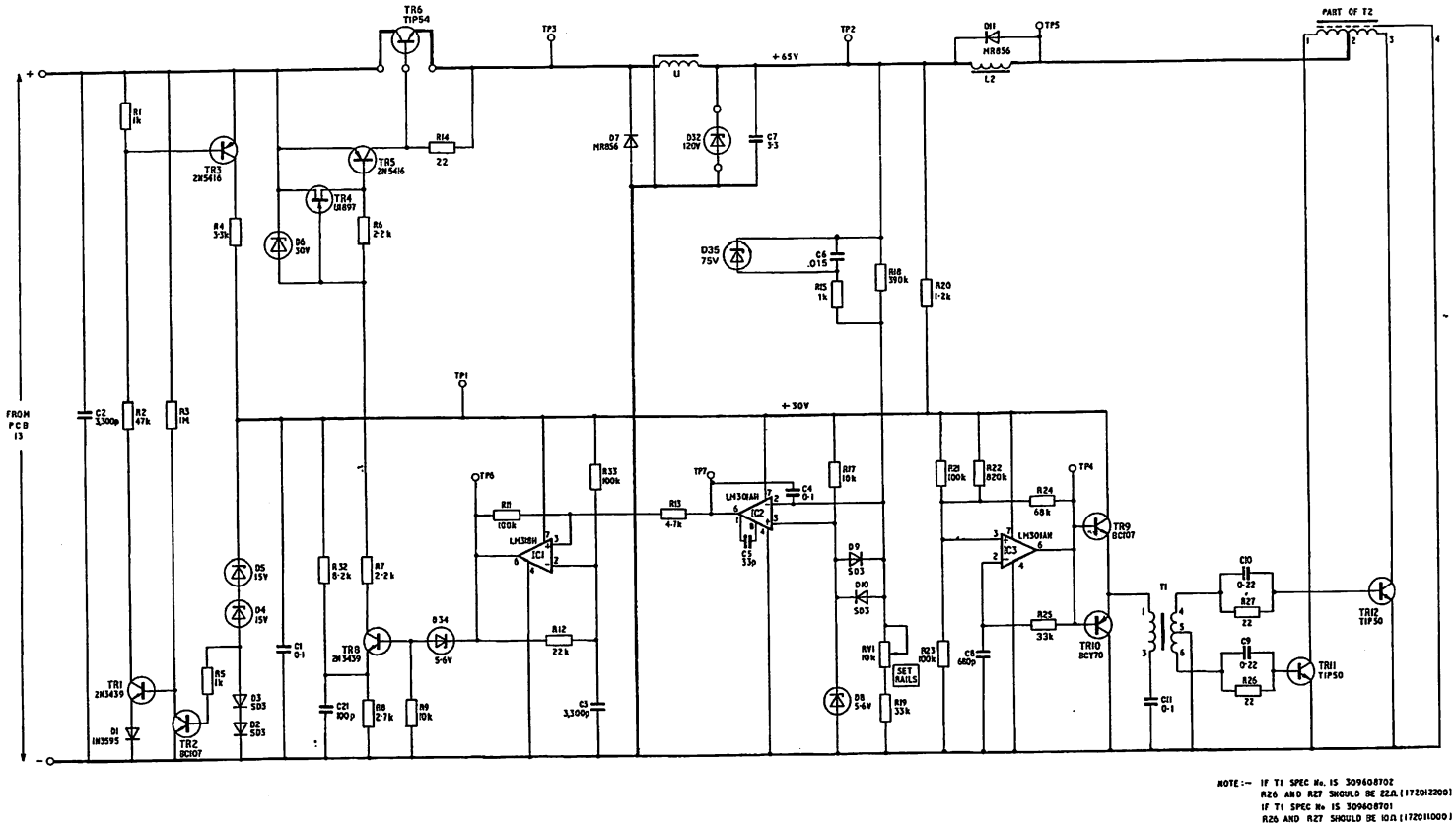
The anodes of the display elements are fed with +180V, output on P4.

Note that terminal 17 of transformer T2 is at Guard potential and should NOT be connected to 0V, nor to Supply Earth.

WARNING – FLOATING SUPPLIES

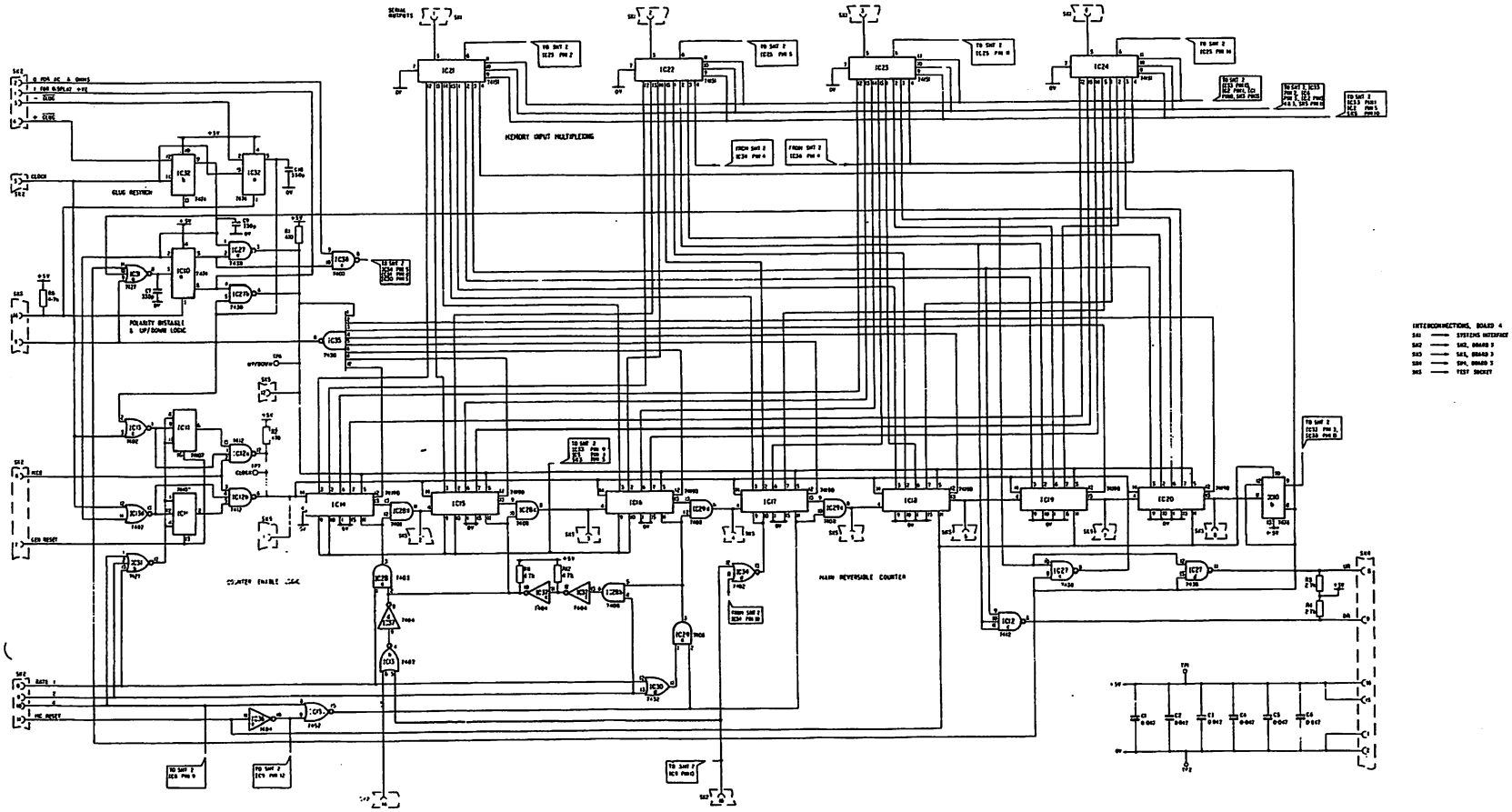
For safety always use an isolating transformer.

← Diag. 6.13

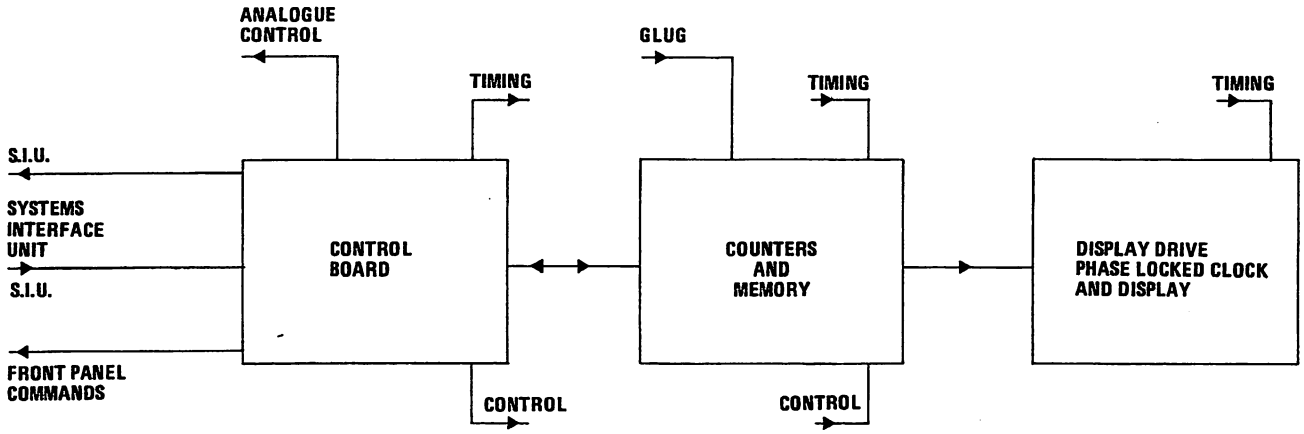


NOTE:— IF T1 SPEC No. IS 30960870Z
R26 AND R27 SHOULD BE 22Ω. (17Z012200)
IF T1 SPEC No IS 30960870T
R26 AND R27 SHOULD BE 10Ω. (17Z011000)

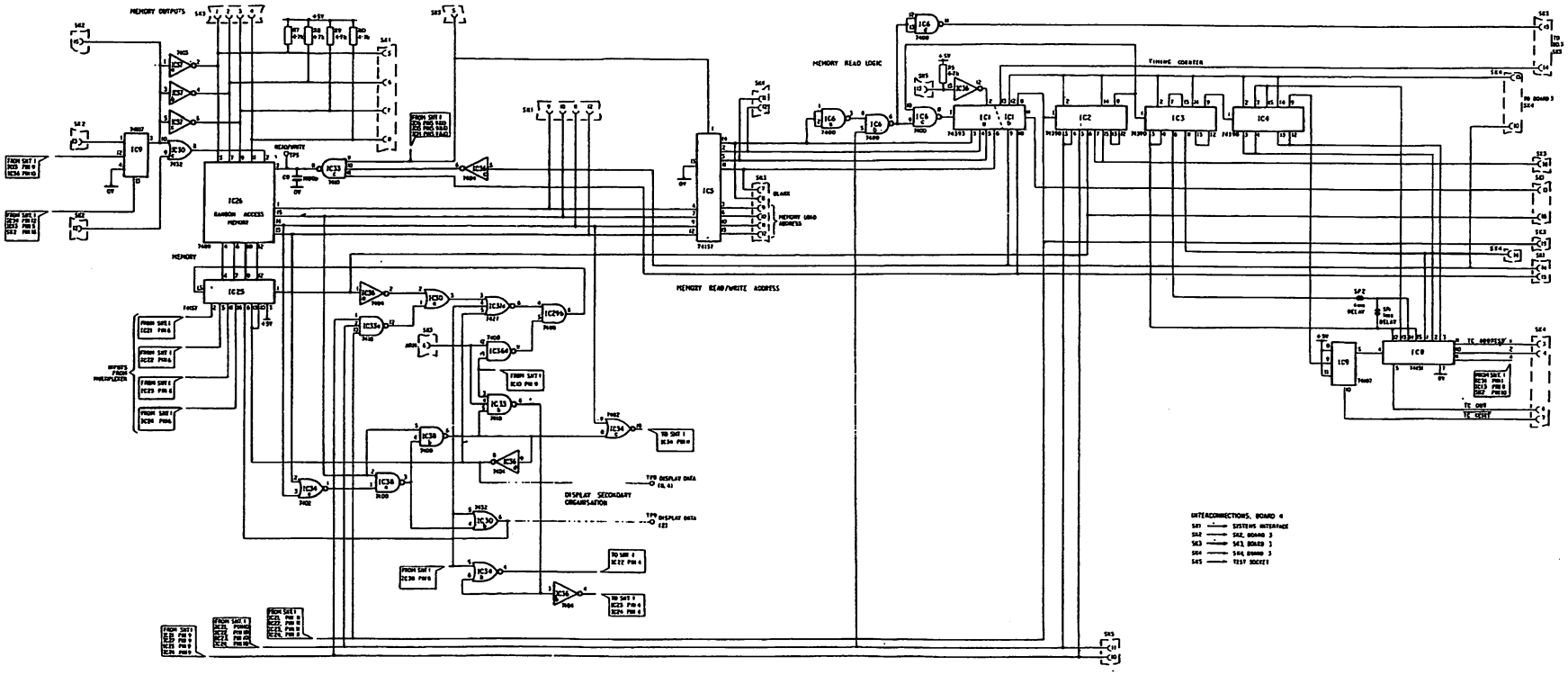
Power Supply Diag. 6.12 pcb 7 (sheet 1)



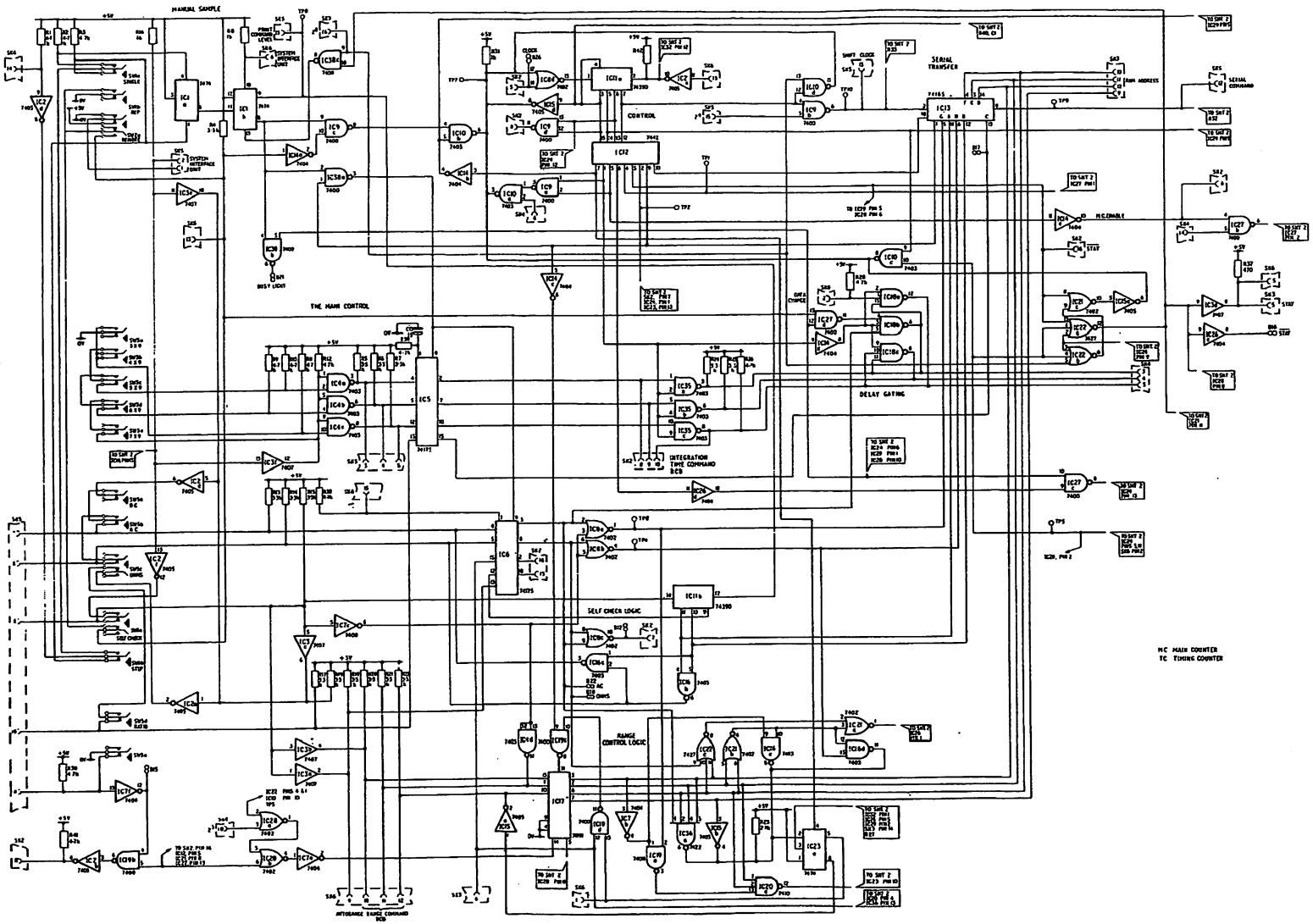
Counters and Memory Diag. 6.15 pcb 4 (sheet 2)



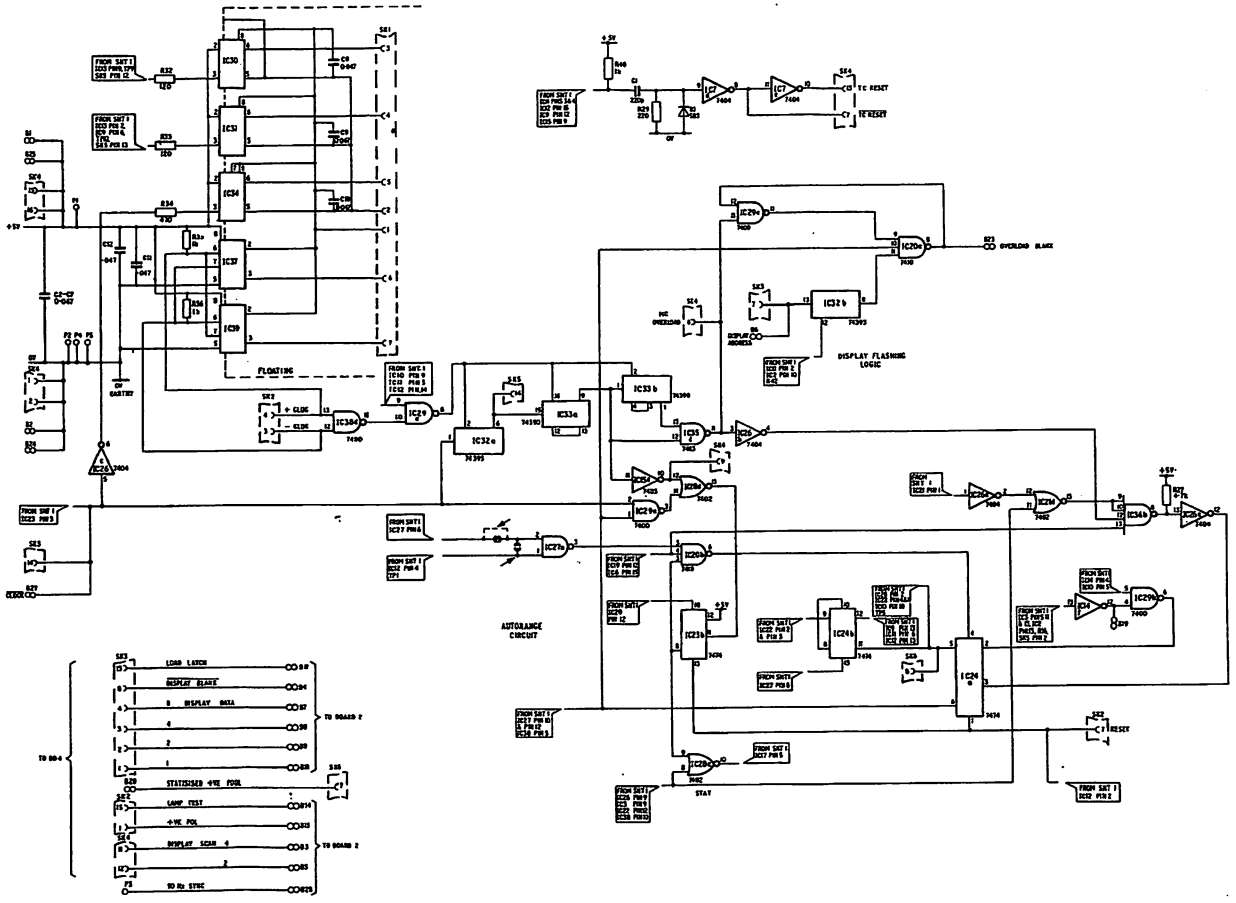
Block Schematic Diag. 6.14



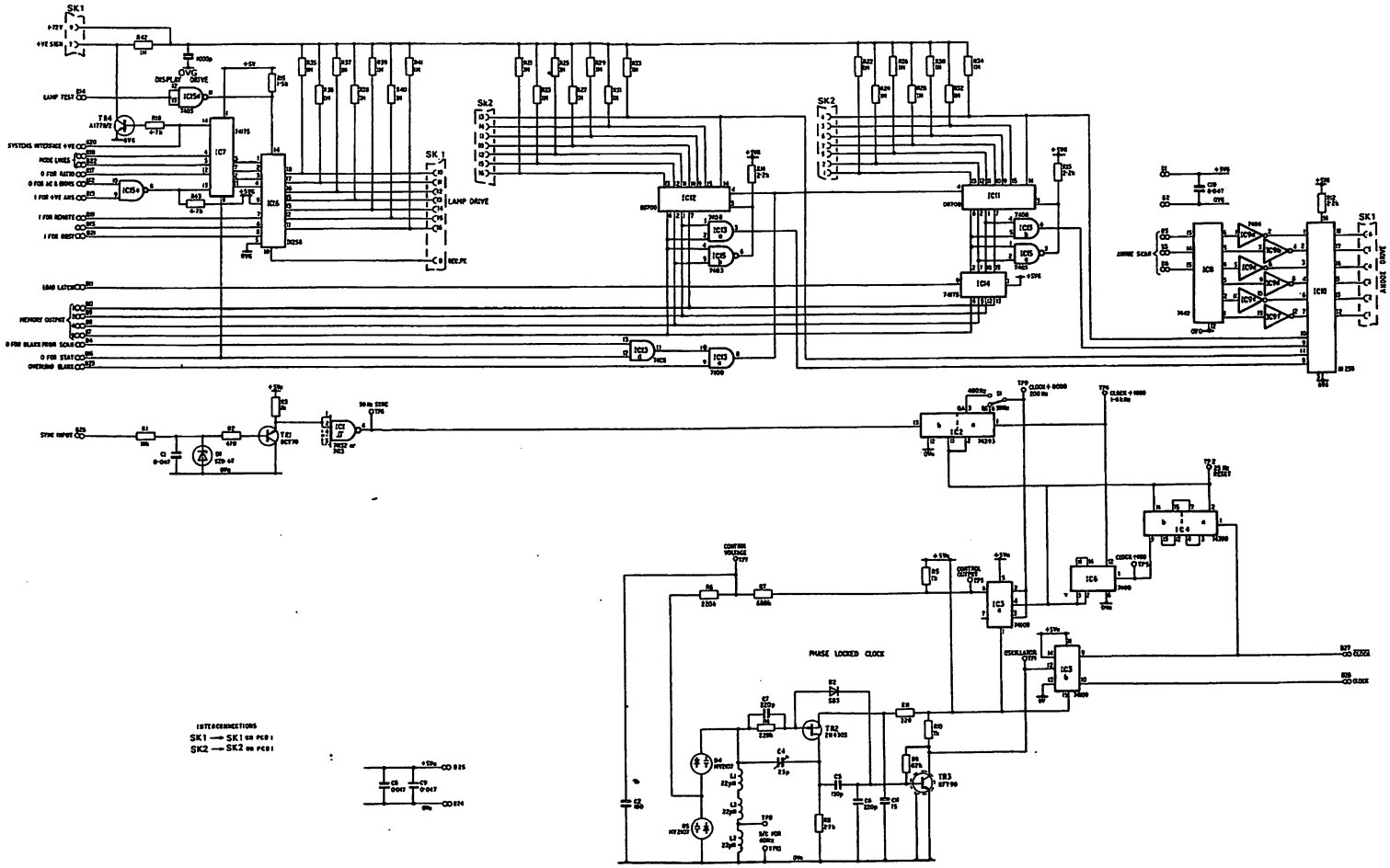
Counters and Memory Diag. 6.16 pcb 4 (sheet 1)



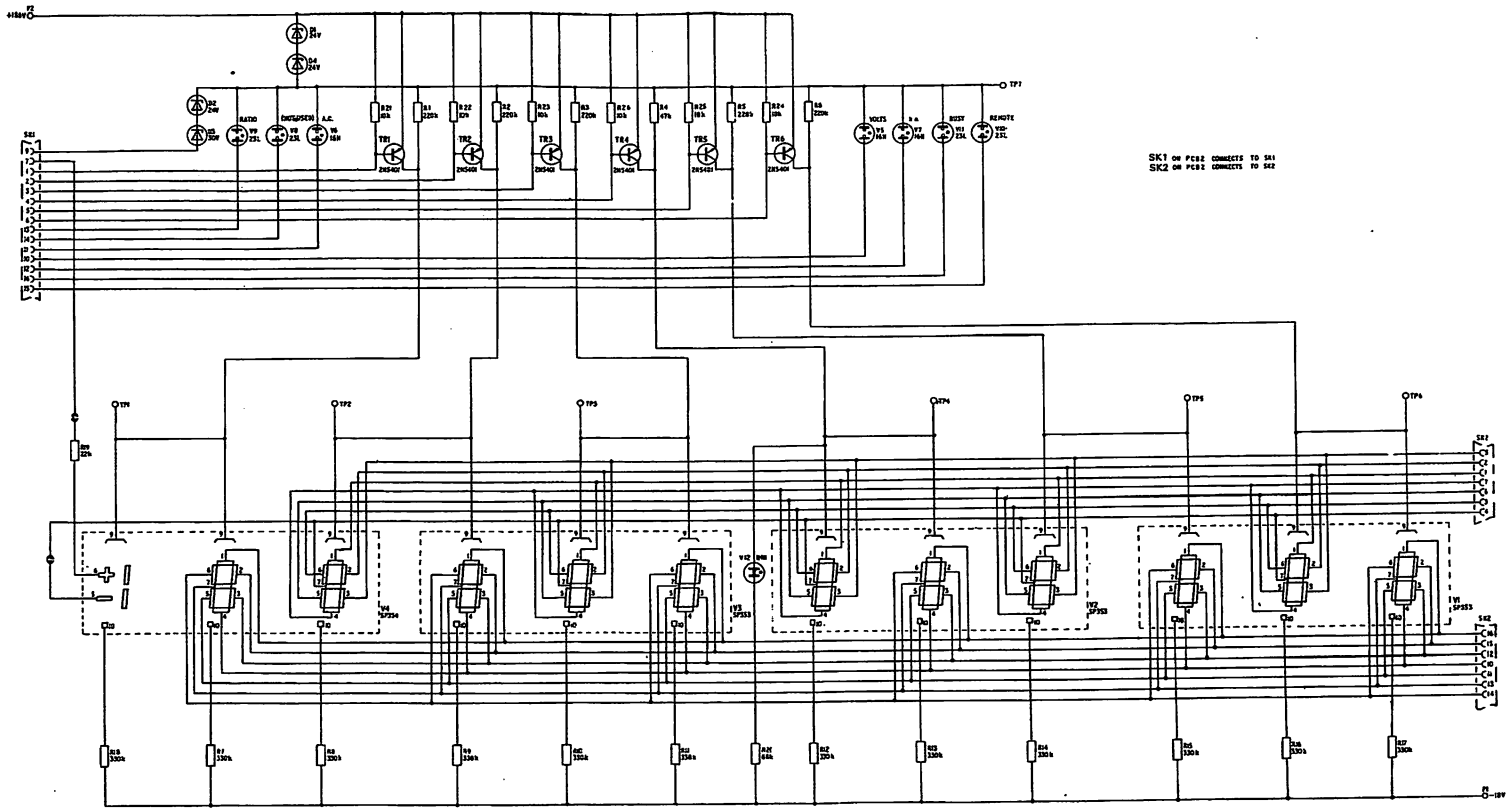
Control Board Diag. 6.17 pcb 3 (sheet 1)



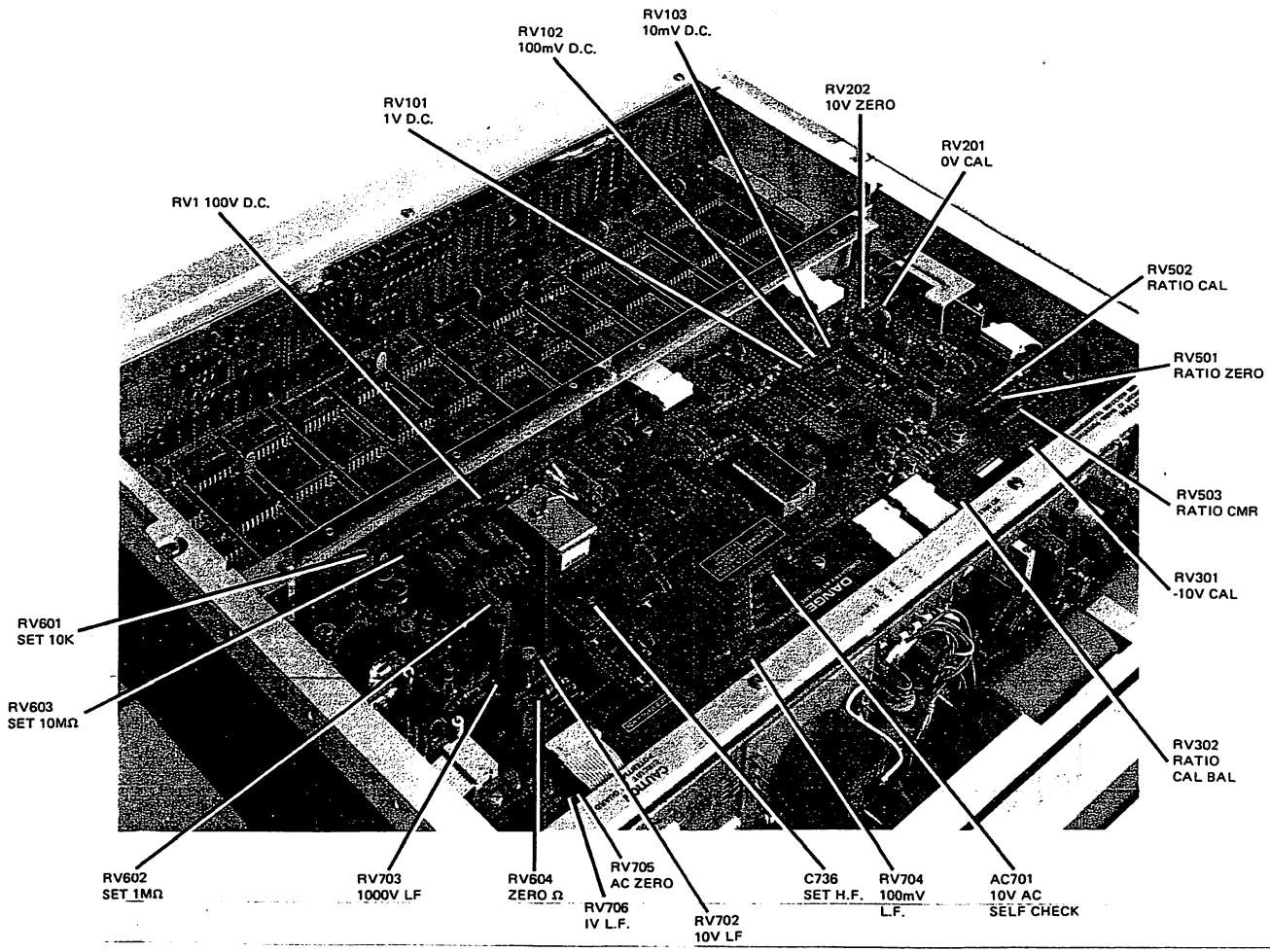
Control Board Diag. 6.18 pcb 3 (sheet 2)



Display Drive and Phase Locked Clock Diag. 6.19 pcb 2



Display Diag. 6.20 pcb 1


RV103
10mV D.C.
RV102
100mV D.C.
RV202
10V ZERO
RV101
1V D.C.
RV201
0V CAL
RV1 100V D.C.
RV502
RATIO CAL
RV501
RATIO ZERO
RV503
RATIO CMR
RV301
-10V CAL
RV601
SET 10K
RV603
SET 10MΩ
RV302
RATIO
CAL BAL
RV602
SET 1MΩ
RV703
1000V LF
RV604
ZERO Ω
RV705
AC ZERO
RV706
IV L.F.
RV702
10V LF
C736
SET H.F.
RV704
100mV
L.F.
AC701
10V AC
SELF CHECK

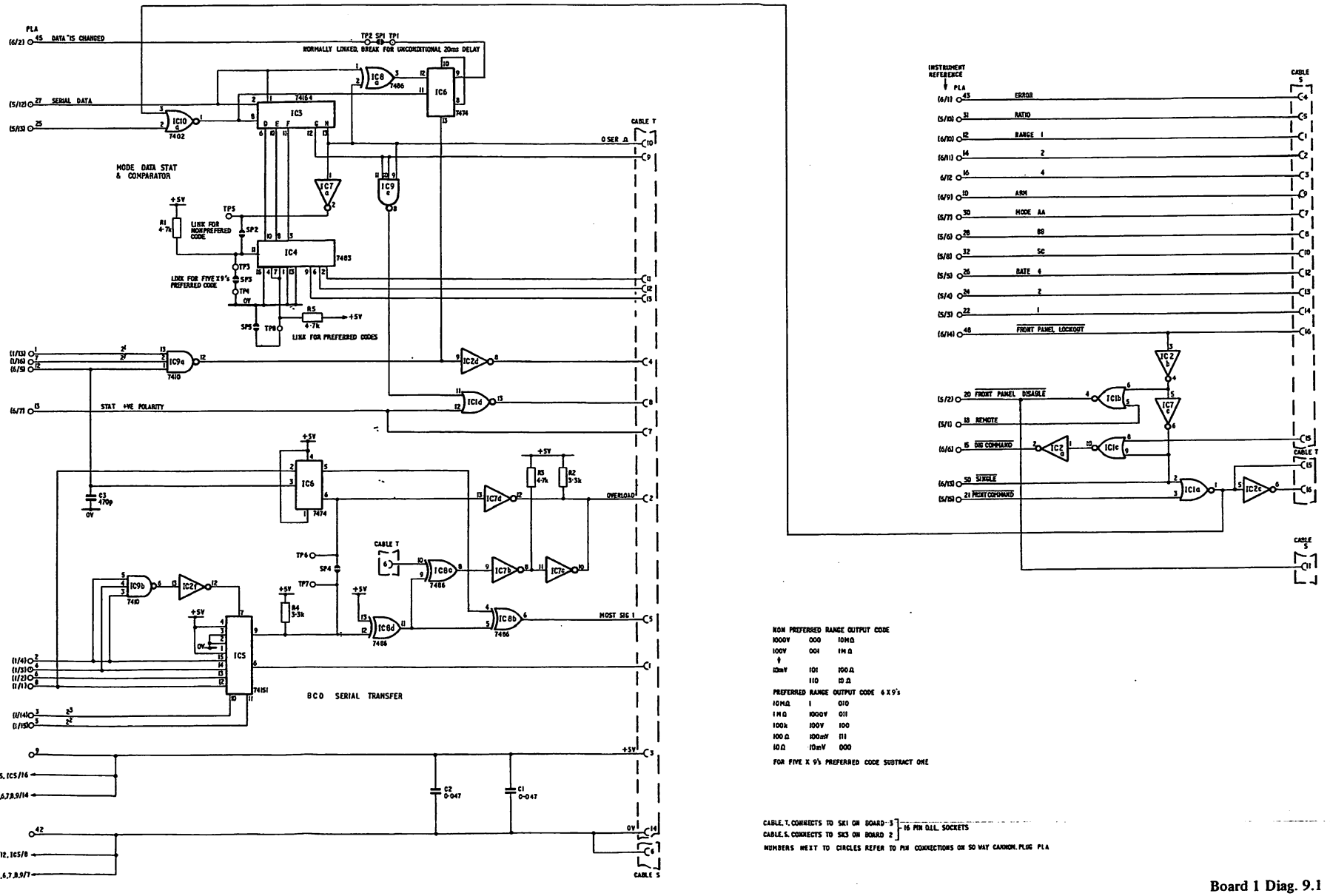
NOTES

1. To avoid the slowing down effect of range hunting when Autorange is remotely commanded, receipt of a SAMPLE Command is necessary for autorange to occur. When in LOCAL operation however, detection of an overload causes an immediate Autorange upwards, independent of the receipt of SAMPLE Command.
2. Should a SAMPLE Command occur during a self-protecting autorange sequence it will be stored, to be obeyed once the overload condition no longer exists. With the foregoing exception SAMPLE Command occuring at any time other than after a PRINT Command output, will be ignored.

CONNECTION TABLE

SKB Pin No.	FUNCTION		SKB Pin No.	FUNCTION
1	1×10^6		26	+ ve POLARITY
2	8×10^5		27	– ve Output code
3	4×10^5		28	FUNCTION output code 0 for A.C. } Both 0 for CHECK
4	2×10^5		29	0 for Ω } Both 0 for CHECK
5	1×10^5		30	(4)
6	8×10^4		31	(2) RANGE Output
7	4×10^4		32	(1)
8	2×10^4		33	PULSE PRINT Command
9	1×10^4		34	LEVEL (Output signal)
10	8×10^3		35	DATA CAN CHANGE Output
11	4×10^3	Staticised	36	OVERLOAD (Output signal)
12	2×10^3	BCD output	37	EARTH/Logic '0' level
13	1×10^3	data	38	FRONT PANEL LOCKOUT
14	8×10^2		39	SAMPLE Command - CONTACT
15	4×10^2		40	SAMPLE Command - Pulse
16	2×10^2		41	RATIO Command
17	1×10^2		42	FUNCTION Command 0 for AC } Both 0 for CHECK
18	8×10^1		43	(DC, AC (RMS or Ω) 0 for Ω } Both 0 for CHECK
19	4×10^1		44	(4)
20	2×10^1		45	(2) INTEGRATION TIME
21	1×10^1		46	(1) Command
22	8×10^0	Not available	47	AUTORANGE Command
23	4×10^0	when using	48	(1)
24	2×10^0	Adaptor	49	(2) RANGE Command
25	1×10^0	Cable.	50	(4)

Systems Interface 50-way Cannon Socket Connections.



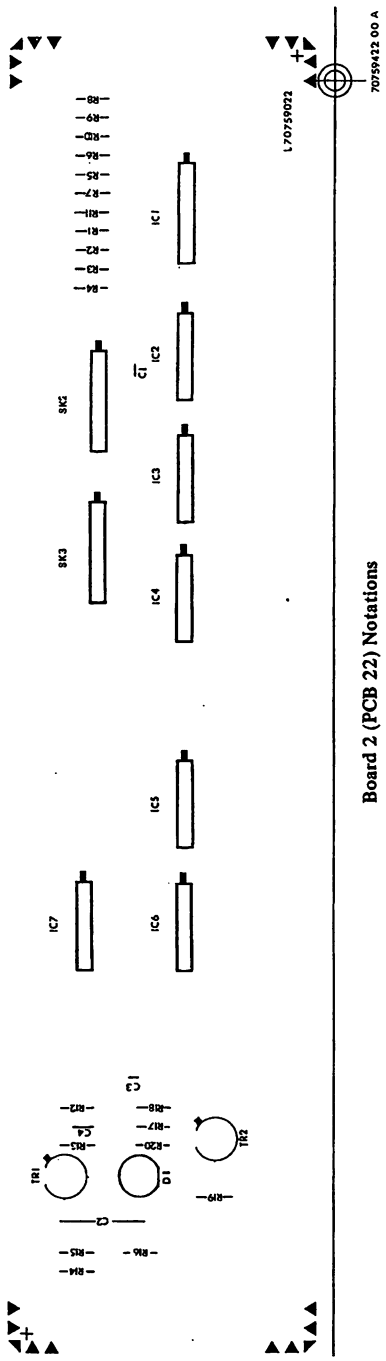
NON PREFERRED RANGE OUTPUT CODE		
1000V	000	10MΩ
100V	001	1MΩ
↓		
10mV	101	100Ω
	110	10Ω

PREFERRED RANGE OUTPUT CODE 6 X 9's	
10MΩ	010
1MΩ	1000V 011
100k	100V 100
100Ω	100mV 111
10Ω	10mV 000

FOR FIVE X 9's PREFERRED CODE SUBTRACT ONE

CABLE T, CONNECTS TO SK1 ON BOARD 3 — 16 PIN D.I.L. SOCKETS
CABLE S, CONNECTS TO SK3 ON BOARD 2 — 16 PIN D.I.L. SOCKETS
NUMBERS NEXT TO CIRCLES REFER TO PIN CONNECTIONS ON 50 WAY CANNON PLUG PLA

Board 1 Diag. 9.1



Board 2 (PCB 22) Notations

Board 2 Diag 9.2

RANGE COMMAND codes applied to IC1 are converted to internal codes, by incrementing by 1 for the OHMS mode and 2 for the VOLTS DC/AC mode.

IC3a, b and d disable these range commands if:–

1. ERROR is detected by the instrument on SK3 pin 4 (IC 6 pin 1 goes low).

2. in Local operation, IC7 pin 1 high→IC6 pin 6 high →IC6 pin 2 low.

3. in the Self Check mode, SK3 pin 10 low.

RATIO COMMAND (Low at SK2 pin 1) is transmitted to the instrument via SK3 pin 5 unless:–

1. It is in the OHMS mode (IC 5 pin 4 not low)

or 2. in the Self Check mode (IC 6 pin 4 low)

or 3. in Local operation (IC 7 pin 1 high).

MODE codes on SK2 pins 9 and 10 are transmitted to the instrument unless:–

1. It is the Self Check mode

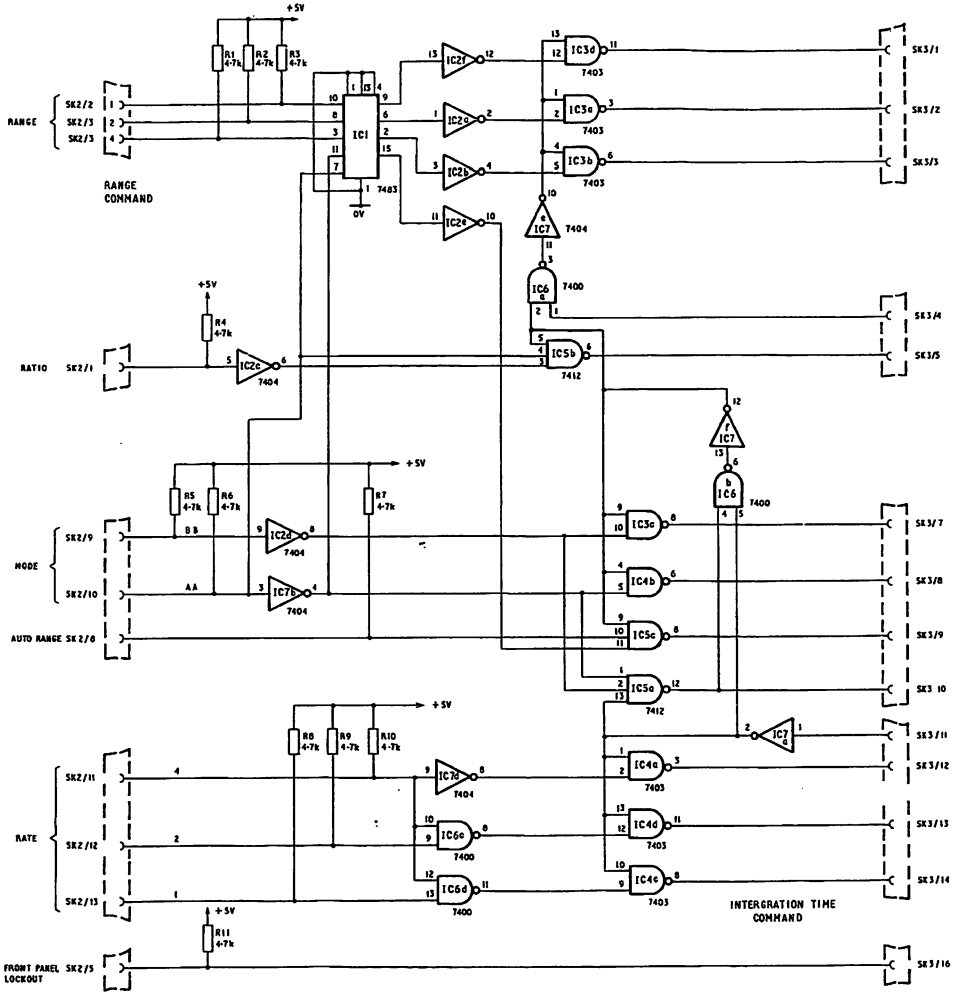
or 2. in Local operation when IC3c and IC4b will block commands.

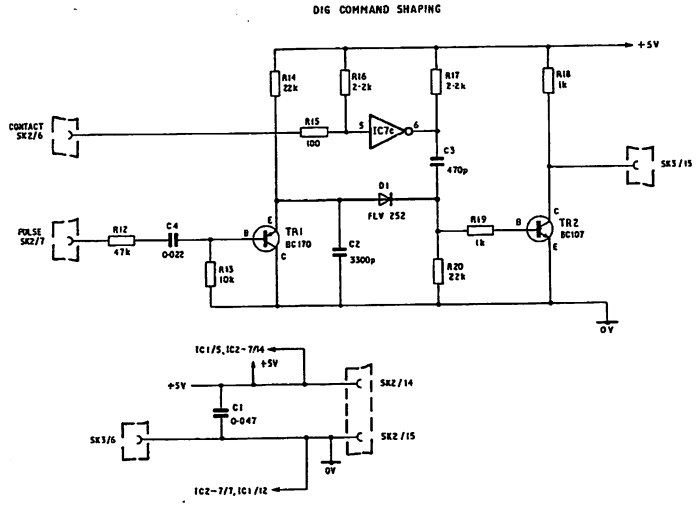
RATE COMMANDS on SK2 pins 11, 12 and 13 are transmitted to the instrument via SK3 pins 12, 13 and 14 unless it is in Local operation, when the commands will be blocked by IC4 a, c and d.

IC6c and d force code 0 on SK3 pins 12, 13 and 14 for input commands 0, 1, 2, 3. Input commands 4, 5, 6, 7 are unaffected.

CONTACT and PULSE SAMPLES are filtered for optimum noise rejection and OR-ed together to produce a low on SK3 pin 15. The specifications for these inputs are given in this section of the manual.

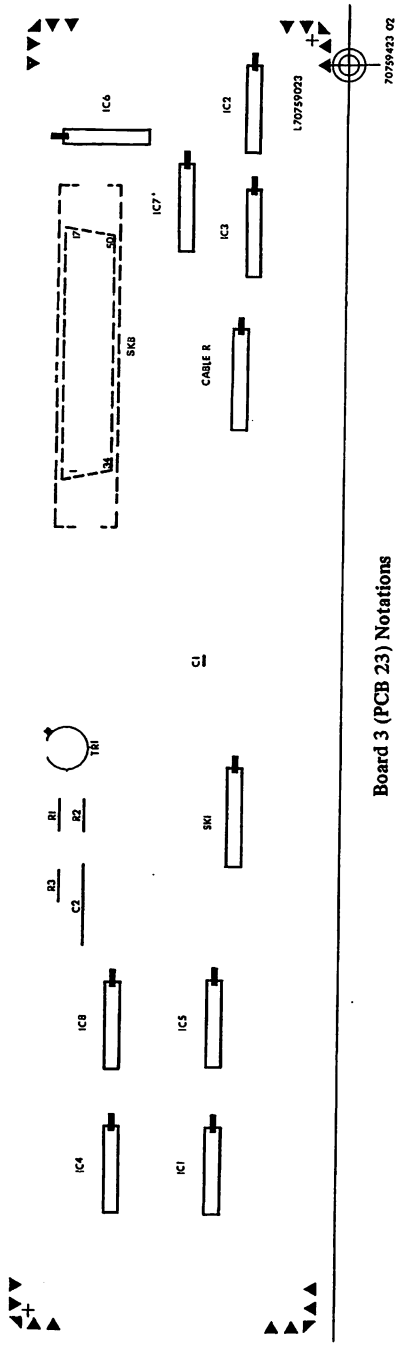
← PCB 22 Notations





SK2 CONNECTS TO CABLE R ON BOARD 3
SK3 CONNECTS TO CABLE S ON BOARD 1
} 16 PIN D.I.L. SOCKETS

Board 2 Diag. 9.2



Board 3 (PCB 23) Notations

Board 3 Diag 9.3

Input Commands on SKB are passed directly to board 2 via cable R.

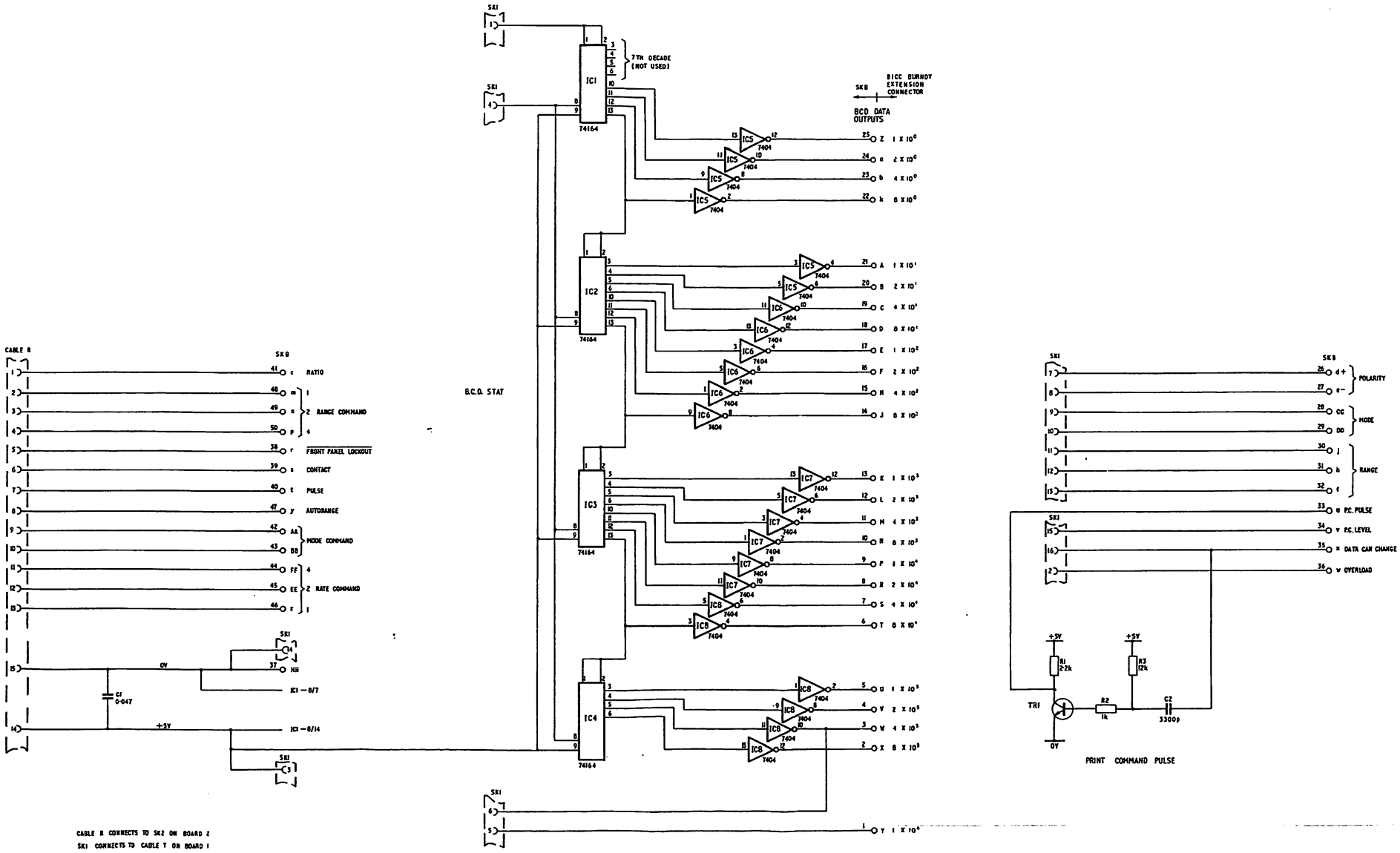
Output information from board 1 is applied directly to SKB.

A PRINT COMMAND PULSE of 12μs duration is produced by TR1 when DATA CAN CHANGE goes low.

32 clock pulses are applied to the clock inputs of shift registers IC's 1 to 4 at 800 kHZ while the serial information is applied to IC1 pins 1 and 2. The transfer lasts for 40μs. IC's 5 to 8 invert and buffer the outputs.

Note. Current jumper lead notations refer to modules ser no 000161 onwards. On modules prior to this serial number:
Cable R was annotated T.
Cable S was annotated R.
Cable T was annotated S.

← PCB 23 Notations



Board 3 Diag. 9.3