TRANSMISSION MEASURING SET PMG-3

for measuring level, noise, and frequency
in the frequency range 50 Hz to 20 (110) kHz

Service Manual BN 9202; Series A ...

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Wandel & Goltermann

PRECISION ELECTRONIC
MEASURING INSTRUMENTS

6 PRELIMINARY NOTES

6.1 INTRODUCTION TO THE SERVICE CONCEPT

Maintenance and repair are the two main tasks which occur in servicing of measuring equipment. The equipment handbook with its operating instructions, its servicing instructions and the Appendix provides all necessary information.

The operating instructions provide all necessary basic information on the instrument. Section 5 of the operating instructions describes all non-electrical maintenance work such as cleaning and lubrication of moving parts, if such work is necessary.

The servicing instructions provide all special information for repair. Section 8 "Checking important technical data" is used for both maintenance and repair.

The information was selected such that an experienced technician can carry out all common repair work. Tasks which are normally carried out only during manufacture of an instrument have generally been omitted.

The Appendix contains all block diagrams, circuit diagrams, parts lists and component layout plans of the printed circuit boards. In addition, it provides the necessary information for reading the circuit diagrams and ordering spare parts. It contains a German/English/French/Spanish translation list for all important terms used in the Appendix.

6.2 TEST EQUIPMENT

The test equipment listed here should be regarded as recommendations. Equivalent instruments made by other manufacturers can also be used.

Instrument	Requirements	Rec. type	Manufacturer	Used in section
Digital frequency counter	50 Hz ... 20 kHz	PM 6614	Philips	8.2
Level Meter	50 Hz ... 60 kHz	SPM-11 with PSE-11	W&G	8.4
Milliwatt Power Meter	50 Hz ... 110 kHz	EPM-1 with TKS-10, TKSA-600, TKSE-600	W&G	8.3 8.6
Level Generator	50 Hz ... 110 kHz Z_{out} = 600 Ω Balanced	PS-19	W&G	8.5, 8.6 8.7
Termination resistor	600 Ω ± 1 %			8.4
Oscillo-scope	DC ... ca 50 MHz with probe	HM 705	Hameg	7.7
Digital voltmeter	4 $\frac{1}{2}$ digits	8050 A	Fluke	7.7

Figure 6-1 Test equipments

7 NOTES ON FAULTFINDING AND REPAIRS

7.1 INSTRUCTION SAFETY

7.1.1 PROTECTION AGAINST ELECTRICAL ACCIDENTS

Protection class

This instrument belongs to safety class I in accordance with VDE 0411 or IEC Publ. 348. The included mains cable contains a protective conductor. Except in specially certified rooms, the plug of this cable may be inserted only in outlet sockets with a protective conductor connection. It is not permitted to disconnect the protective conductor, either inside or outside the instrument.

Opening the instrument

Opening covers or removal of parts with the aid of tools can expose parts which carry voltages. Terminal points may also carry voltages.

Before opening the instrument, it must be disconnected from all voltage supply sources.

If calibration, maintenance, or repair of the open instrument with voltage connected is unavoidable, then this may be carried out only by a trained person who is familiar with the accompanying risks.

Capacitors in the instrument may retain their charges even when the instrument has been disconnected from all voltage sources; see the circuit diagrams for these capacitors.

Fuses

Only fuses of the specified ratings may be used.

Repair, replacement of parts

Repairs are to be carried out in a workmanlike manner. Particular attention should be paid to ensuring that the design features of the instrument are not changed such that its safety is reduced. In particular, the leakage paths and air gaps and the spacing provided by the insulation must not be reduced.

Use only original parts for replacement. Other replacement parts are permissible only if they do not reduce the safety characteristics of the instrument.

Tests after repair and maintenance

Testing the protective conductor.

Correct connection and good condition are checked by visual inspection and by measuring the resistance between the protective conductor pin of the plug and the instrument. The resistance should be < 0.5 Ω. During the measurement, move the cable; variations in the resistance value indicate a damaged cable.

Testing the insulation resistance.

Measure the insulation resistance at 500 V DC between the voltage pins of the mains plug and the protective conductor pin with the mains switch of the instrument set to "On". The insulation resistance should be > 2 MΩ.

7.1.2 CIRCUIT PROTECTION NOTES

Handle MOS components with care!

Some of the components in this instrument are MOS (metal oxide silicon) components. These are easily damaged or destroyed by static charges, ripple voltages of ungrounded instruments, or other interference voltages. Destruction by static charges can be avoided by observing the following rules:

- Wherever possible, leave MOS components in the original packing materials until they are required for use. All pins of the components must be connected conductively (black, electrically conductive foam material).
- Before removing MOS components or printed circuit boards carrying such components, bring the electrically conductive part of the packing materials into contact with a conductive bench top or the chassis of the instrument being repaired.
- Before touching MOS components, grasp the reference potential conductor with one hand.
- All tools, instruments, the part of the instrument being repaired and the person carrying out the repair should have the same potential as the reference potential conductor (e.g. a conductive bench top or, alternatively, the chassis of the instrument being repaired). For this reason, tools with which MOS components are to be handled should first be brought into contact with the reference potential. Tools must not have insulated handles.
- If work is carried out on a printed circuit board or other subassemblies of the instrument while these are removed from the instrument, and if these are not placed on a conductive bench top, then the ground of the printed circuit board or subassembly must be connected to the reference potential.

Destruction due to ripple voltages during soldering can be avoided by establishing a permanent connection between the soldering iron and the chassis of the instrument being repaired.

MOS components can be identified by the letters MOS, CMOS, or MOSFET in the component designation of the parts list.

7.2 S O L D E R I N G I N S T R U C T I O N S

We recommend the use of thin solder with only a small amount of flux. The following should be noted:

- Soldering times for all components $\leq$ 5 s;
- Soldering temperatures $\leq$ 260°C;
- Avoid splashing flux on switch contacts;
- When soldering on switch contacts or other electromechanical components, ensure that the flux does not creep onto the contact surface.

Instructions for unsoldering multi-pin components:

By far the best method is to extract the solder from each pin with the aid of a special desoldering tool. After removal of solder, move the component slightly to ensure that all pins are free. Do not use force! Through-plated holes are very sensitive to tension during desoldering! In the case of dual inline components, damage to the printed circuit board can be avoided by cutting off the pins on the component side and then unsoldering each pin separately.

Soldering on thin film circuits

Soldering on thin film circuits requires precise temperature control, minimum soldering times and special soldering aids. The danger of destroying the circuit by normal procedures is so great that we recommend that the complete thin film circuit be replaced.

7.3 INSTRUMENT IDENTIFICATION

The following instrument identification is necessary for enquiries, ordering spare parts, or checking whether these servicing instructions belong to the instrument to be repaired:

Type designation, designation of the special version, installed options, series index and serial number.

Figure 7-2 shows where the instrument identification can be found.

7.4 REMOVAL OF KNOBS AND COVERS

See Figure 7-1 for removal of control knobs

See Figure 7-2 for removal of covers

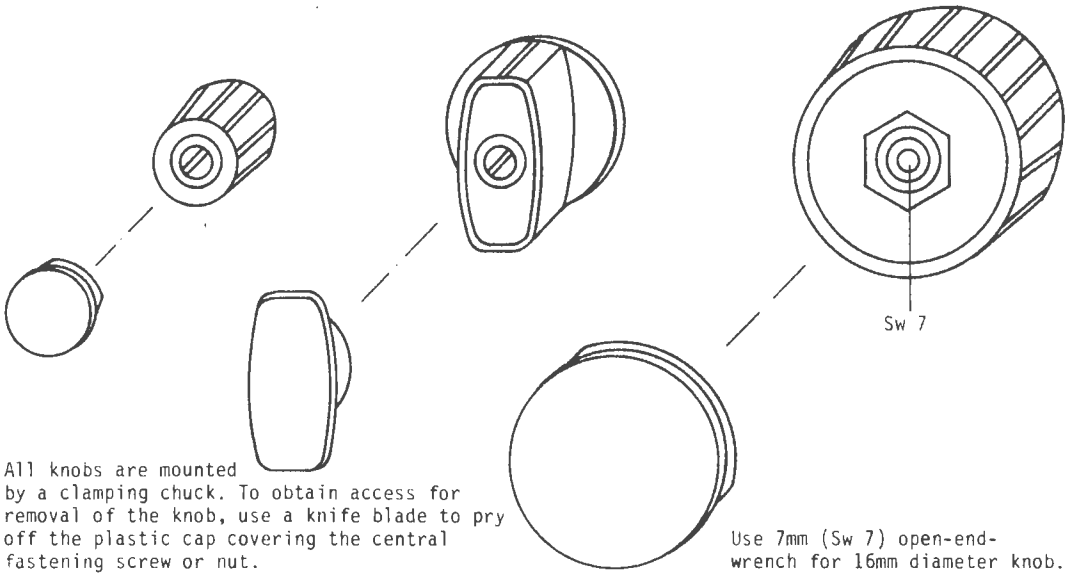
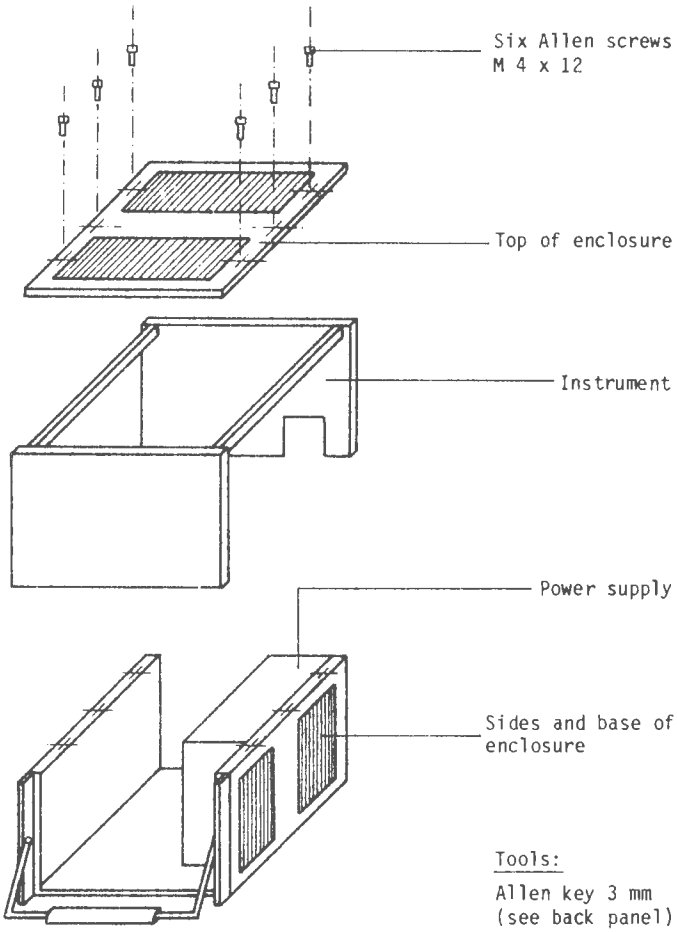


Figure 7-1 Removal of knobs

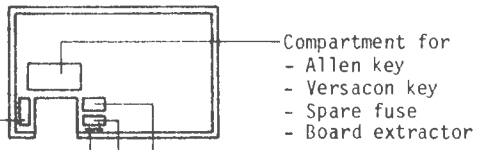
After the 6 upper Allen screws have been removed, the instrument is lifted out of the enclosure. The power supply remains in the enclosure, but is connected to the instrument via a cable harness.



Tools:

Allen key 3 mm
(see back panel)

Back panel:



Instrument address

1	16
2	●
3	18
4	19
5	20
6	21
7	22
8	23
9	24
10	25
11	26
12	27
13	28
14	29
15	30

Indicates if signature list has been provided

Version .....type	
BN ...../01	
BN ...../02	●
BN ...../03	

Version

..... options	
BN ...../00.01	
BN ...../00.02	●
BN ...../00.03	

Fitted options

Figure 7.2 Removal of covers and instrument identification

7.5 POSITIONS OF SUBASSEMBLIES ADJUSTMENT COMPONENTS, TEST POINTS

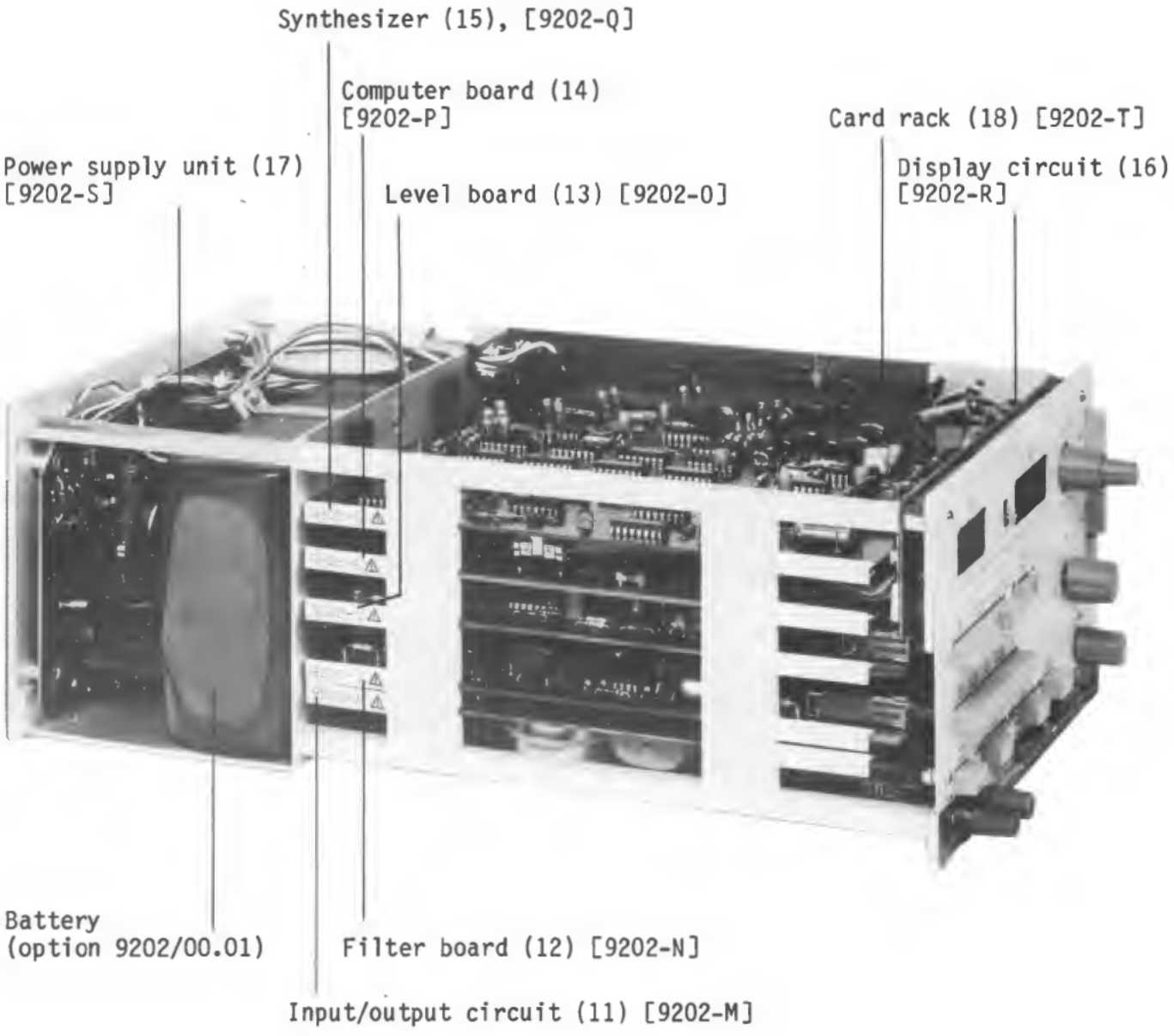


Figure 7-3 Arrangement of printed circuit boards

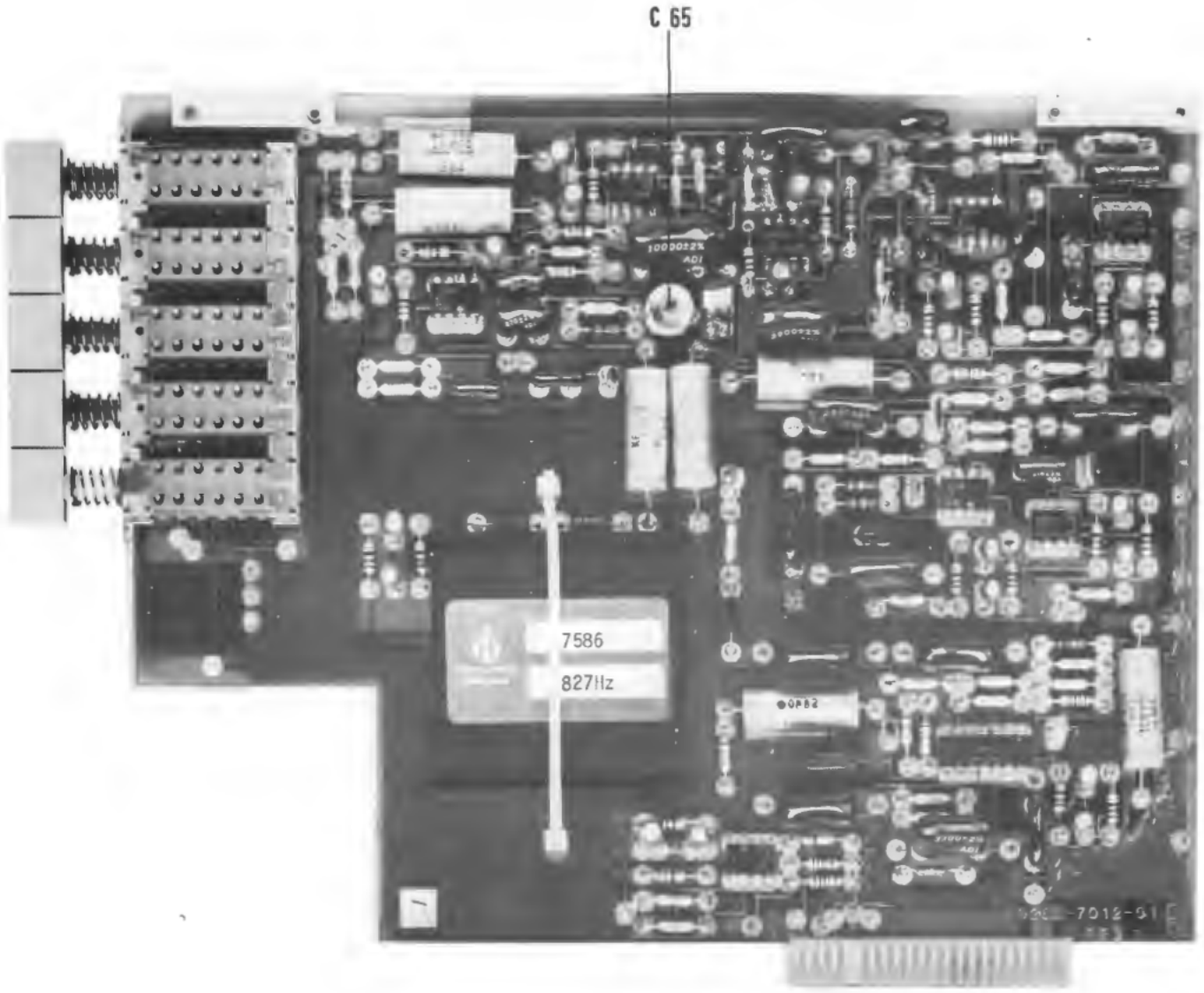


Figure 7-4 Filter board (12) [9202-N]

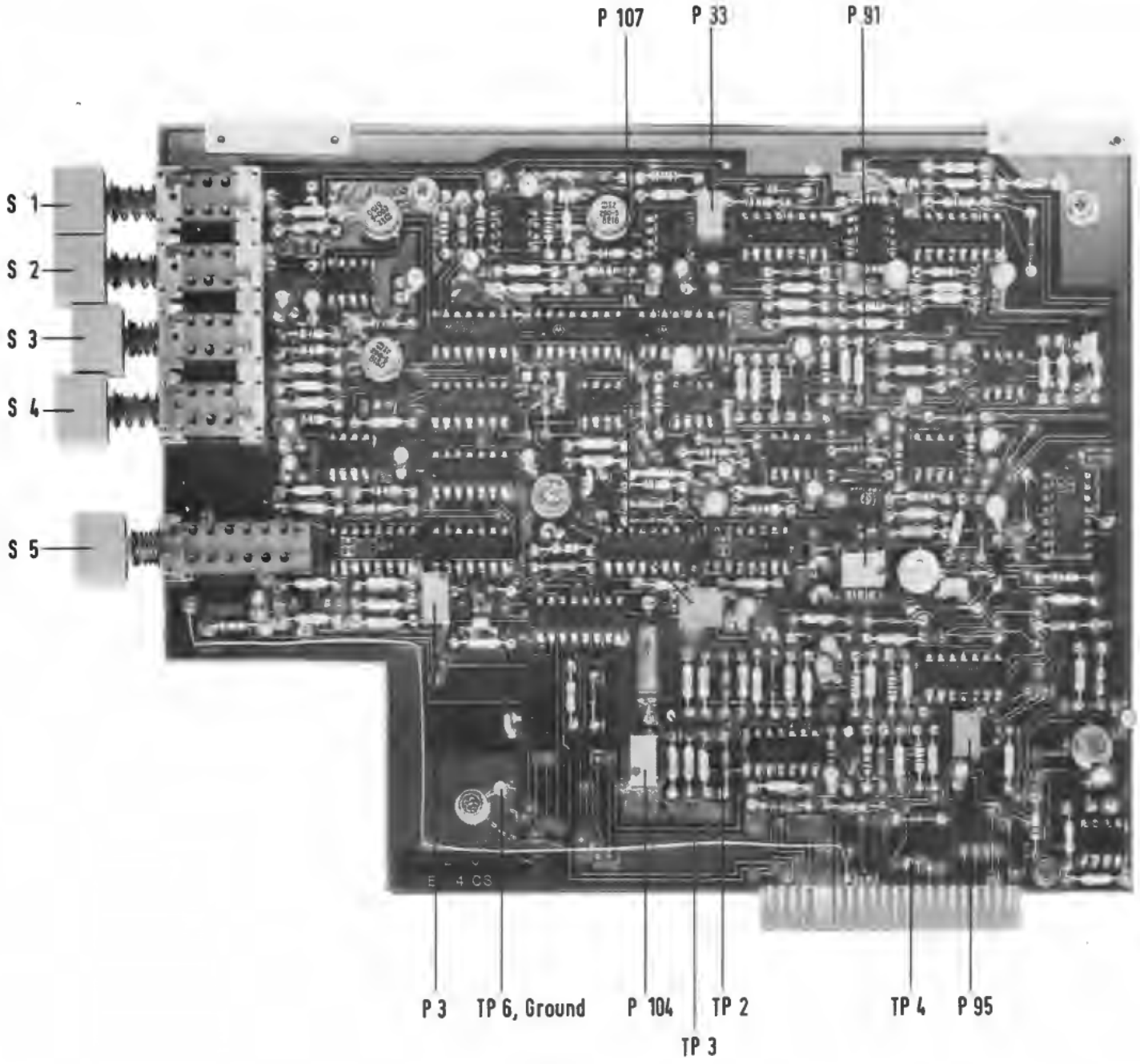


Figure 7-5 Level board (13)

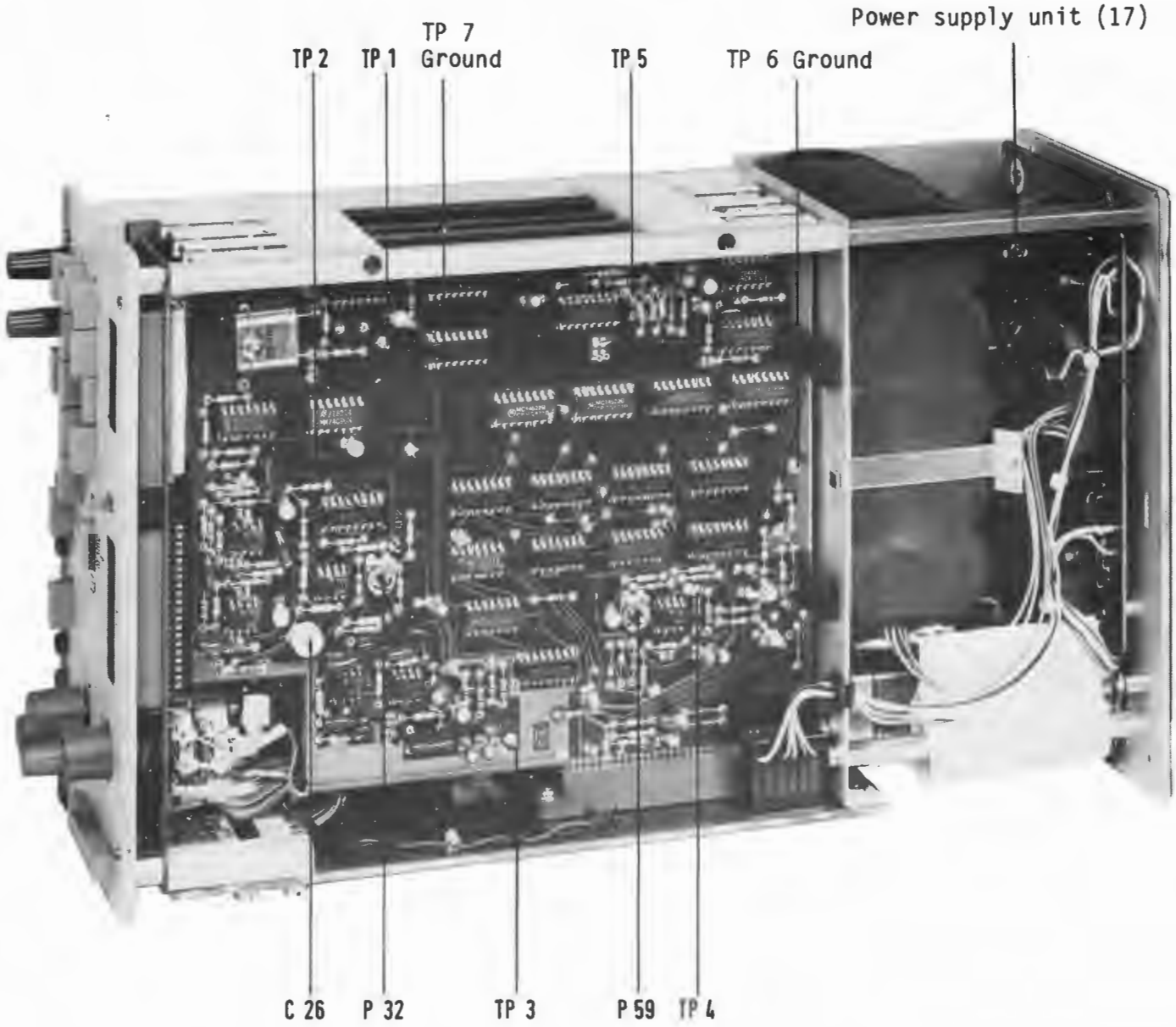


Figure 7-6 Synthesizer (15), [9202-Q]

7.6 ADJUSTMENT INSTRUCTIONS

Trimmer	Adjustment	Section
P 1303	Adjustment of 40 dB attenuator	
P 1333	Gain adjustment (absolute level calibration)	
P 1395	Reference voltage adjustment; measure at TP 2, adjust for 1.0 V ± 1 mV	9.3.2
P 13104	Reference voltage adjustment; measure at TP 3, adjust for 0.903 V ± 7 mV	
P 13107	Log slope adjustment; measure at TP 4, pulse width 10 ms/dB	
C 1501	Solder on a capacitor with a value for a frequency of 1 MHz ± 5 Hz at TP 1	9.5.1
C 1526	Mixer balance, 40 kHz signal; measure at TP 3, residual signal ≤ -70 dB	9.5.4
P 1532	Mixer balance, 40.820 kHz carrier; measure at TP 3, residual carrier ≤ -70 dB	
C 1507	AGC voltage adjustment. Solder on value of capacitor as required. Measure at TP 5: 7 V ± 1 V at f = 20 kHz, 4.5 V ± 0.5 V at f = 0 Hz.	9.5.2
P 1559	Offset adjustments; adjust for 0.0 V at TP 4.	9.5.3

Figure 7-7 List of adjustment components

8 CHECKING IMPORTANT TECHNICAL DATA

8.1 INTRODUCTION

This section describes procedures with which the most important characteristic data of the instrument can be checked. Wherever possible, the use of commercially available test equipment is suggested.

Unless otherwise specified, the tests should always be carried out within the nominal operating ranges of temperature and mains voltage.

If the technical data specify a warming-up period, then the tests should be started only after this period has elapsed.

Checking of important technical data is intended to show whether the indicated measured value lies within the guaranteed error limits. These checks can be fully successful only if the intrinsic error of the test configuration used is negligible.

Otherwise, the following rule applies:
If the error of the test configuration used is $\pm m$ and if the guaranteed error limits for the instrument being tested is $\pm e$, then

a value outside the limits $\pm(e + m)$
indicates that the guaranteed error limits
have certainly been transgressed;

a value within the limits $\pm(e - m)$
indicates that the guaranteed error limits
have not been transgressed.

The values for e and m are specified for each test. The value m depends on the test equipment used and must therefore be determined separately if other test equipment is used.

For a systematic check of the data, proceed in the sequence specified here.

Adjustment of the instrument being tested should be carried out only if the result of one or more checks lies outside the limits $\pm(e + m)$.

8.2 SEND FREQUENCIES

Required test equipment:

1 digital frequency counter PM 6614 Philips

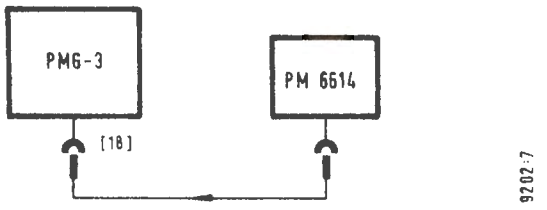


Figure 8-1 Test configuration

Equipment settings:

PMG-3:

Display	[7]	: generator
Send frequency	[5]	: CONT.
Resolution	[2]	: 1 Hz
Measuring mode	[6]	: level
Send level	[4]	: 0.0 dBm
Input switch	[12]	: A receiver B generator

PM 6614:

Measuring time	10 seconds

Check the frequencies listed in the table below. Ensure that the indications on the PMG-3 and PM 6614 are identical. Change the frequencies with [5] and [9].

Frequency (PMG-3)	Setting	Error limits (e)	Test configuration error (m)
19999 Hz 420 Hz 820 Hz 3000 Hz	[9] CONT. [5] 420 [5] 820 [5] 3000	±1 Hz	Negligible

Figure 8-2 Table for checking send frequencies

8.3 SEND FREQUENCY RESPONSE

Required test equipment:

1 Milliwatt Power Meter	EPM-1	W&G
1 Test Probe	TKS-10	W&G
1 Test Probe Adapter	TKSA-600	W&G

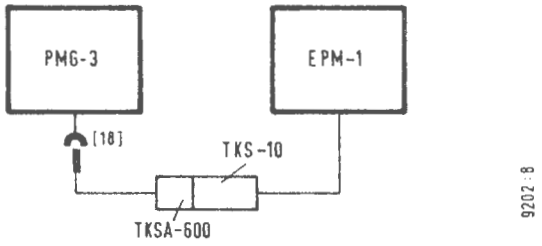


Figure 8-3 Test configuration

Equipment settings:

PMG-3:

Display	[7]	: generator
Measuring mode	[6]	: level
Input impedance	[12]	: 600 Ω
Send frequency	[5]	: 820 Hz
Input switch	[12]	: A receiver
		B generator

EPM-1:

Measuring range : 0 dBm ± 0.2 dBm

Adjust the level control [4] for an indication of 0 dBm on the EPM-1. At the frequencies listed in the table below (with switch [5] set to CONT.), check the level variations.

Frequency	50 Hz	200 Hz	820 Hz	5 kHz	10 kHz	20 kHz
Error limit (e)	±0.5 dB	±0.1 dB	Ref.	±0.1 dB	±0.1 dB	±0.1 dB
Test configuration error (m)	±0.02 dB					

Figure 8-4 Table for send frequency response

8.4 GENERATOR HARMONIC DISTORTION

Required test equipment:

1 Selective Level Meter	SPM-11	W&G
1 Level Generator	PSE-11	W&G
1 600 Ω BNC termination resistor		

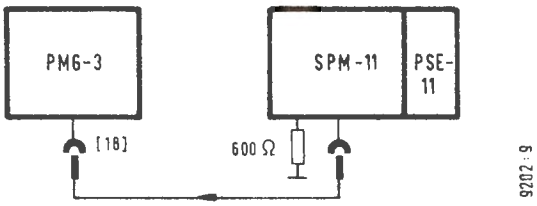


Figure 8-5 Test configuration

Equipment settings:

PMG-3:

Display	[7]	: generator
Input impedance	[12]	: 600 Ω
Measuring mode	[6]	: level
Input switch	[11]	: A receiver
		B generator
Send frequency	[5]	: CONT.

SPM-11:

Measuring mode : LINEAR, low distortion
PSE-11/tuning : f

Set the PMG-3 and the SPM-11 to the same level and frequency. Tune the SPM-11 for a peak indication. Measure the harmonic distortion ratios at 2f and 3f with the PSE-11.

PMG-3 Send level	0 dBm	+10 dBm			
SPM-11 Filter	8 Hz	40 Hz			
Frequency	50 Hz	300 Hz	820 Hz	3 kHz	20 kHz
2f, 3f	≥ 41 dB	≥ 62 dB	≥ 62 dB	≥ 62 dB	≥ 62 dB
Test configuration error (m)	±0.7	±1.5 dB	±1.5 dB	±1.5 dB	±1.5 dB

Figure 8-6 Table for generator harmonic distortion ratio

8.5 L E V E L D I S P L A Y

Required test equipment:

Level Generator PS-19 W&G

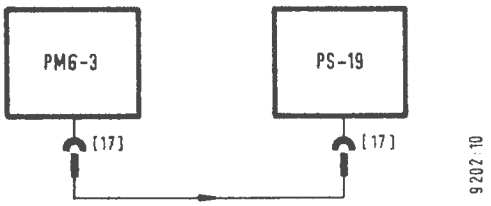


Figure 8-7 Test configuration

Equipment settings:

PMG-3:

Display [7] : receiver
Measuring mode [6] : level
Input impedance [11] : 600 Ω
Input switch [12] : A receiver
B generator

PS-19:

Frequency : 820 Hz
Impedance [15] : 600 Ω
Level [4] : 0 dBm

Set up each of the levels shown in the table below on the PS-19 and read off the corresponding values on the PMG-3.

PS-19 Send level	Error limits (e)	Test configuration error (m)
0 dBm +10 dBm -10 dBm -20 dBm -30 dBm	±0.1 dB	±0.15 dB
-40 dBm -50 dBm -60 dBm	±0.2 dB	±0.2 dB
-70 dBm	±0.5 dB	

Figure 8-8 Table for level display

8.6 RECEIVER FREQUENCY RESPONSE

Required test equipment:

1 Milliwatt Power Meter	EPM-1	W&G
1 Test Probe	TKS-10	W&G
1 Test Probe Adapter	TKSA-600	W&G
1 Calibration Adapter	TKSE-600	W&G
1 Level Generator	PS-19	W&G

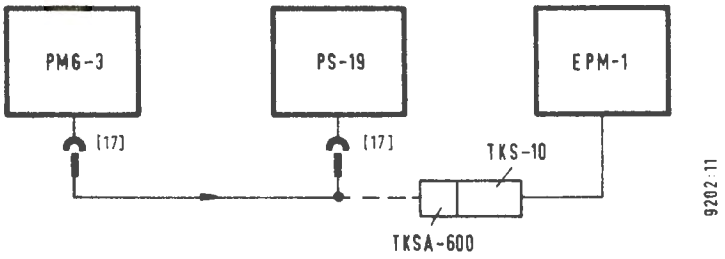


Figure 8-9 Test configuration

Equipment settings:

PMG-3:

Display	[7]	: receiver
Input impedance	[11]	: 600 Ω
Measuring mode	[6]	: level
Input switch	[12]	: A receiver B generator

PS-19:

Frequency		: 820 Hz
Level	[4]	: 0 dBm
Impedance	[15]	: 600 Ω

EPM-1:

Measuring range switch : 0 dBm ± 0.2 dBm
Calibration level switch : 0 dB, 75 Ω

Measurement of the intrinsic frequency response:

Calibrate the EPM-1 and connect it to the PS-19. At the frequencies shown in the table below, measure and note the levels shown on the EPM-1. Connect the PS-19 to the PMG-3 with a short cable. Then measure and note the PMG-3 display at the various frequencies. The difference between the results of the two measurements at each frequency must lie within the error limits (e).

Frequency setting on PS-19 (in Hz)	Error limits (e)	Test configuration error (m)
200	±0.5 dB	±0.02 dB
820 3000 10000 20000	±0.1 dB	
50000 110000	±0.2 dB	

Figure 8-10 Table for receiver frequency response

8.7 C H E C K I N G T H E F I L T E R S

Required test equipment:

1 Level Generator PS-19 W&G

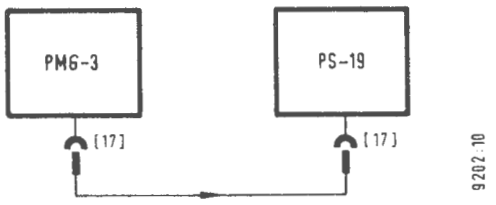


Figure 8-11 Test configuration

Equipment settings:

PMG-3:

Display [7] : receiver
Input impedance [11] : 600 Ω
Input switch [12] : A receiver
B generator

PS-19:

Frequency : 1000 Hz
Level [4] : 0 dBm
Impedance [15] : 600 Ω

Set up the PMG-3 as shown in the following table and check the indicated levels.

Measuring mode [6]	Filter [8]	Level display (dBm)	Test configuration error (m)
Level	-	0 ± 0.1	
Noise, sound-programme	Flat	0 ± 0.5	
Noise, sound-programme	Weighted	0 ± 1.0	±0.15 dBm
Noise, telephone	Flat	0 ± 0.5	
Noise, telephone	Weighted	1 ± 1.0	
Noise, telephone	Notch	< -50	

Figure 8-12 Table for checking the filters

9 CIRCUIT DESCRIPTION

9.1 INPUT AND OUTPUT SECTION, circuit diagram (11)

The input and output section consists of 3 units:

- Input stage
- DC loop-holding circuit
- Output stage

This assembly processes all input and output signals. In addition, the assembly contains a DC loop-holding circuit for output/input socket "A".

9.1.1 INPUT STAGE

The input stage consists of the termination resistors, a transformer which converts the balanced input signal to an unbalanced signal and a 6/8 dB amplifier (IC 2/1). Furthermore, the input stage has a 32/34 dB attentuator and an isolating stage (IC 2/2) for measurement of noise to ground (common mode noise). The analog switch (IC 1) selects the operating modes "Normal" and "Noise to ground" and also switches the gain of the input amplifier when the input impedance is changed. The gain of the amplifier is 8 dB at 600 Ω and 6 dB at 900 Ω. Capacitor C 14 compensates for the overall frequency response of the instrument. Switch S 1 connects input socket "A" to the socket for the dial-up unit, which permits dial-up and seizure of a telephone line.

Switch S 4 inverts the functions of sockets "A" and "B". If one socket is connected to the input, then the other socket acts as an output socket.

Switch S 2 permits selection of normal termination or high impedance input. The input impedance (600 Ω or 900 Ω) is selected with switch S 3. Capacitor C 2 protects the input transformer Ü 1 against DC voltages.

The diode circuit consisting of Gl 8, Gl 9, Gl 24 and Gl 25 limits the secondary voltage of the input transformer Ü 1 and protects the input amplifier against destruction by excessive alternating voltages. Resistors R 5 to R 7 form the 32/34 dB attenuator for measurement of noise to ground.

9.1.2 DC LOOP-HOLDING CIRCUIT

The DC LOOP-HOLDING circuit consists of IC 5, T 4 to T 6 and the associated components. Its purpose is to provide a low resistance for maintaining the direct current of a dial-up telephone connection without loading the alternating voltage. The bridge rectifier consisting of Gl 11 to Gl 14 allows the circuit to accept a direct current with positive or negative polarity. Transistors T 4 to T 6 drive IC 5, which acts as the switching element. IC 5 also acts as a current limiter. Capacitors C 12 and C 13 filter out the alternating components of the signal in order to ensure that the impedance of this circuit remains high over the whole operating and frequency range.

9.1.3 OUTPUT STAGE

The output stage amplifies and balances the signal which comes from the frequency generator. The output impedance can be switched between 600 Ω and 900 Ω with switch S 5.

The input signal for this output stage is amplified by 18 dB in amplifier 3/1. The amplified signal is both connected to the switch T 3 and to the gain matching circuit (R 28 to R 30) of the output power stage via an attenuator. Resistor R 29 determines the output level.

The output power stage consists of IC 3/2 and transistors T 1 and T 2. It is connected as a current source. The resistors R 3 and R 4, which can be selected with switch S 5, determine the output impedance. Transformer Ü 2 converts the unbalanced signal into a balanced output signal. Capacitor C 9 blocks the DC voltage and thus protects transformer Ü 2. The diode circuit Gl 3, Gl 4, Gl 22 and Gl 23 acts as a limiter circuit for the primary side of Ü 2 and thus protects the power amplifier against excessive alternating voltages at the output socket. The frequency response of the output stage is determined by capacitors C 10, C 11 and inductance L 1. The value of capacitor C 11 can be changed to smooth the frequency response at the upper end of the frequency range. Resistor R 26 is short circuited in the operating mode 600 Ω in order to provide the necessary gain compensation.

Switch T 3 drives amplifier stage (IC 4) which has a gain of 16.96 dB. The output of this stage is connected back to the receiver of the instrument to permit measurement of the send level. Switch T 3 switches off this output when the instrument is set to the operating mode "Receive", thus preventing cross talk via the send/receive switch S 4.

9.2 F I L T E R S E C T I O N, circuit diagram (12)

The filter section provides 4 separate weighting characteristics which comply with the Bell specification 41009. It also contains a 1010 Hz notch filter to permit noise measurements in the notch gap. As the notch filter consists of a hybrid circuit (Fi-1), it requires no adjustment.

The four filters, namely sound-programme channel weighted flat (15 kHz), sound-programme channel weighted, telephone (voice) channel flat (3 kHz) and telephone weighted (C weighting filter) consist of active high and low-pass filters.

In order to save power, each filter receives its supply voltage only when it is switched on. Activation is carried out by the switch groups "A" and "B" of each "selection switch".

The quadruple operational amplifier IC 1, with its related components, forms the C weighting filter when connected in series with the telephone filter. These two filters receive the supply voltage together.

The dual operational amplifier IC 2, IC 3 and the related components form the filter for the flat telephone channel. IC 4 and IC 5 and the related components form the filter for the weighted sound-programme. The flat sound-programme filter is constructed with IC 6, IC 7, IC 8 and the related components. The dual operational amplifier IC 9 buffers the input and output of the filter section. It is the only assembly in this circuit which always receives voltage, regardless of which filter is selected. This permits the operating mode "Wideband noise" (no filter in the circuit). The switch configuration permits the use of the 1010 Hz notch filter either together with any one of the four filter types or alone in the operating mode "wideband noise".

9.3 AUTOMATIC RANGE SWITCHING AND RECTIFIER CIRCUIT, board [9202-D]

The automatic range switching and rectifier circuit is the heart of the PMG-3. It amplifies, attenuates and rectifies the input signal. It also generates digital signals which correspond to the level of the input signal. The dynamic range is 99.9 dB.

Short functional description:

Variable attenuator stages and fixed amplifier stages are connected alternately in series. Adjustment of the attenuation is controlled by an up/down counter. The output signal of the last amplifier stage is first rectified and monitored by a window comparator. Up and down counting pulses are generated until the rectified signal lies within the window. Upward and downward counting increases or decreases the attenuation in 1 dB steps. The data of the up/down counter are also connected to the computer section, where the level display of the input signal is calculated with a resolution of 1 dB.

When the DC signal from the rectifier lies within the window, its maximum variation can be 1.8 dB. This is connected to an analog-digital converter which provides the 0.1 dB resolution.

Active low-pass filters are used to limit the bandwidth to 230 kHz in the operating modes "Level" and "Sound-programme" and to 35 kHz in the operating mode "Noise".

Two rectifiers are provided: a true RMS rectifier for level and noise measurements and a quasi-peak rectifier for sound-programme measurements.

9.3.1 MEASURING MODES

1.) Level measuring mode:

The switch SI/I selects the unweighted signal from the filter board. After passing through the attenuator and amplifier stages, the signal is connected directly to the RMS rectifier.

2.) Sound-programme noise measuring mode:

The switch SI/I again selects the unweighted signal and passes it via analog switch IC 30/2 to the quasi-peak value rectifier.

3.) Telephone noise measuring mode:

The switch SI/III selects the weighted signal from the filter board. IC 17, a 35 kHz low-pass filter with a gain of 10 dB, is connected into the signal path before the RMS rectifier.

4.) Noise to ground measuring mode:

Switch SI/IV sets up the same signal path as SI/III. In addition, it initiates 40 dB correction in the computer circuit. Furthermore, it switches the input/output section to the measuring mode noise to ground.

5.) Send level measuring mode:

Regardless of the positions of switches SI/I - IV, switch S 5 activates the RMS rectifier. In order to prevent cross talk between the input signal and the output signal, the input/ output section is switched to the measuring mode "Noise to ground". This reduces by 40 dB the input signal reaching the automatic range board.

9.3.2 AUTOMATIC RANGE SELECTION

0/20/40 dB attenuator (IC 1, C 3, P 3):

The signal which reaches the automatic range selection circuit first passes through the 0/20/40 dB attenuator, which is controlled by IC 1. C 3 provides compensation for the 20 dB attenuator at high frequencies. Potentiometer P 3 permits fine adjustment of the 40 dB attenuator.

20 dB amplifier stage (IC 2, C 6):

The output of IC 1 drives IC 2, a 20 d8 amplifier stage. C 6 protects this amplifier against DC offset voltages and couples the signal to the second attenuator.

0/20 dB attenuator (IC 3, IC 4):

IC 3 connects either 0 or 20 dB attenuation into the circuit. The signal is then amplified by 20 dB by amplifier stage IC 4, which is identical with amplifier stage IC 2.

0/20 dB attenuator (IC 5, IC 6, C 55):

IC 5, together with R 19 and R 20, also forms a 0/20 dB attenuator. C 55 provides frequency compensation. This amplifier drives IC 6, which has a gain of approximately 10 dB.

0/10 dB attenuator (IC 7, IC 8, P 33):

IC 7, together with R 26 and R 27, forms the next 0/10 dB attenuator, with C 58 for frequency compensation. This attenuator drives IC 8, which has a gain of approximately 10 dB, and which can be adjusted with P 33. This adjustment with P 33 is the absolute level calibration of the receiver.

0/4/8 dB attenuator (IC 9, IC 10):

IC 9 selects 0, 4, or 8 dB attenuation. IC 10 isolates this attenuator from the next stage.

0/1/2/3 dB attenuator (IC 11, IC 12):

IC 11 selects 0, 1, 2 or 3 dB attenuation. IC 12/1, which follows this attenuator, has a gain of approximately 14 dB. This drives a noise limiting filter (IC 12/2) with a limit frequency of 230 kHz.

Isolating stage (IC 29/1):

After the noise limiting filter, the signal branches to various other stages. IC 29/1 passes the signal to the frequency counter in the computer section and to the volume potentiometer for the monitor loudspeaker.

Attenuator overview

The following diagram shows the attenuators selected for various input levels when the PMG-3 is operated in the operating mode "Level".

Input level (dBm)	IC 1		IC 3	IC 5	IC 7	IC 9		IC 11		
	40 dB	20 dB	20 dB	20 dB	10 dB	8 dB	4 dB	3 dB	2 dB	1 dB
0		X	X	X	X	X				
-1		X	X	X	X	X				
-2		X	X	X	X		X	X		
-3		X	X	X	X		X		X	
-4		X	X	X	X		X			X
-5		X	X	X	X		X			
-6		X	X	X	X			X		
-7		X	X	X	X				X	
-8		X	X	X	X					X
-9		X	X	X	X					
+11	X		X	X	X					
+1	X		X	X						
-9		X	X	X	X					
-19		X	X	X						
-29			X	X	X					
-39			X	X						
-49				X	X					
-59				X						
-69					X					
-79										

Figure 9-1 Attenuator overview in mode "Level"

35 kHz low-pass filter with 10 dB gain (IC 17, IC 30/1, R 56):

IC 17 forms a 35 kHz low-pass filter with a gain of 10 dB. This is used together with the RMS rectifier for telephone noise measurements. The gain can be adjusted with R 56. IC 30/1 selects the signal source for the RMS rectifier; it passes the signal through the 35 kHz low-pass filter or bypasses this filter.

RMS rectifier (IC 18):

IC 18 is a true RMS rectifier. C 40 and C 41 block all DC voltages which may come from the preceding amplifier stages.

Quasi-peak value rectifier (IC 13, IC 14/1-3, IC 32):

IC 13, IC 14/1 and the related components form a full wave rectifier. Offset adjustment of the OPs is carried out with P 91. The frequency response can be adjusted with R 157. Increasing the value of R 157 attenuates the lower end of the frequency band. R 157 also affects the gain. C 25 is charged with the peak voltage of the rectifier. The residual ripple is reduced by IC 14/2, together with R 148 and C 60/61. IC 32 acts as a low resistance voltage source of approximately 0.9 V for rapid reversal of the charge on C 60/61.

Integrator (IC 14/4, IC 15/2):

IC 30/2 passes the DC signal to integrator IC 14/4. C 32 and C 33 are the integration capacitors. The signal is compared with the reference voltage of 1.000 V. The differential output voltage of this stage is connected to a window comparator. The integrator capacitor can be

discharged by switch IC 15/2. This discharge operation shortens the setting time of the automatic range selection circuit, as it ensures that the signal falls within the comparator window immediately after each step of the automatic range selection. If this were not the case, the output signal of the integrator would have to adjust level within the window in a series of steps, due to the large time constant.

Threshold comparators (IC 19/3, 4, IC 16/2, 3, 4):

R 75, 76, 77 and R 79 determine the threshold voltages which correspond approximately to a level difference of 1.8 dB from the input level. As long as the DC signal lies within the window, the output states of IC 19/3 and IC 19/4 remain unchanged. As soon as the DC signal moves outside the window, the automatic range selection circuit is adjusted in steps. The attenuation is changed in steps of 1 dB, either upwards or downwards, to return the DC signal within the window.

The two outputs of IC 19/3, 4 are connected to three gates. IC 16/2 acts as an "Or" gate. Whenever one of the two comparators is triggered, it generates a counter pulse. This is the counter pulse for the up/down counter. At the same time, this pulse is used to discharge the integration capacitor via IC 15/2, and to simultaneously switch off the input signal of the integrator with IC 15/1. Furthermore, the counter pulse triggers IC 22/2. This causes C 25 to be discharged via IC 31/1, and C 60/61 is charged to approximately 0.9 V via IC 31/2.

IC 16/3 and IC 16/4 form an RS flipflop. Depending on which of the two threshold comparators was triggered, the flipflop selects up or down mode for the up/down counter until the changed attenuation causes the DC signal to again lie within the window.

Analog/digital converter (IC 20, IC 15/4, IC 21, IC 22/1, IC 15/3, IC 29/2):

The level of the signal has a maximum range of 1.8 dB while the DC signal remains within the window.

This voltage is now connected to an analog/digital converter which has a resolution of 0.1 dB. This ADC converts the voltage into pulses. A variation in the pulse width of 1.0 ms corresponds to a level change of 0.1 dB. The DC signal coming from IC 14/4 is smoothed by R 74 and C 34. This smoothing circuit has a limit frequency of approximately 2 Hz. IC 20 compares the DC signal with the reference voltage of 1.000 V.

This reference voltage can be adjusted with P 95.

During initialization, switch IC 15/4 is closed, permitting capacitor C 47 to charge to the output voltage of IC 20. After a period of 10 ms, switch IC 15/4 opens and C 47 starts to discharge via R 106 and R 107. When the capacitor voltage reaches the threshold set with P 104, the comparator IC 21 triggers IC 22/1. The pulse width is thus proportional to the charge in capacitor C 47. The linearity of the discharge slope can be adjusted with potentiometer P 107, thus guaranteeing precise switching.

This pulse can be observed at TP 4; it is the positive part of the square wave.

A pulse from the computer section starts the ADC via diode G 7.

Whenever the automatic range selection circuit executes a step, C 34 is charged via IC 15/3 to one of two voltages. IC 29/2 produces these two voltages: 0.93 V for counting upwards and 1.07 V for counting downwards. The reason for this is to rapidly bring the input voltage of the ADC to a referred value after the automatic range selection circuit has stepped. R 74 and C 74 normally delay this process. The output of the ADC is thus available more rapidly and is synchronized with attenuator stepping. This avoids flickering in the display.

Up/down counter (IC 23, IC 24, IC 25, IC 27, IC 28):

The up/down counter consists of IC 23 and IC 24. These form a two decade counter with a range of 0 to 99. The gates IC 28/1 and IC 28/2 block the counting pulses in order to prevent the counter from overflowing. The counter counts up to 99 and stops or counts down to 0 and stops. R 111 and C 50 delay the counter pulse to ensure that it is always preceded by the switching pulse for upward or downward counting.
The inverter IC 26/5, together with R 109 and C 49, sets the counter to 0 before a new counting operation is initiated.

The gates IC 27/3, IC 27/4 and IC 25/3 are activated when the state of IC 23 is 0. This occurs if the input level is below -70 dBm and the frequency display is disabled.

The remaining gates and inverters of IC 25 to IC 27 decode the output signals of the counter IC 23 in order to switch the 10, 20 and 40 dB attenuators in a specific sequence. In order to optimize the signal-to-noise ratio, the 20 dB attenuator which is farthest from the input is connected into the circuit first. This ensures that the noise of the input amplifier is attenuated as much as possible.

The counter IC 24 drives the 1 dB attenuator directly.

The 8 BCD outputs of the two up/down counters are connected to the computer section in order to calculate the level display.

The straps l-b and c-d permit interruption of the counting pulses and the up/down signal for testing purposes.

9.4 C O M P U T E R S E C T I O N (14)

The digital signal processing of the PMG-3 is carried out in the computer section. This generates the level display information and contains most of the circuits for the frequency display. The battery voltage monitoring circuit is also part of this assembly.

9.4.1 FREQUENCY COUNTER

The frequency counter is a flicker-free, 4 1/2 digit LCD display with selectable resolution. The level display is driven by the frequency counter and processes all levels above -70 dBm in the measuring mode "Level" and "Sound-programme"; otherwise, the counter is disabled and zero appears in all digits of the display.

A resolution of 1 Hz or 10 Hz can be selected with the aid of switch [2] on the front panel. The input signal, which is normalized by the automatic range switching circuit, is connected to limiter IC 1/1, which generates a square wave signal with an amplitude of 13 V_p from this signal. This square wave signal is then connected to a phase-controlled 1:10 frequency multiplier. IC 2 contains a phase meter and a V.C.O. IC 3 divides the output frequency by 10, which means that the V.C.O. has to run at 10 times the input frequency in order to lock the phase locked loop.

Transistor T 1 replaces the frequency-determining resistor of the V.C.O. This makes it possible to increase the sensitivity of the V.C.O., permitting it to cover a wide frequency range without an excessively large control voltage. This V.C.O covers a range greater than four decades.

This signal, which is 10 times the frequency of the output signal, passes through a switchable frequency doubler IC 10. The final result is a sequence of pulses with 10 or 20 times the input signal frequency. The reason for this multiplication of the measured frequency is that it

permits the use of a shorter counter gate time and simultaneously ensures that the information is available faster. The gate time is 200 ms for a resolution of 1 Hz or 40 ms for a resolution of 10 Hz.

The multiplied frequency is connected to IC 29/2 which is the actual main counter gate. From here, the signal passes to the hysteresis counter. The task of this counter is to suppress flickering of the display which is seen in most counters because the measured signal is not synchronized with the time base (the gate pulses). The hysteresis counter is a 1:4 counter with gates which detect either zero or three. If a zero is detected, the counter is set to two before the next measurement. If these gates detect a three, they are reset to zero. The purpose of this circuit is to add or subtract counting pulses in order to prevent the hysteresis counter from overflowing, as this would result in flickering of the main counter between the measuring cycles.

Flipflop IC 30 is a 4:1 divider and the gates in IC 39 detect "zero" and "three". These gates are set by the "STORE" pulse (which also goes to the main counter) and set the RS flipflop IC 38/1, 2. IC 38/3, 4 are set by the "RESET" pulse (reset counter), which controls the actual resetting of the hysteresis counter. The hysteresis counter provides a digital hysteresis such that even small changes in the edges of the signal cannot cause changes in the display. As this circuit simultaneously executes 4:1 division, the gate time must be four times as long.

With a resolution of 1 Hz, this gate time would be 4 seconds. Due to the multiplication (x 20), the gate time is in fact only 200 ms. For a resolution of 10 Hz (x 10), the gate time must be 40 ms.

9.4.2 TIME BASE

The time base circuit receives its reference frequency from the frequency generator. This frequency is 1 kHz and is connected to binary counter IC 26. The binary outputs of this counter are processed by gates IC 27/1 and 2 to form the gate times 40 ms and 200 ms. Depending on the position of the switch "Resolution", only one of these two gates is enabled. In order to obtain a gate time of 200 ms, IC 27/1 combines the outputs 128, 64 and 8 ms. In order to obtain a gate time of 40 ms, IC 27/2 combines the outputs 32 and 8 ms. IC 29/1 is an "Or" gate for these two outputs and generates the actual gate pulse. At the end of the gate time, IC 26 is reset by the D flipflop (IC 36/1) after 1 ms and starts a new measuring cycle. As the "dead time" is only 1 ms, the time for displaying a new result is very short. During this 1 ms, the $\overline{\text{"STORE"}}$ and $\overline{\text{"RESET"}}$ pulses are generated by gates IC 17/1 and 17/2. The $\overline{\text{"STORE"}}$ and $\overline{\text{"RESET"}}$ pulses are required by the main counter, the hysteresis counter, the overflow counter IC 28 and the overflow buffer IC 36/2.

The main counter outputs (a 4 1/2 decade LSI circuit on the display section) generate a carry pulse when the counter has counted to 10,000 and 20,000. The carry counter IC 28 switches to the state "H" after the second carry pulse, resulting in the "Out of range" state when the counter reaches 20,000. During the measuring time, the D flipflop IC 36/2 stores the "Out of range" signal. The "Out of range" signal from IC 28, which is not stored, disables the main counter, causing the last four decades to display zero. The stored "Out of range" signal initiates a 1 Hz clock pulse which is generated by IC 37 and causes the "1" and "Out of range" arrows to blink alternately via the exclusive-or gates IC 41/1 and 2. This is the "Out of range" indication. The clock from IC 37 is the switching frequency for the LCD display (back plane), which is generated by the main counter module. The exclusive-or gates IC 41/3 and 4 switch the decimal points.

There are two further conditions which disable the counter. If the operating mode "Noise" is selected, IC 29/4 generates a disable signal. The hysteresis counter IC 30 is then disabled if the input signal is $\leq$ -70 dBm.

If a resolution of 1 Hz is selected and the input frequency is then greater than 110 kHz, the comparator IC 1/2 switches the x 20 multiplier to x 10. This ensures that the maximum frequency of the hysteresis counter is not exceeded.

9.4.3 ANALOG/DIGITAL COUNTER

The A/D counter also includes a hysteresis counter which is identical to that in the frequency counter. As the A/D counter must execute 10 counting operations per 10 ms, it must receive a clock frequency of 1 kHz. For this reason, a 4 kHz clock is connected to the hysteresis counter via the A/D counter gate IC 32/1. The gate pulse comes from the automatic range selection circuit. At the end of the gate pulse, counter IC 21 is enabled and starts counting the 4 kHz clock pulses. When the counter reaches the value 2, it generates a "Sample pulse" (which is used for the hysteresis counter and for the sender section).

When the counter reaches the value of 4, it generates a "RESET" pulse (which is required for the hysteresis counter and the A/D counter IC 35).

The A/D counter normally terminates an A/D cycle by counting from 0 to 19. If no new A/D cycle starts, the A/D counter continues counting past this range. When it reaches the value of 80, the counter generates a pulse which again initiates A/D conversion in order to maintain the A/D cycle.

During an A/D cycle, IC 45 stores 6 bits of the counter information. The four low order bits of the memory output are the 0.1 dB value and the two other bits are added via adder IC 33 to the information of the 1 dB attenuator. The carry output of this adder is then added in IC 33 to the 10 dB attenuator information. IC 33, IC 34 and IC 45 thus generate the sum of the attenuator information and A/D result in the form of 3 1/2 BCD positions.

9.4.4 GENERATION OF LEVEL INFORMATION

The task of this circuit is to convert the information on the attenuator settings into a dBrN or dBm level and to display this level with the appropriate sign. The attenuator information can vary between 0.0 and 100.0, and the display must lie between approximately -80.0 and +19.9 in the measuring modes level and sound-programme. When the display passes through zero, the counting operation must be reversed. This is done by changing the algorithm. In the operating mode "Noise", the display is equal to the attenuator information. This means that no correction is necessary and the information is passed without change to the LCD decoder drivers. In the measuring mode "Noise to ground", correction is necessary (due to the 40 dB attenuator for noise to ground measurements). This correction is accordingly 40 dB. This value is added to the attenuator information, which means that the final "Noise to ground" display lies between 40 and approximately 140 dBrN. It should be noted that the unit is displayed only in the positive direction in the operating mode "Noise" and that it is also possible for the display to reach 100 dBrN or larger in the operating mode "Noise to ground" (NTG). In all other operating modes, the 100 dB position is disabled.

In the operating mode "Level" and "Sound-programme", the algorithm is as follows:

If the input level is $\geq$ 0 dBm, the correction value is subtracted from the attenuator information. If the input level is below 0 dBm, the attenuator information is subtracted from the correction value. The correction value is 80. This makes it clear that the direction of the display is reversed when the level passes through 0 dBm. This also applies if the display is less than 0 dBm. The minus sign is then displayed.

Detection of the 0 dBm point is carried out with the value of the "80" bit of the attenuator information. If the input level is 0.0 dBm or higher, the attenuator information is $\geq$ 80.0. The correction value of 80 is subtracted from the attenuator information. This is done by adding 20 and removing the 100 dB bit (half digit), resulting in 0.0. This method naturally only works for levels $\geq$ 0.0 dBm. This is also the range which is used. The complementary control pin 5 of IC 23, IC 24 and IC 25 is "Low", which means that no complement is formed. The attenuator information is passed directly. The value 20 is added in IC 13.

For levels < 0 dBm, the attenuator information is converted to the complement form by IC 23, IC 24 and IC 25. IC 13, IC 14 and IC 15 then add 80.1 to this value. 80.1 is used instead of 80.0, as the circuit generates a nines complement. -0.0 becomes 0.9, which means that 0.1 must be added in order to again obtain 0.0. If, for example, the input level is -20 dB, then the attenuator information is 60.0. The complement of this value is 39.9. If 80.1 is now added to this complemented value, the result is 120.0. If the "1" is removed and the minus sign displayed, the actual display is then -20.0. To summarize, the correction factor is as follows:

Measuring mode "Level" or "Sound-programme": attenuator information -80 (input level $\geq$ 0 dBm)

Measuring mode "Level" or "Sound-programme": 80 - attenuator information (input level < 0 dBm)

Measuring mode "Noise": level display (dBrN) = attenuator information (no correction)

Measuring mode "Noise to ground": level display (dBrN) = attenuator information + 40

Gates IC 12/3 and IC 12/4 control the two and eight bits which are added in IC 13. The four bit input of IC 13 becomes "1" if the operating mode "Noise to ground" is selected. Generation of the complement is activated by the eight bit output of IC 33 via IC 4/1 and IC 12/1. The 0.1 bit is handled by the connection between the carry input of IC 15 and the complement control. Gates IC 12/3, IC 12/4 and inverter IC 11/4 enable the two or eight bit input to IC 13 only in the operating mode "Level" or "Sound-programme". Otherwise, these two bits are set to zero.

The information for the level display coming from adders IC 13, IC 14 and IC 15 passes to the LCD buffer decoder drivers IC 6, IC 7 and IC 8. The outputs of these drivers are connected via a 40 pole flat cable to the display unit. At the end of the A/D cycle, the buffers accept the new information with the aid of the STROBE pulse. The blanking inputs are activated only if the level lies outside the range. The signal "Out of range" is activated by the "Carry output" of the attenuator adder IC 33, which becomes "1" if the attenuator information exceeds 99.9. This corresponds, in the measuring modes "Level" or "Sound-programme", to +19.9 dBrN, in the operating mode "Noise" to 99.9 dBrN, and in the operating mode "Noise to ground" to +139.9 dBrN.

If the input level is out of the measuring range, the display is blanked and the minus sign starts to blink. The state "Out of range" enables flipflop IC 19/1, which passes the clock pulse for blinking of the minus sign via IC 4/2 and IC 4/3 to the LCD display. This clock pulse is generated by IC 37. The blanking signal is generated by IC 19/2, which can generate three different output states:

A "High" in the state "Out of range", a square wave signal if the battery charge is below the minimum value, or "Low" under all other conditions.

IC 16 and IC 9 observe the negative and positive supply voltages. The outputs are connected to the "Or" gate IC 20/2 in order to generate the signal "Insufficient battery charge". This signal permits IC 19/2 to change state and causes the complete level display to blink. This is not true for the operating state "Out of range", which always has priority over the indication "Insufficient battery charge".

The gates IC 4/2, IC 4/3 and IC 4/4 drive the minus sign and the 1/2 digit position of the display.

9.5 FREQUENCY GENERATOR (15)

The frequency generator consists of four subassemblies:

- The 1 MHz oscillator and the dividers
- The phase locked loop (PLL)
- The tuning counters and the pulse generator
- The mixer and the filters

The complete assembly forms a complete, tunable sinusoidal oscillator with a frequency range of 20 Hz to 20 kHz. It is an independent unit which requires only a negative and a positive supply voltage of 12-15 V DC. It also generates two clock signals - with fixed frequencies - for the computer section.

9.5.1 1 MHz OSCILLATOR AND DIVIDER

The 1 MHz oscillator contains crystal Q 1 as the frequency-determining element. Gate IC 1/1 forms the oscillator. Capacitor C 1 is used for fine tuning of the frequency. Gate IC 1/2 is an isolating stage. The decoupled 1 MHz frequency drives the 5:1 divider IC 2. The output of this divider is connected to a second 5:1 divider (IC 5), which provides two 40 kHz signals at its output: a square wave pulse and a composite pseudo-sinusoidal signal. The square wave pulse is used as a clock pulse, while the pseudo-sinusoidal signal acts as a source for the 40 kHz filter.

The 40 kHz clock signal is divided again by 1,000:1 in the two dividers IC 3 and IC 4, thus generating the 40 Hz reference pulses. The 40 kHz clock signal is also divided by 10 and 40 (IC 29/1 and 29/2), providing the two stabilized 4 kHz and 1 kHz clock outputs.

9.5.2 THE PHASE LOCKED LOOP (PLL)

The phase locked loop is the heart of the frequency generator. It generates a 40 to 60 kHz square signal from which the output frequency is derived. The frequency resolution of this output is 1 Hz.

The PLL IC 6 contains a voltage controlled oscillator (VCO) and a flank-triggered phase detector. IC 11 to IC 14 form the switchable 1:n divider. In this circuit, n covers a range from 40,000 to 60,000.

The VCO operates in a frequency range from 800 to 1,200 kHz. Its output is multiplied by two by IC 8, whose output drives the first divider IC 14. The output of the divider drives the phase regulation input (pin 3) of the phase detector IC 6. The 40 Hz clock pulse is connected to the reference input (pin 14) of IC 6. The VCO output also drives a 20:1 divider (IC 2 and IC 3) which generates the carrier frequency of 40 to 60 kHz.

The resistors R 7 and R 10 to R 13 and the capacitors C 9 to C 13 and C 50 form the loop filter. This filter is connected between the phase detector output (pin 13) and the VCO input (pin (pin 9). Its purpose is to filter out the variable duty cycle of the phase detector output in order to provide the VCO with a smoothed DC voltage. The monoflop IC 7 generates a current pulse into the filter when phase comparison occurs. The reason for this is to keep the phase detector pulse so wide that it lies outside the non-linear area (0° phase). This considerably reduces the phase noise and the jitter.

The principle of this phase locked loop is best explained with the aid of an example. If the synthesizer is set to the lowest frequency, the VCO oscillates at 800 kHz. After multiplication

by two, this frequency is divided by 40,000, resulting in a 40 Hz signal at the phase detector input. This input always remain at 40 Hz, as the phase detector tunes the VCO such that the loop is locked in a fixed phase. If the division ratio "n" changes, the VCO frequency also changes in order to maintain this phase lock. This makes it clear that the input frequency of the divider changes in steps of 40 Hz. The VCO frequency changes in steps of 20 Hz, as it is followed by a frequency doubler stage. As the VCO signal is divided by 20 in order to generate the carrier, its 20 Hz steps result in 1 Hz steps of the carrier. The frequency doubler permits the use of a 40 Hz reference frequency instead of a 20 Hz reference frequency, thus halving the regulation time.

9.5.3 TUNING COUNTER AND PULSE GENERATOR

The purpose of this assembly is to generate continuously variable, parallel BCD information for setting of the dividers in the phase locked loop. It can be operated at three different fixed frequencies, which are selected by the logic inputs of the assembly.

The up/down counter is used for changing, presetting and storing the required frequency data. The counters are driven by three basic lines: direction (up/down), speed (clock pulse) and preset. The preset lines are connected to the preset inputs of the counters and carry the information in BCD code. The enable input must be activated (set to "1") in order to set the fixed frequency. R 71 and C 45 select the center fixed frequency when power is switched on in order to prevent random frequencies when power is connected. The direction and clock pulse lines come from the tuning pulse generator. A tachometer (DC generator) charges the series connected capacitor C 42, C 43 when the tuning knob is turned. This charge is amplified by IC 26 and connected to the two D inputs of the flipflops IC 25. The polarity of this voltage depends on the direction in which the tachometer was turned. The polarity also determines which of the two flip-flops is enabled. The up/down flipflop IC 23/2 and IC 23/3 is set by the D flipflop in order to control and store the direction of counting. The gate IC 24/4 is an "OR" gate for the outputs of the two D flipflops and generates a clock pulse regardless of the direction. R 67 and C 39 provide a delay in order to ensure that the clock pulse always arrives after (and not during) a change of the counting direction. When one of the two D flipflops is enabled, it is also triggered by a 40 kHz clock pulse. When it is triggered once, the capacitor C 42 or C 43 is discharged via transistors T 1 and T 2, respectively, controlled by gates IC 24/1, 2 and 3. The faster the tuning knob is turned, the faster is the triggering sequence of the D flipflops. This means that the clock frequency increases with the speed of rotation. When a certain speed is reached, diode Gl 11 or Gl 12 conducts and R 54 is connected in parallel with R 55. This reduces the charging time constant by a factor of approximately 47 and provides extremely rapid tuning. This makes it unnecessary to fit an additional switch "Coarse/fine tuning". Gates IC 22/1, 2 and 3 form the "20,000" and "0" detection circuit in order to disconnect the clock pulses from the counters. This prevents the counters from counting downwards past 0 or upwards past 20,000. The 40,000 bit of the dividers is connected to "1". This permits a division range of 40,000 to 60,000 and thus an up/down counting range of the counters of 0 to 20,000.

9.5.4 MIXER AND FILTER

The task of the mixer is to convert the 40 to 60 kHz carrier into a sinusoidal baseband signal of 0 to 20 kHz. The filters remove unwanted spurious signals and images from the signals to and from the mixer.

The 40 kHz low-pass filter IC 9 and IC 10 shapes the 40 kHz pseudo-sinusoidal signal from IC 5 into a purely sinusoidal signal. R 18 determines the level of the sinusoidal signal and sets the baseband output signal to approximately -12.7 dB. The 40 kHz signal then passes to the mixer driver IC 20/1 and IC 20/2. IC 20/2 inverts the phase of the signal (by 180°). The two signals are connected to the mixer switch IC 21. This switch is a double switch which increases the switching balance. The 40 to 60 kHz carrier controls the first switch, which then controls the second switch. This second switch alternately connects the two 40 kHz signals from IC 20 and its output (pin 14) drives the output low-pass filter IC 27 and IC 28. This filter blocks the upper side band and other mixer products and allows the lower side band (0 to 20 kHz) to pass. Capacitors C 48 and C 49 block any DC components at the output of the filter. These DC components can occur if the synthesizer is set to 0 frequency. The filter has a limit frequency of 30 kHz.

The residual signal (40 kHz) is adjusted to minimum with the trimmer capacitor C 26 and the residual carrier is adjusted to a minimum level with P 32. (Due to its design and balance, the mixer suppresses both of these signals.)

The active filter circuit consisting of T 3 and C 55 blocks interference voltages on the positive supply voltage, and thus reduces audio frequency harmonic distortion.

9.6 D I S P L A Y U N I T (16)

The display unit includes all display elements and various control circuits. Two LCD displays are used for display of level and frequency. Most of the control elements control the sender. The sender can be tuned continuously in steps of 1 Hz. The pseudo-continuous tuning is carried out by a tachogenerator (see Section 9.5.3).

The send level adjustment is carried out with two potentiometers with concentric knobs. The larger knob is for coarse adjustment with a range of approximately 65 dB. The fine adjustment knob (smaller knob) permits adjustment of the send level in a range of approximately 2 dB.

The third potentiometer is used for adjustment of the loudspeaker volume and simultaneously acts as an "On/off" switch for the instrument. A small LED below this control lights when the instrument is connected to the AC supply. This display unit contains three further display elements: the level display, the dBm/dBrN indicator and the frequency display. The level display has 3 1/2 active digits. It is driven directly via a 40-core flat cable from the computer section.

The frequency display has 4 1/2 active decades and a symbol for "Out of range" (arrow pointing to the left). With a small slide switch, a resolution of 1 Hz or 10 Hz can be selected for the frequency display and the decimal point is shifted accordingly.

The frequency display is controlled by the LSI counter IC 1, which is installed directly behind the display unit. This IC contains all decade counters, buffer elements and display drivers for the digits.

The display unit is connected to the motherboard via a 26-core flat cable. This cable has a plug mounted on the display unit. The LCD display and the counter ICs are mounted on sockets for ease of replacement.

9.7 POWER SUPPLY UNIT (17)

The power supply unit supplies the instrument with three DC voltages: +5 V, +13.5 V ± 1.5 V and -13.5 V ± 1.5 V. The power supply unit takes its power either from the mains voltage or from the optional battery set. The power supply unit also contains an amplifier and a loudspeaker for AF monitoring purposes and the battery charger.

The AC mains voltage is connected to the instrument via a three-core cable.

A "CORCOM" filter at the input of the power supply unit contains a mains fuse, an interference filter and a voltage selector. One of two mains voltages can be selected: 120 or 220 V. The mains frequency range is 45 to 66 Hz. The mains voltage is connected directly to the mains transformer T 1, which means that the power supply unit is operating whenever the mains is connected. Mains voltage selection is carried out by selecting the appropriate combination of primary windings on the mains transformer T 1. The secondary side generates a voltage of 40 V with center tap to ground. The AC voltage is rectified by diodes Gl 1 to Gl 4. Capacitors C 1 and C 2 smooth the DC voltage. This DC voltage is connected to two points in the power supply unit: to the voltage regulator and to the battery charger.

The battery charger consists of diodes Gl 5 and Gl 7 and resistors R 1 and R 2. The diodes ensure that the batteries cannot be discharged via the power supply unit and the resistors limit the charging current to approximately 200 mA.

The voltage regulators are three-pole circuits with 15 V/1 A. Capacitors C 3 to C 6 provide decoupling for the regulators. Diodes Gl 6 and Gl 8 to Gl 10 permit the instrument to be operated either from the battery or from the regulators. Gl 9 and Gl 10 are Schottky diodes. These ensure that the voltage drop in the battery circuit is as small as possible. The Zener diodes Gl 11 and Gl 12 limit the battery voltage to 16 V and thus prevent overvoltages. The Zener diode Gl 13 stabilizes the +5 V supply. The resistor R 3 for the Zener diode and the AF amplifier are supplied with the positive voltage which comes from the motherboard via the main switch. The on/off switch switches the positive and negative supply voltages of the instrument. Resistor R 7 supplies the LED indicator on the front panel with current such that the LED lights whenever the mains supply is connected. If the mains supply is connected, the battery is also charged.

The AF amplifier consists of IC 3 and the related components. Its purpose is to amplify the normal AC signal to a level which is sufficient to drive the loudspeaker. The input impedance of the amplifier is high, which means that there is only a slight load on the volume control. Resistor R 5 and capacitor C 7 emphasize the low frequencies in order to improve the AF frequency response of the loudspeaker. Capacitor C 9 and resistor R 4 decouple the power supply unit in order to reduce feedback from the amplifier at low measuring levels. The remaining components are for frequency response compensation and loudspeaker connection.