

Dorado Printed Circuit Memory Storage Array

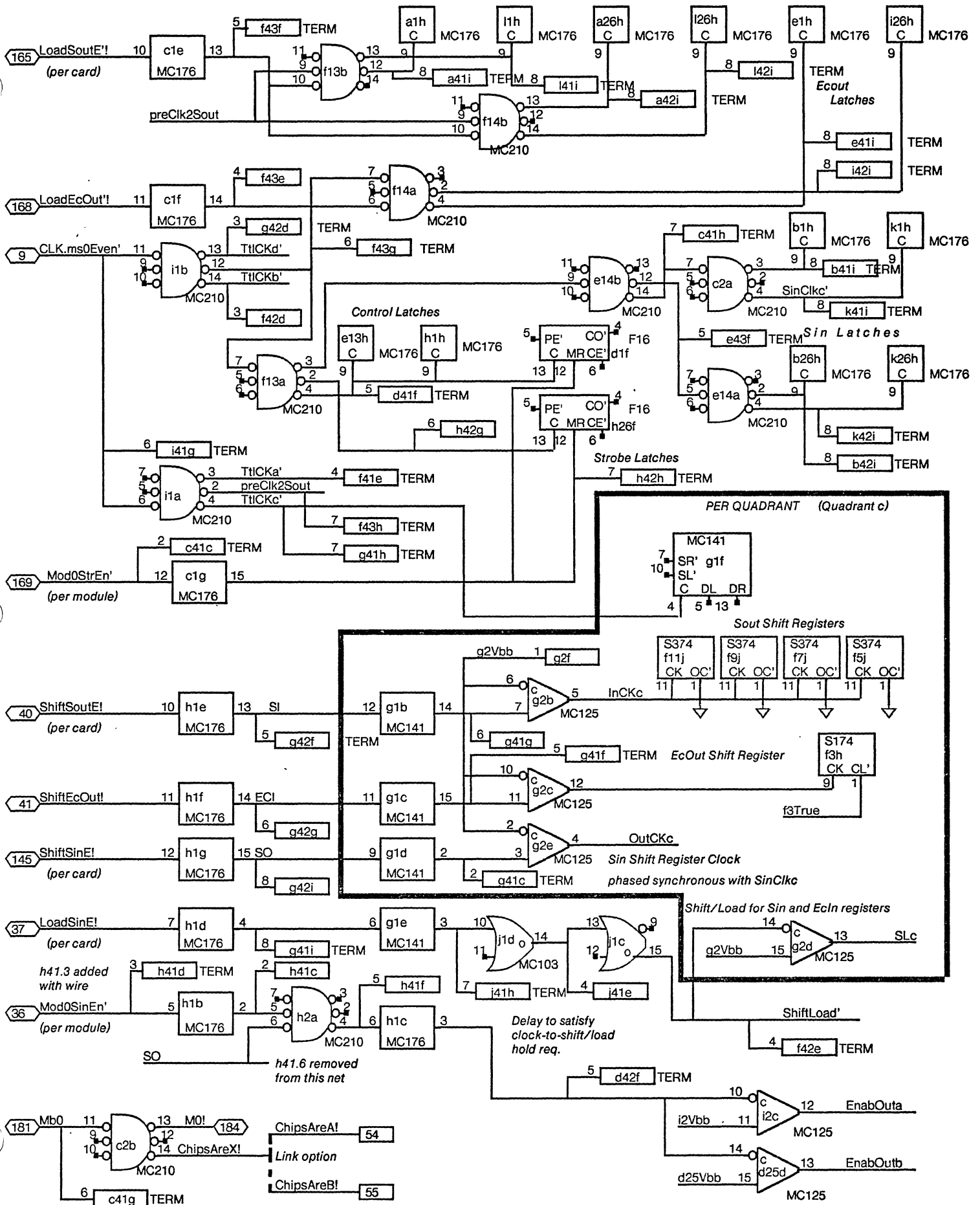
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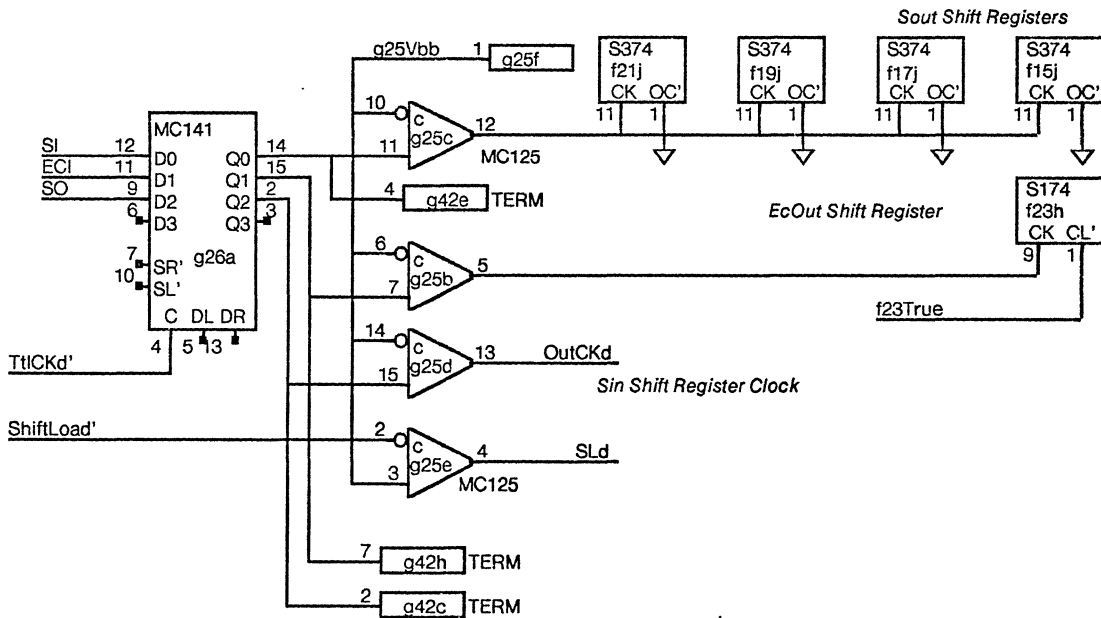
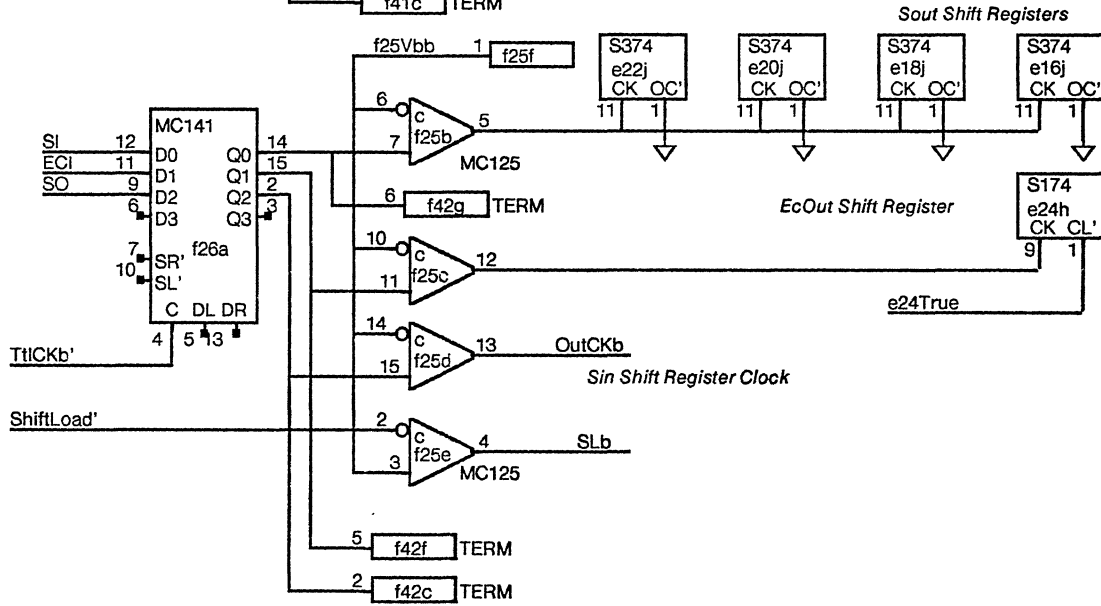
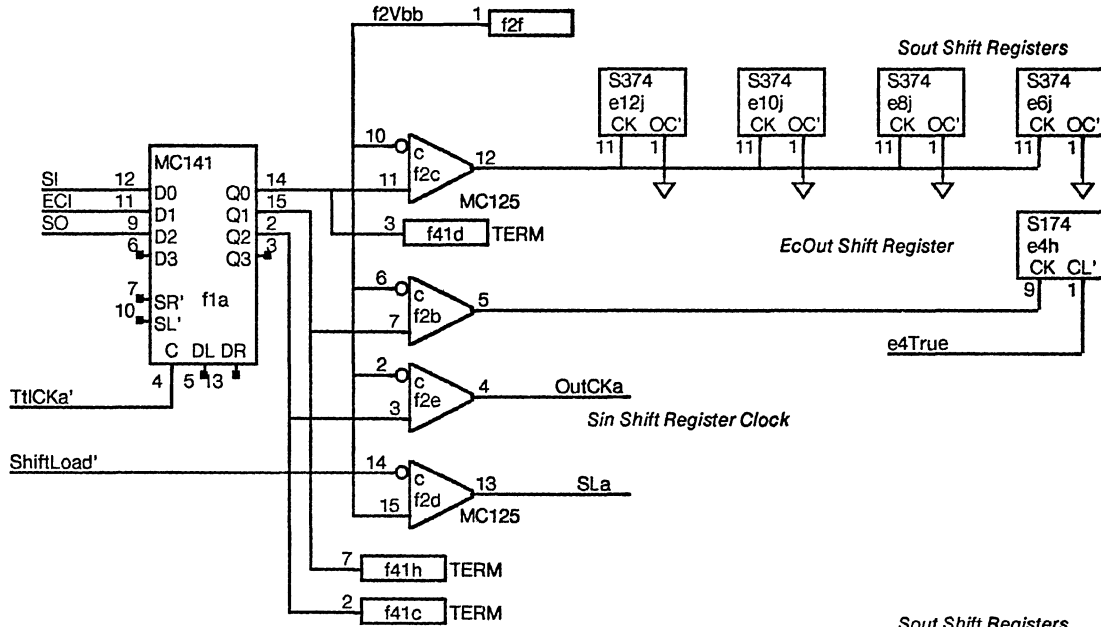
Control _____ 1
TTL Quadrant Clocking _____ 2
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Data Bit Paths _____ 4-11
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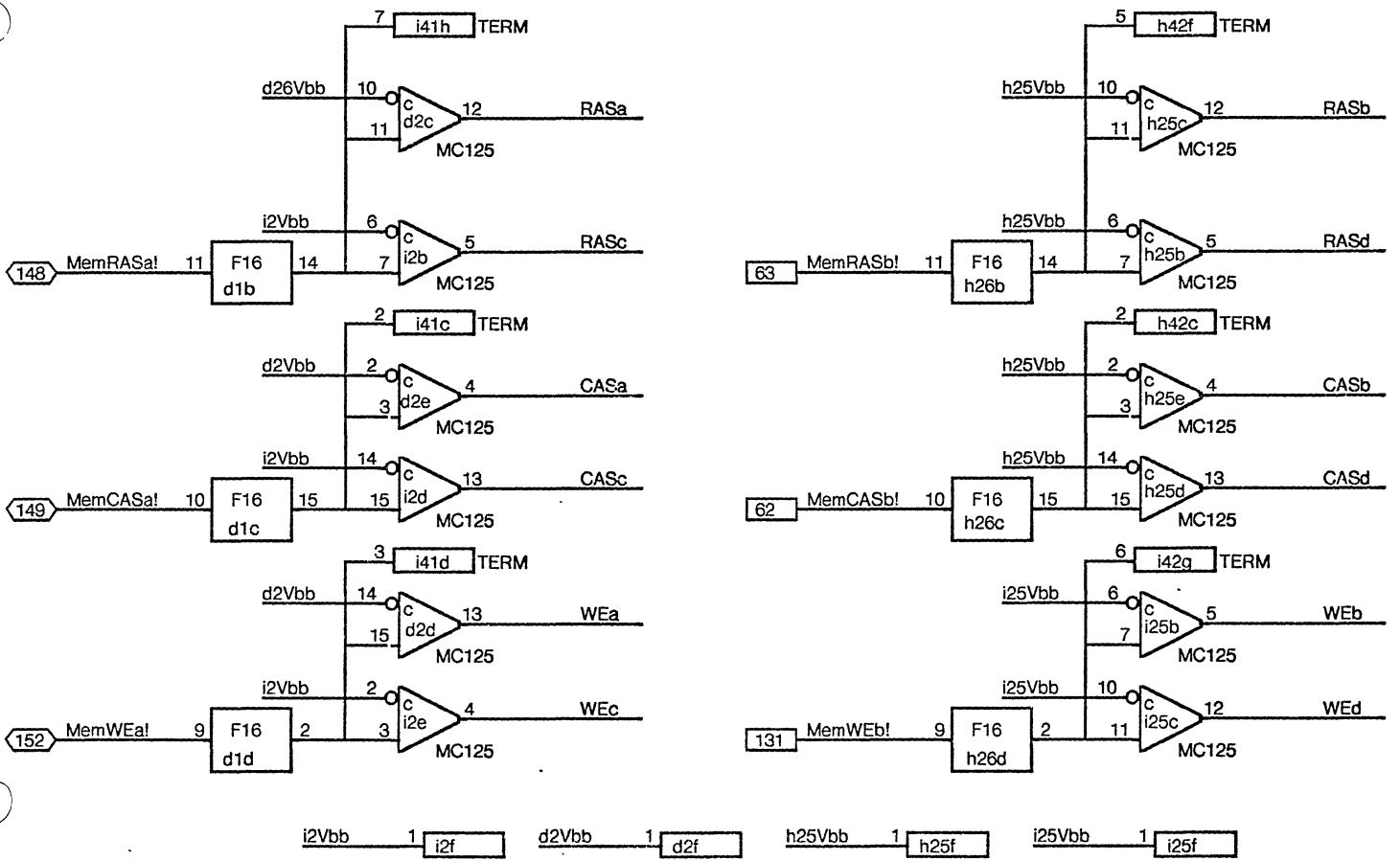
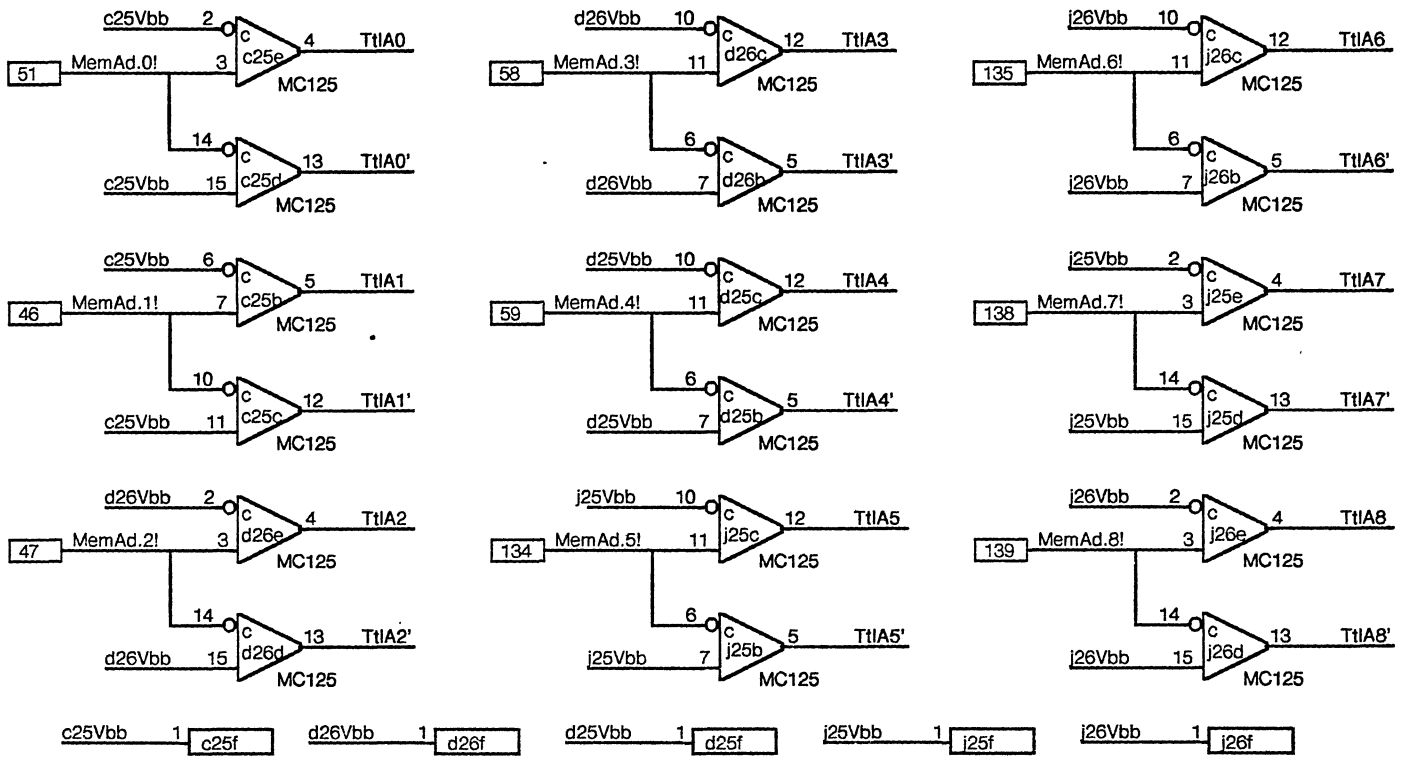
~~ODD~~ EVEN ADDRESSES ON BOTTOM BOARD
ODD ADDRESSES ON TOP BOARD

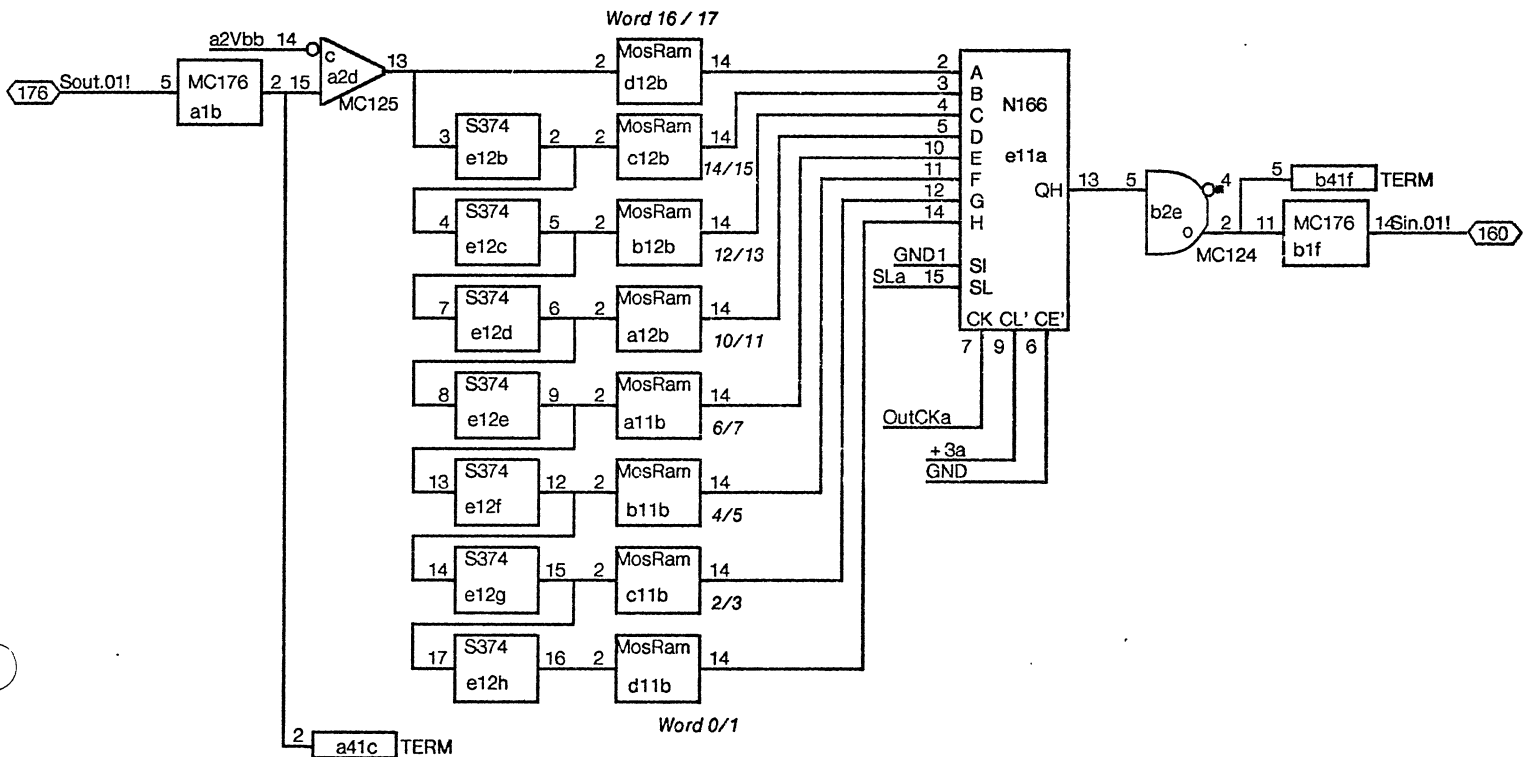
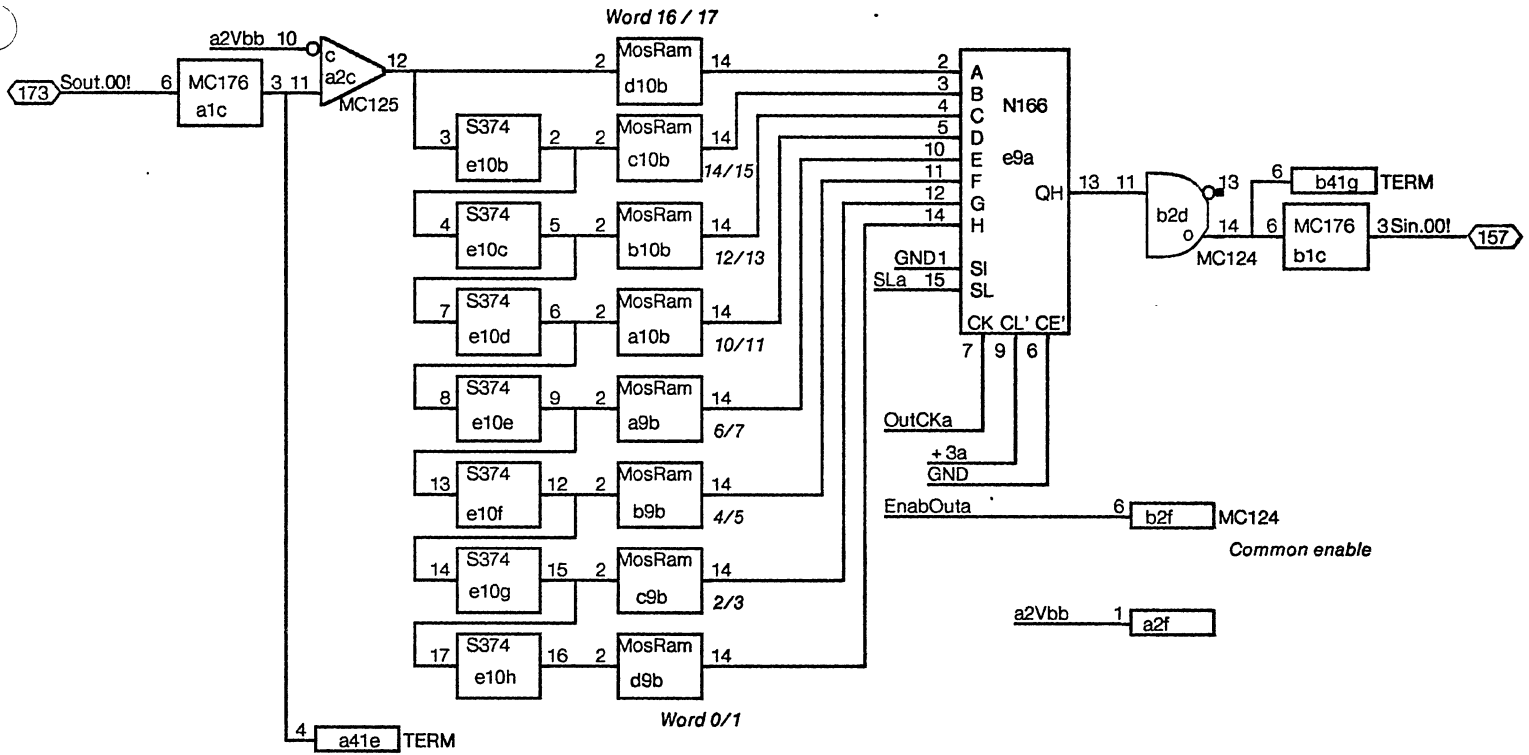
EC OUT 1+5 ON EVEN BOARD
EC OUT 3+7 ON ODD BOARD

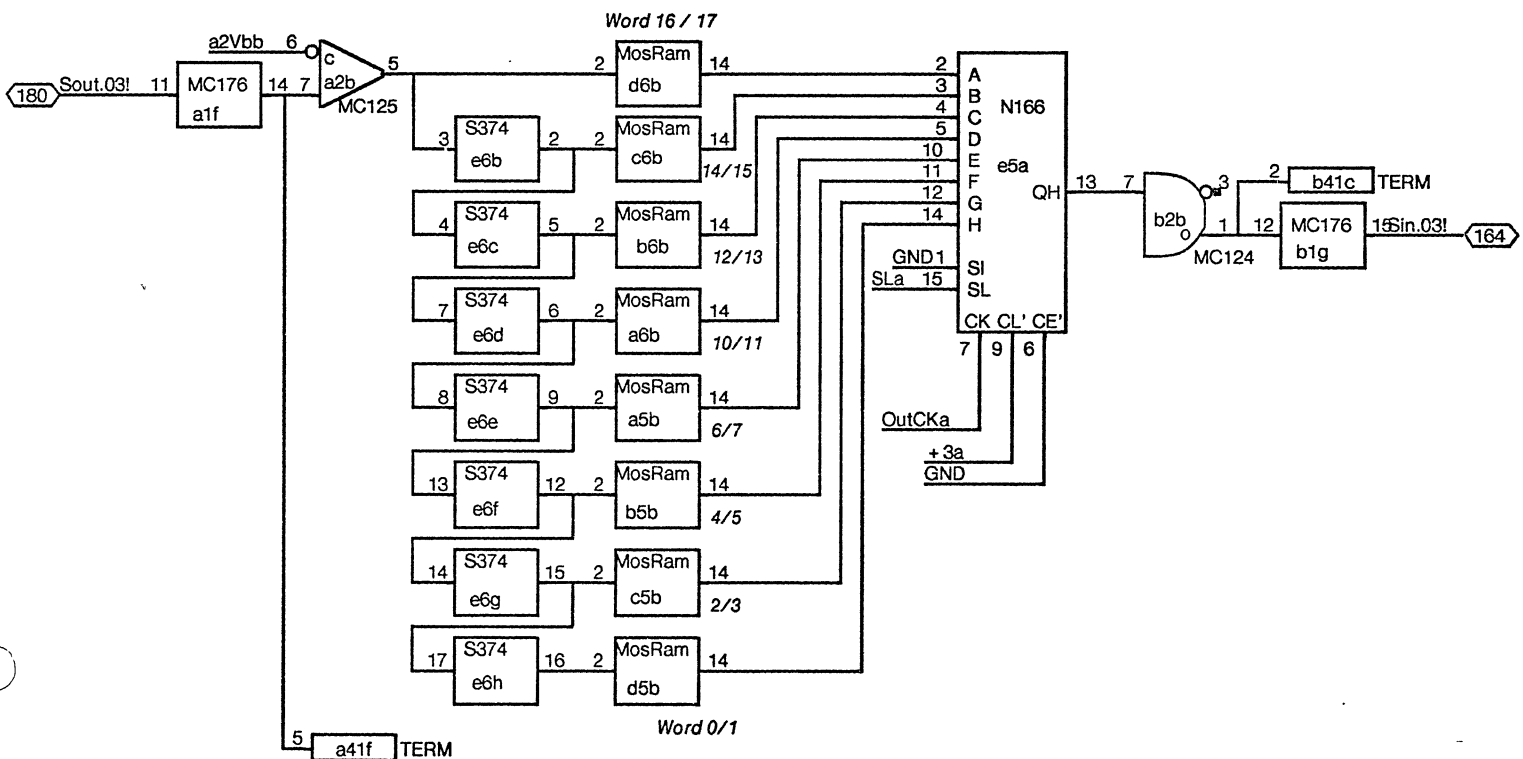
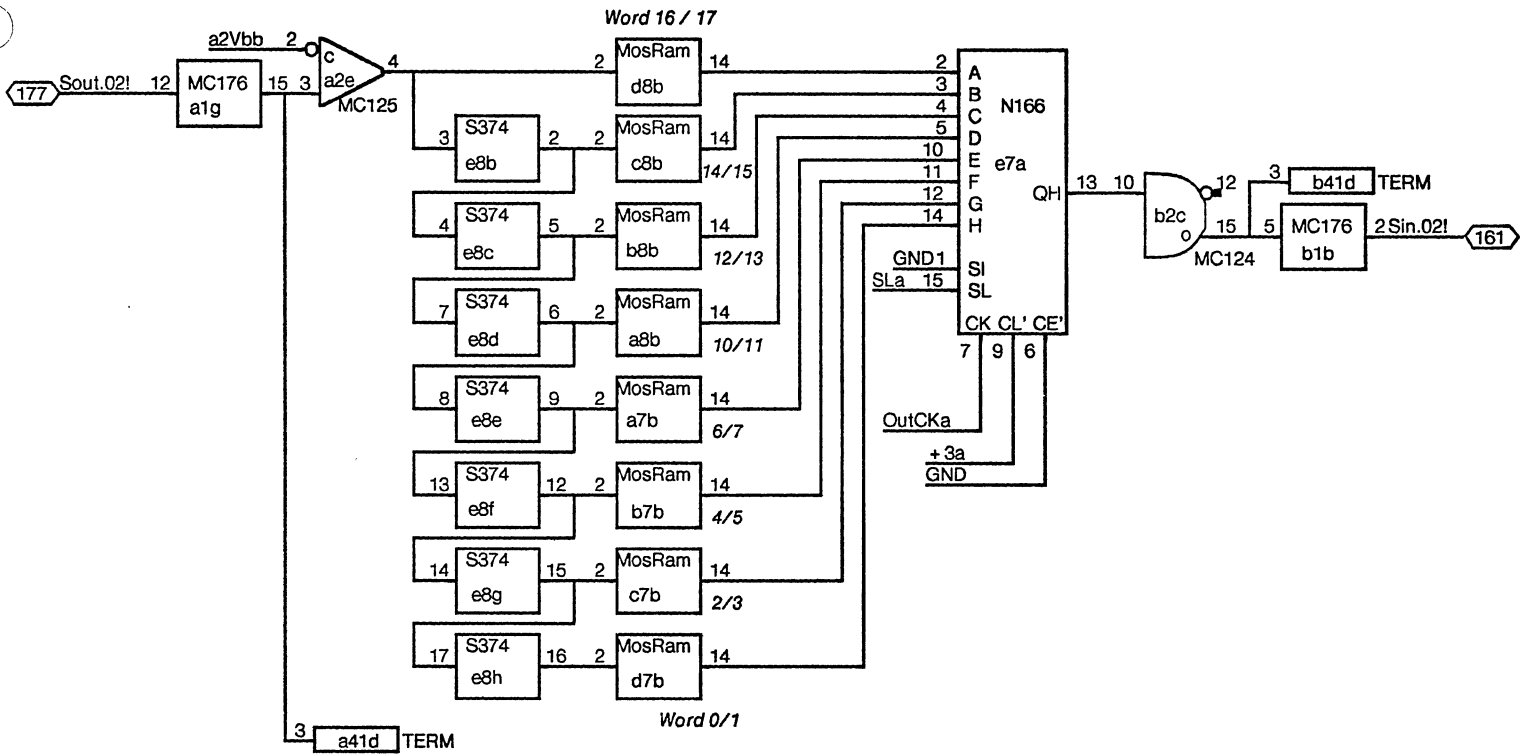
Sout Latches

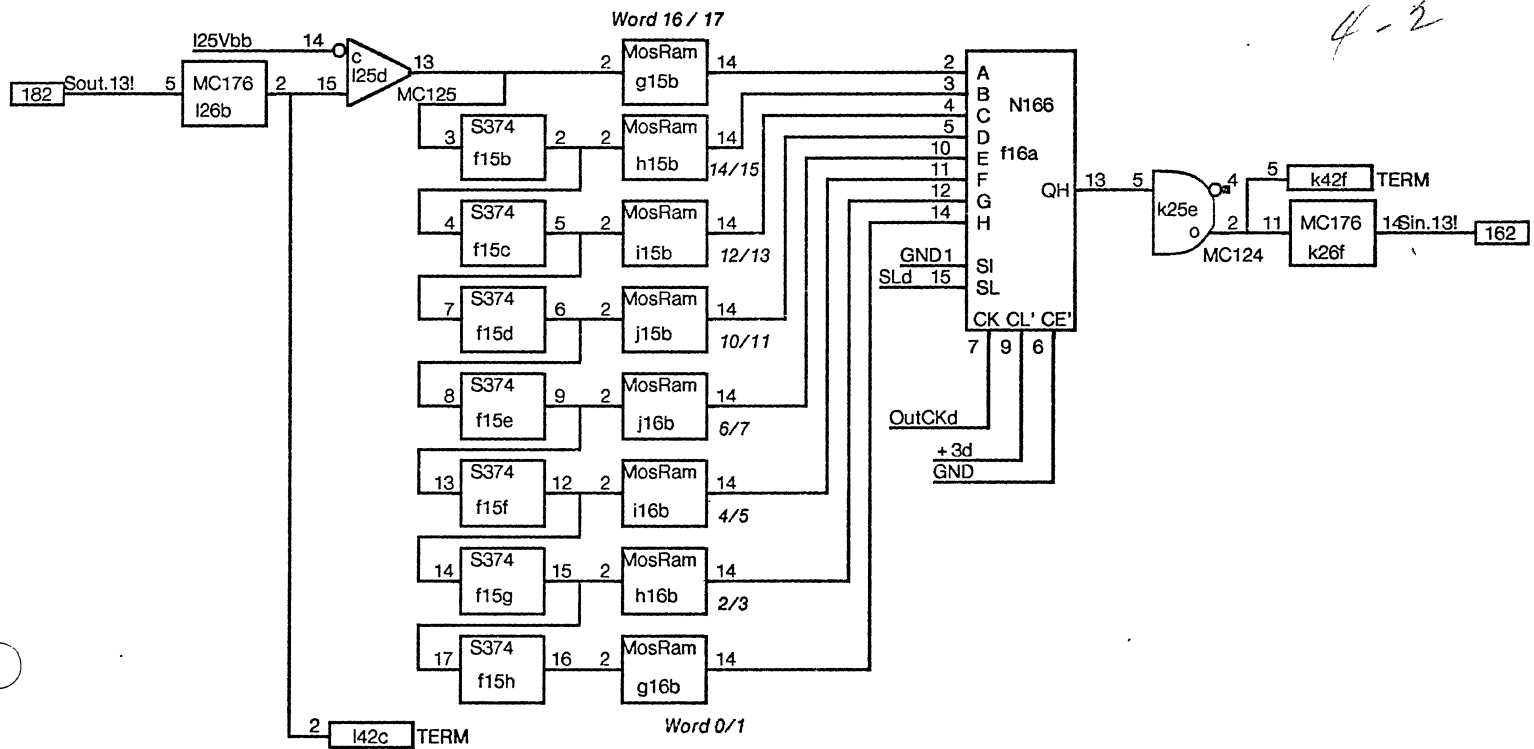
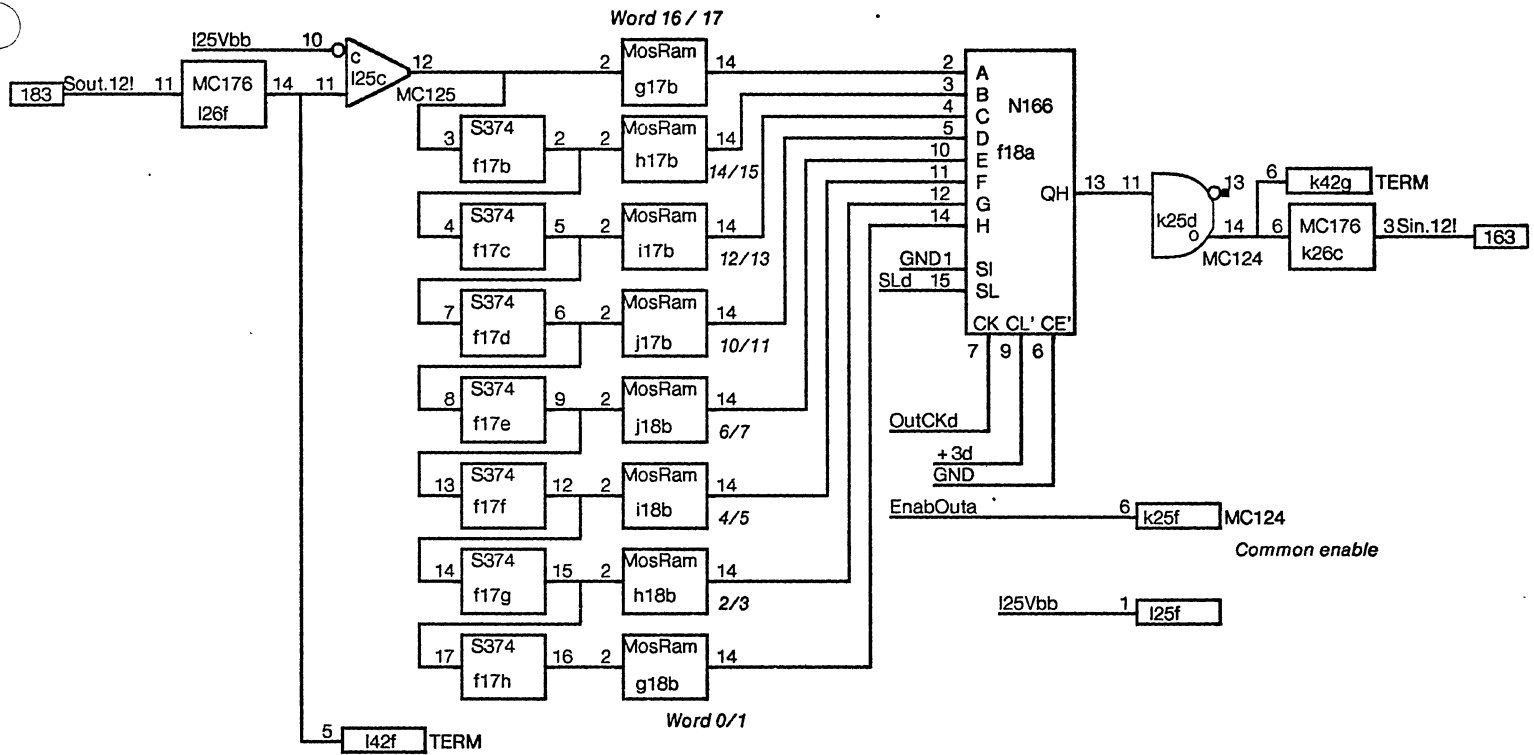




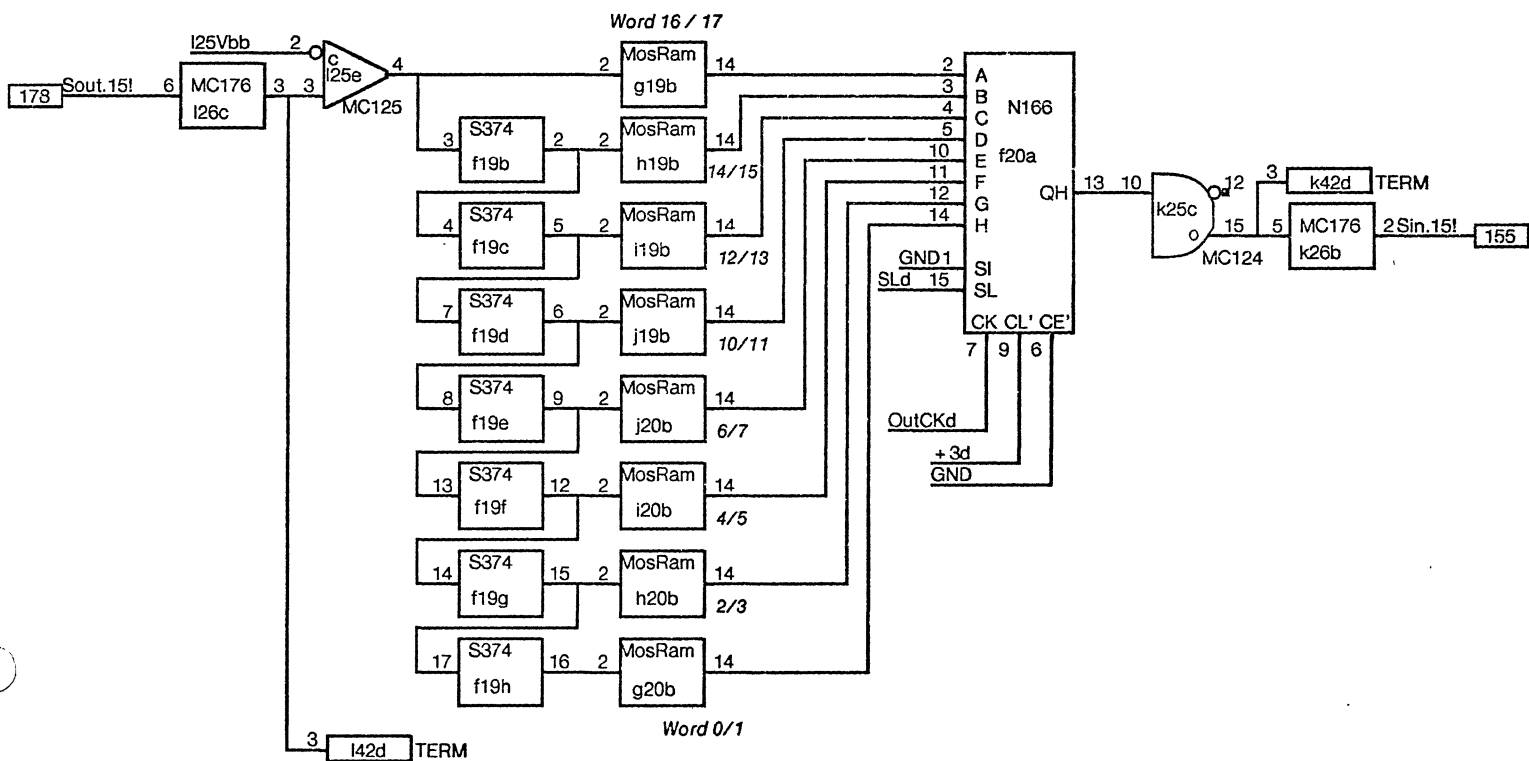
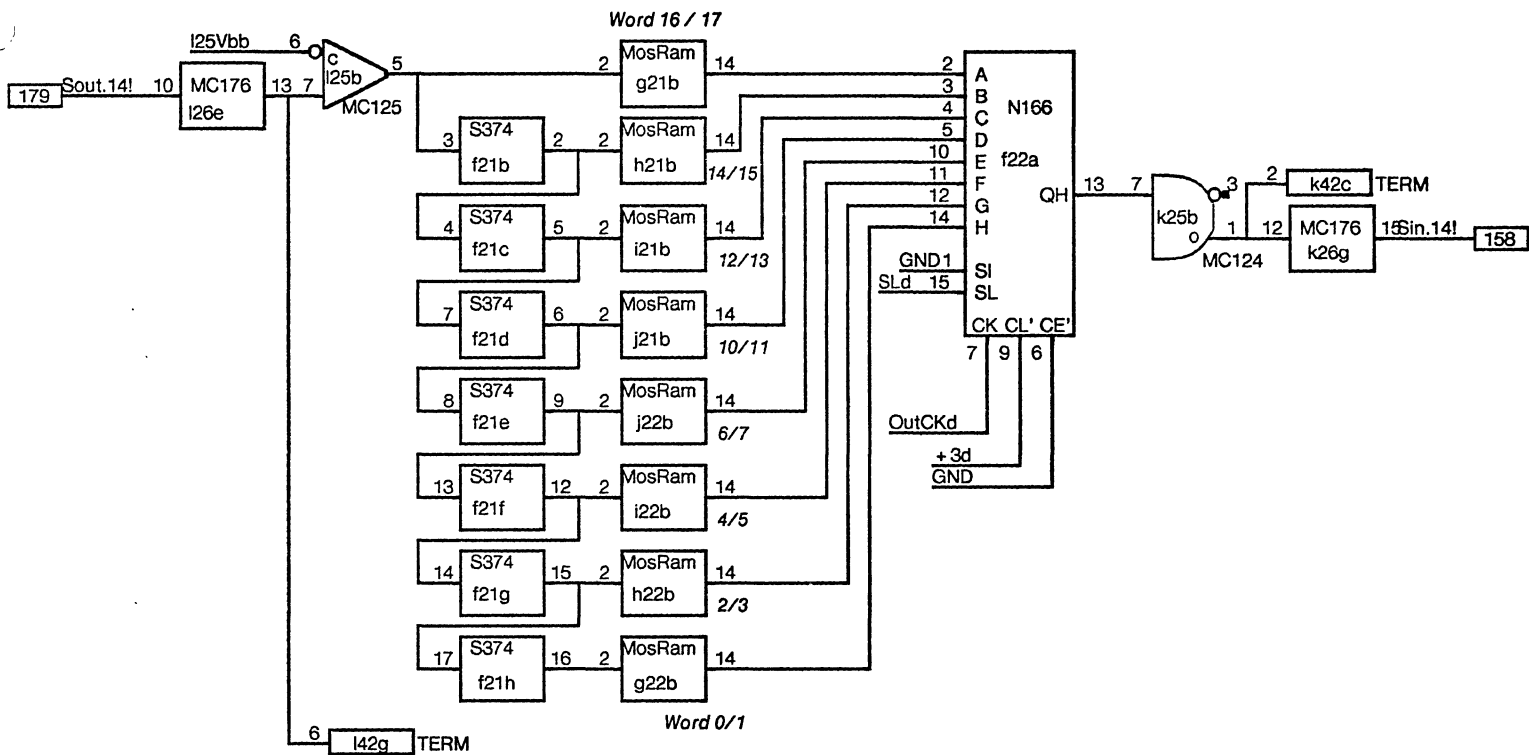


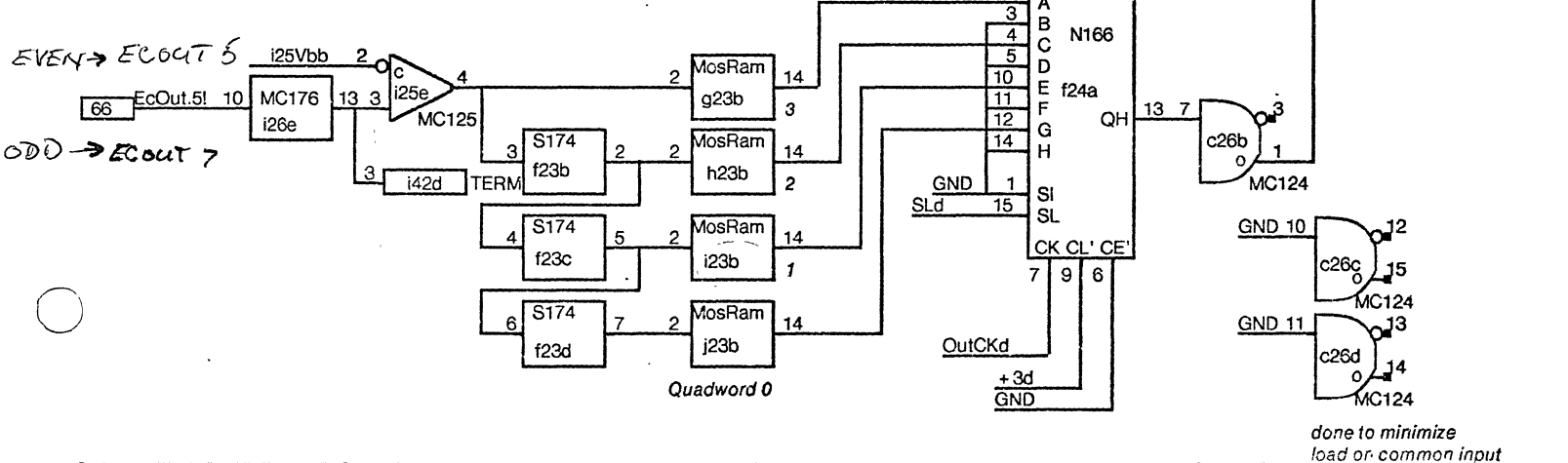
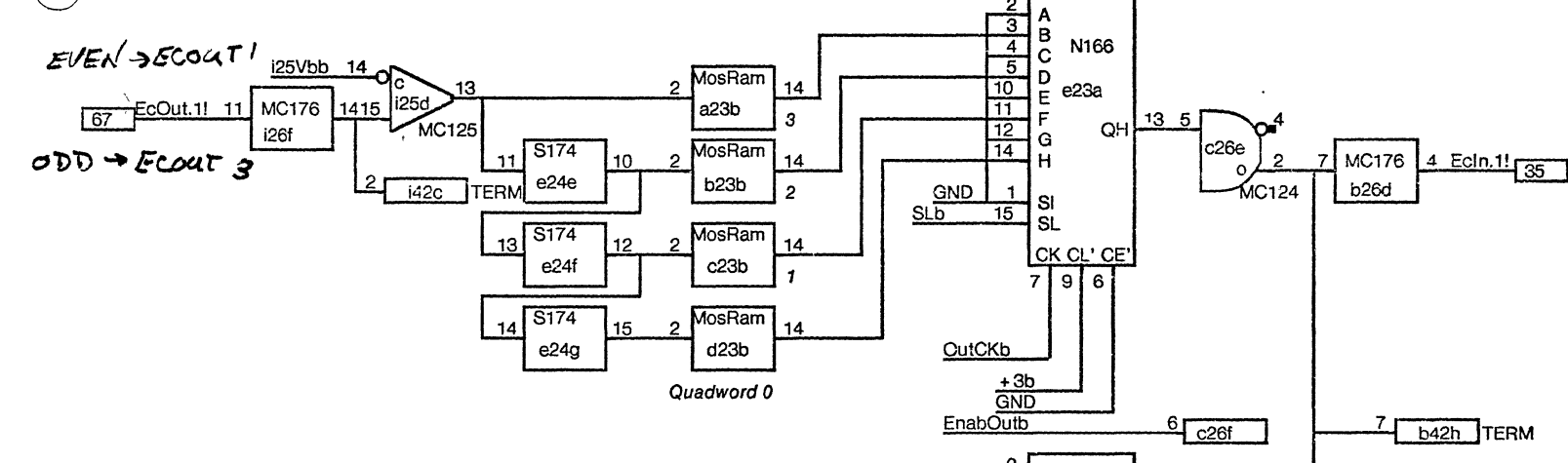
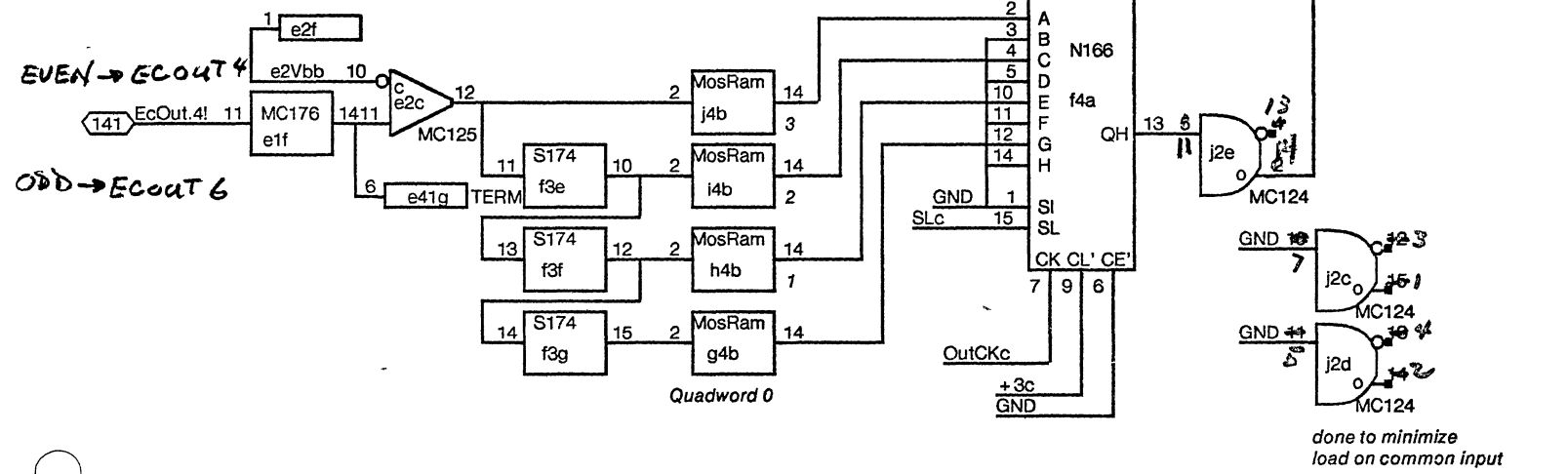
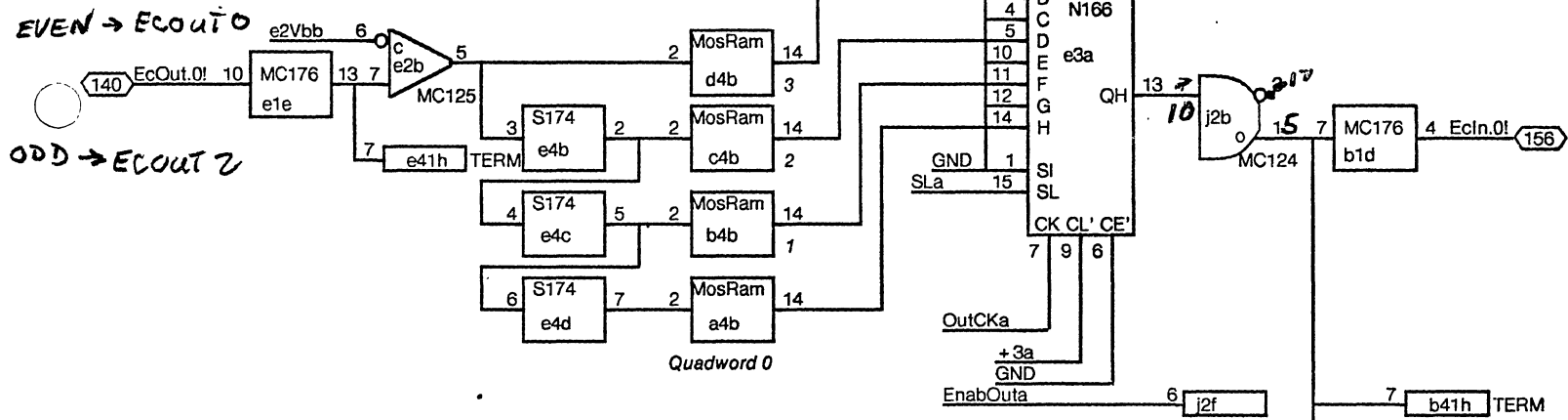


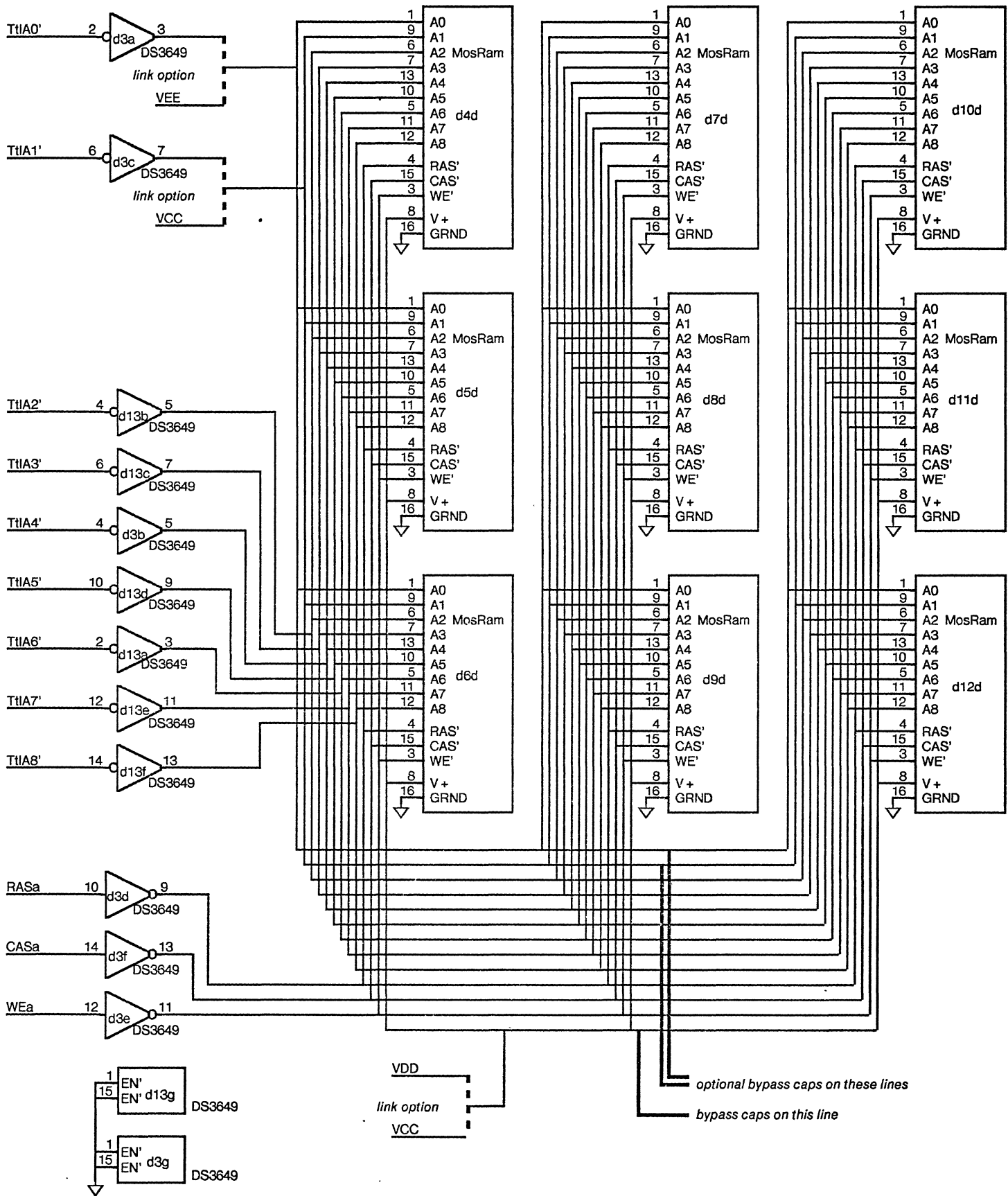


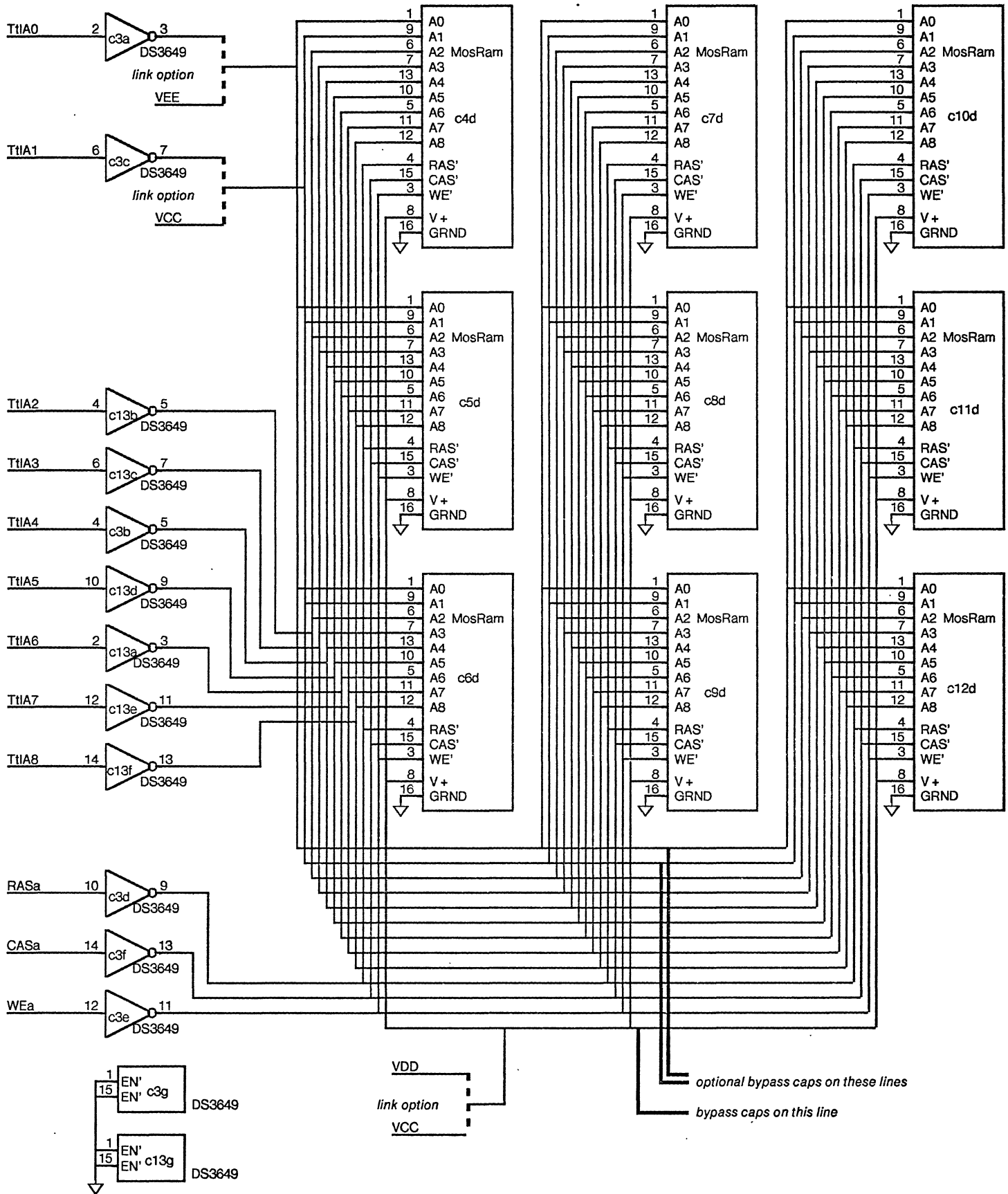


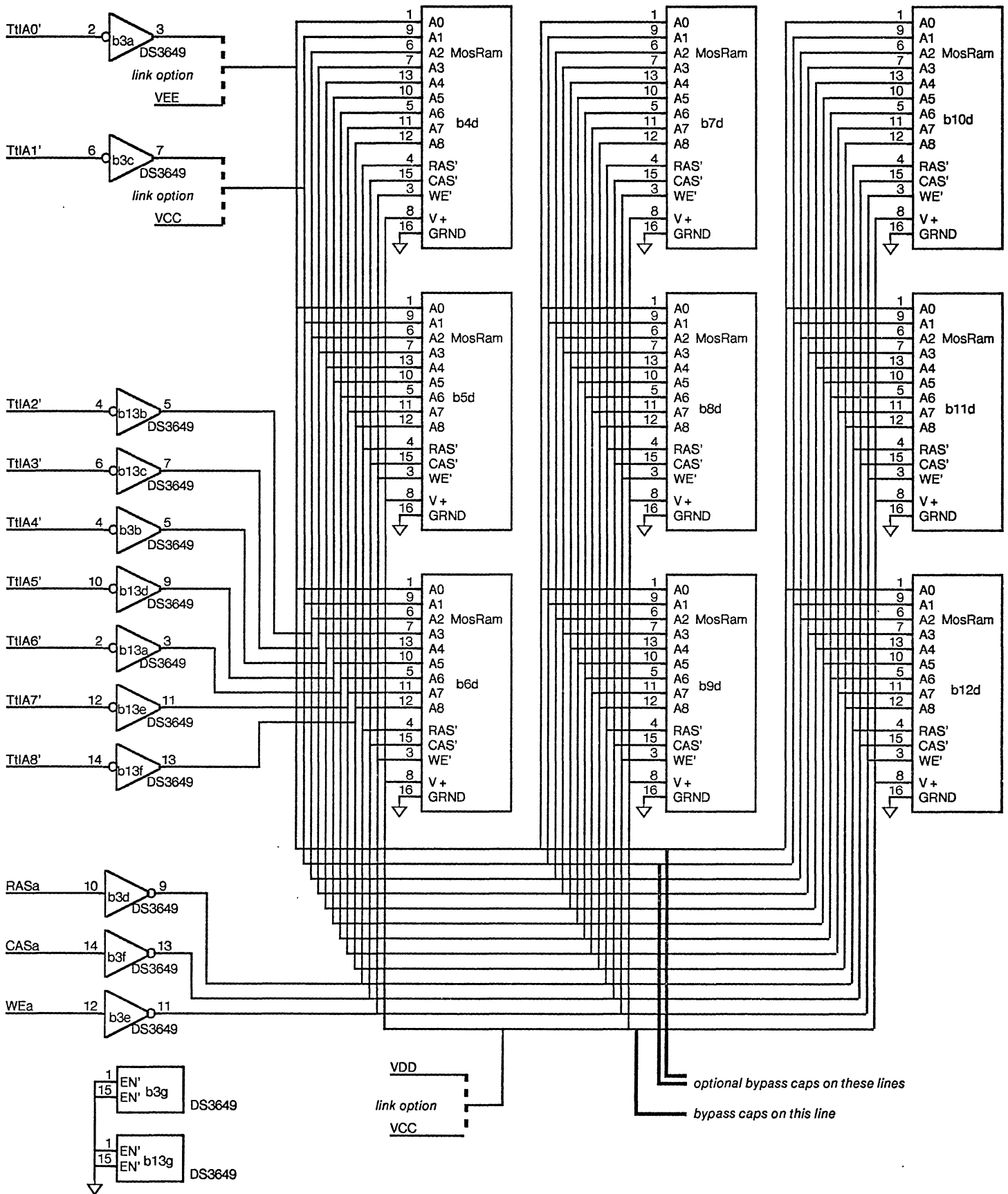
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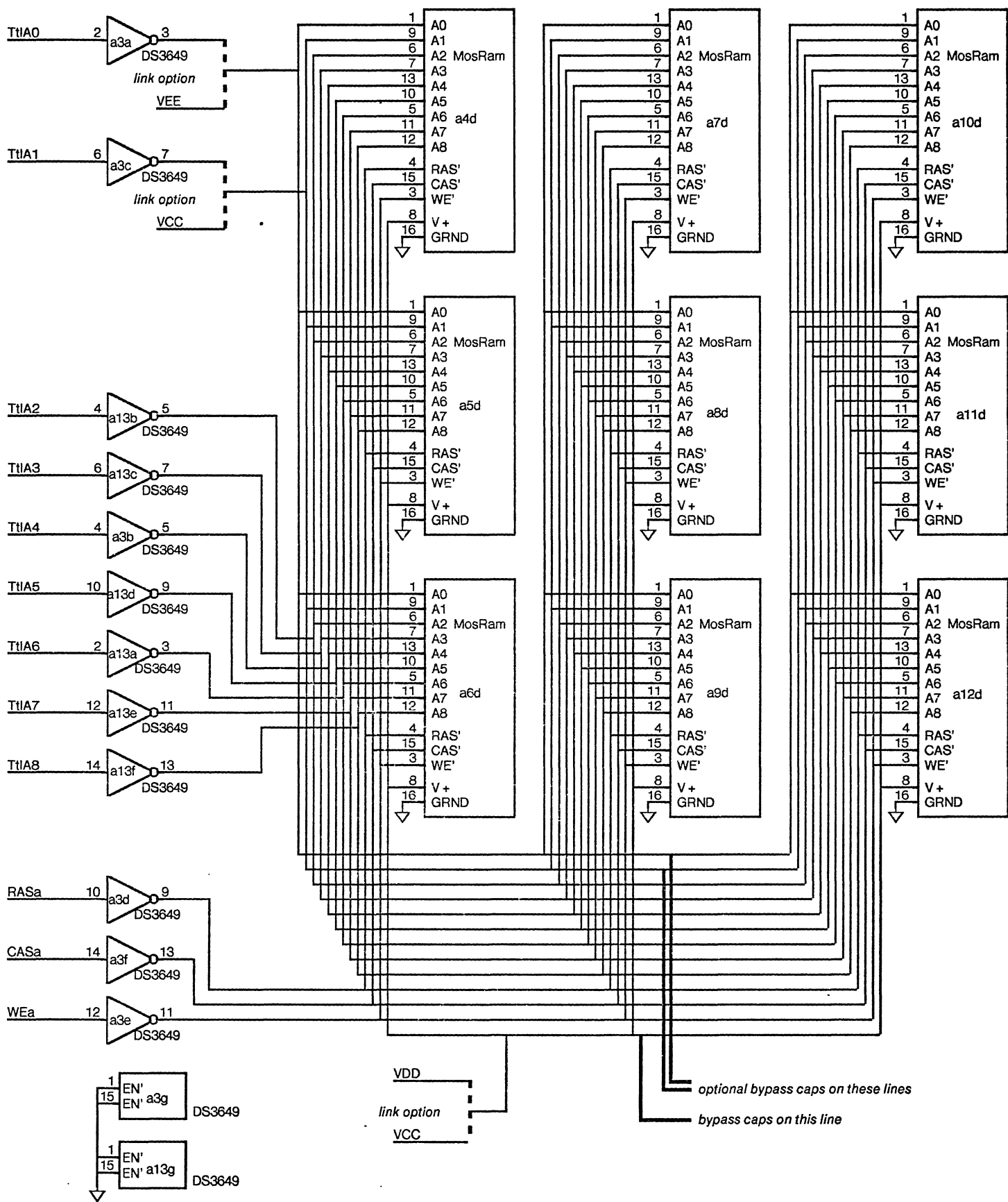


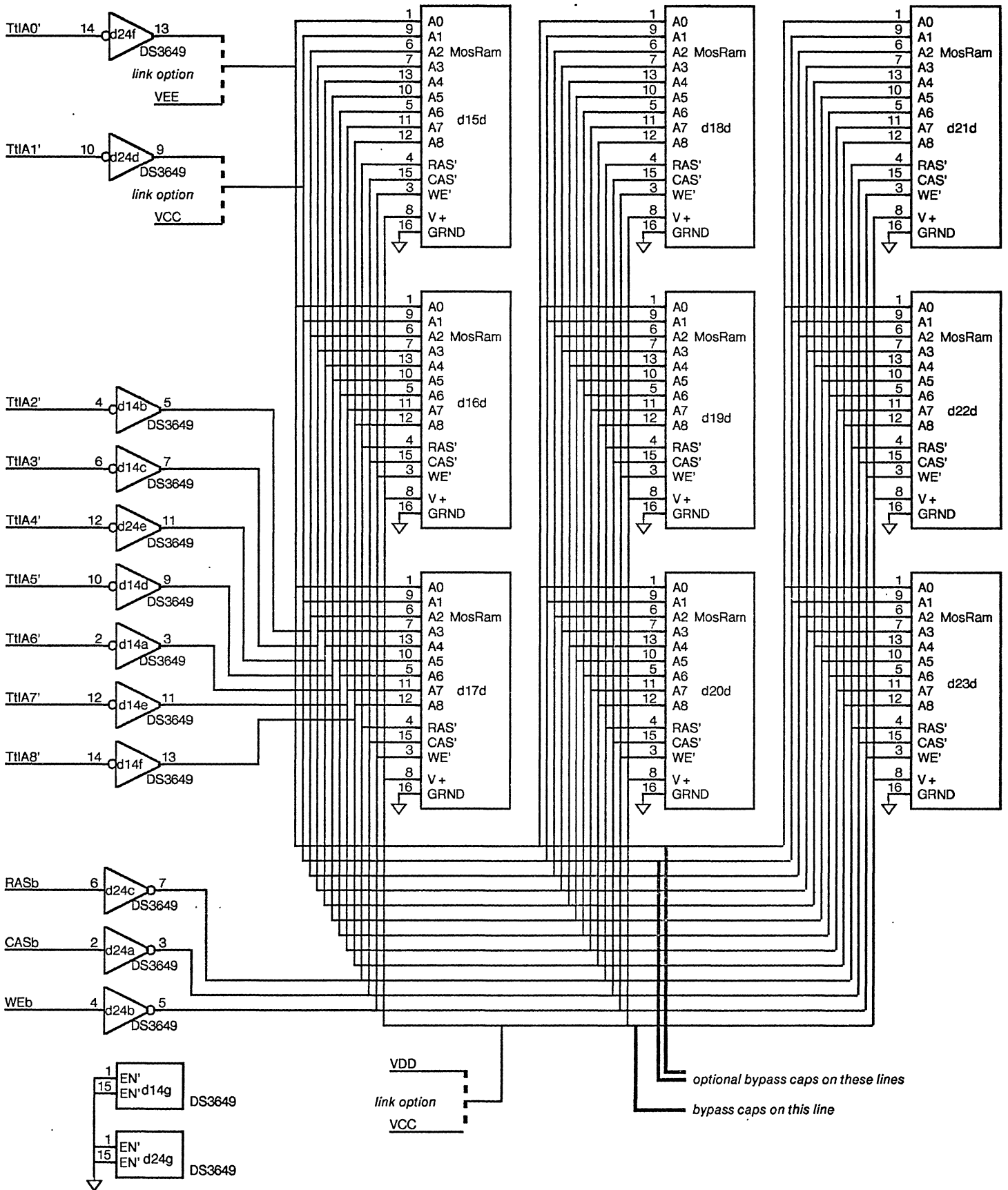


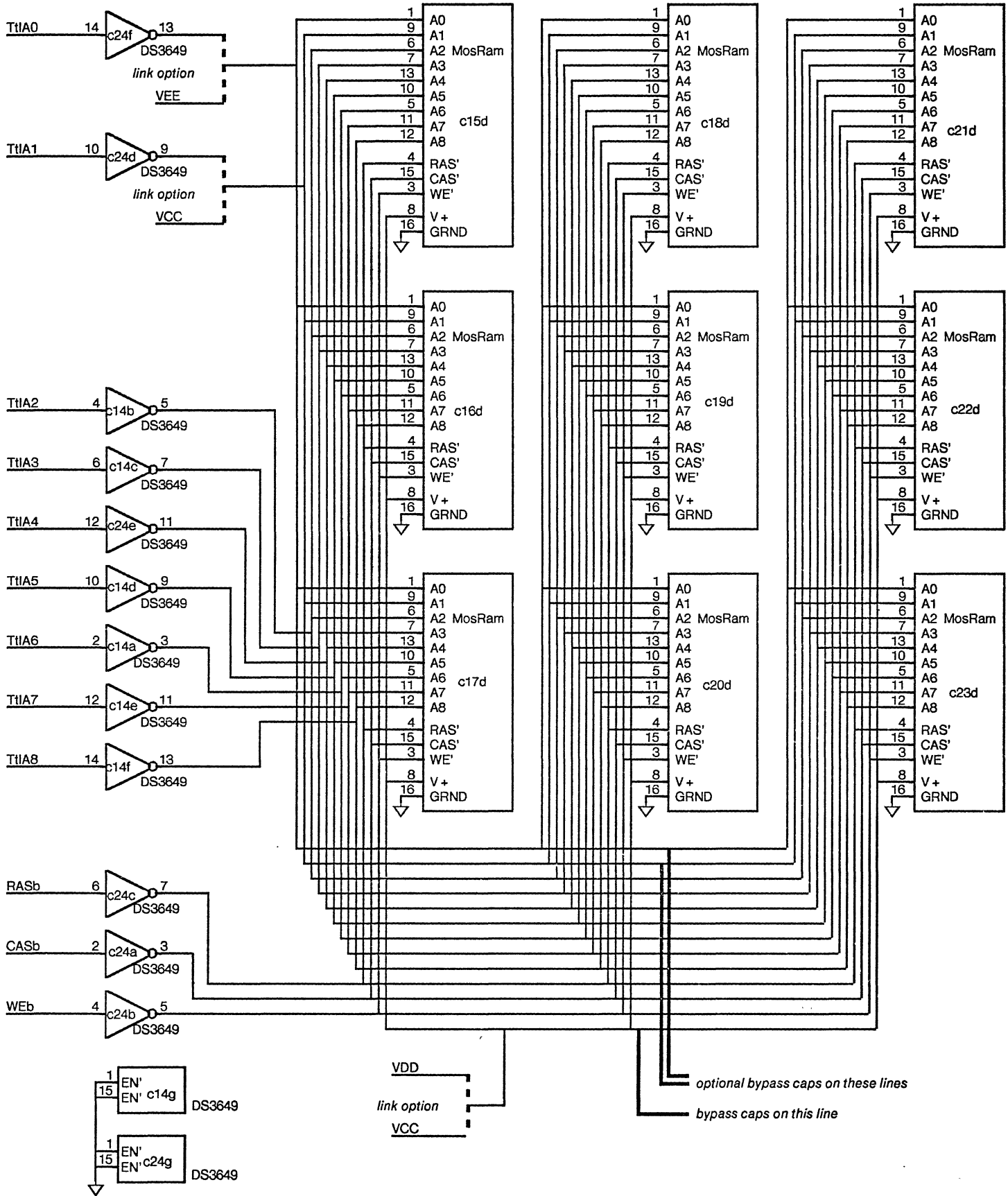


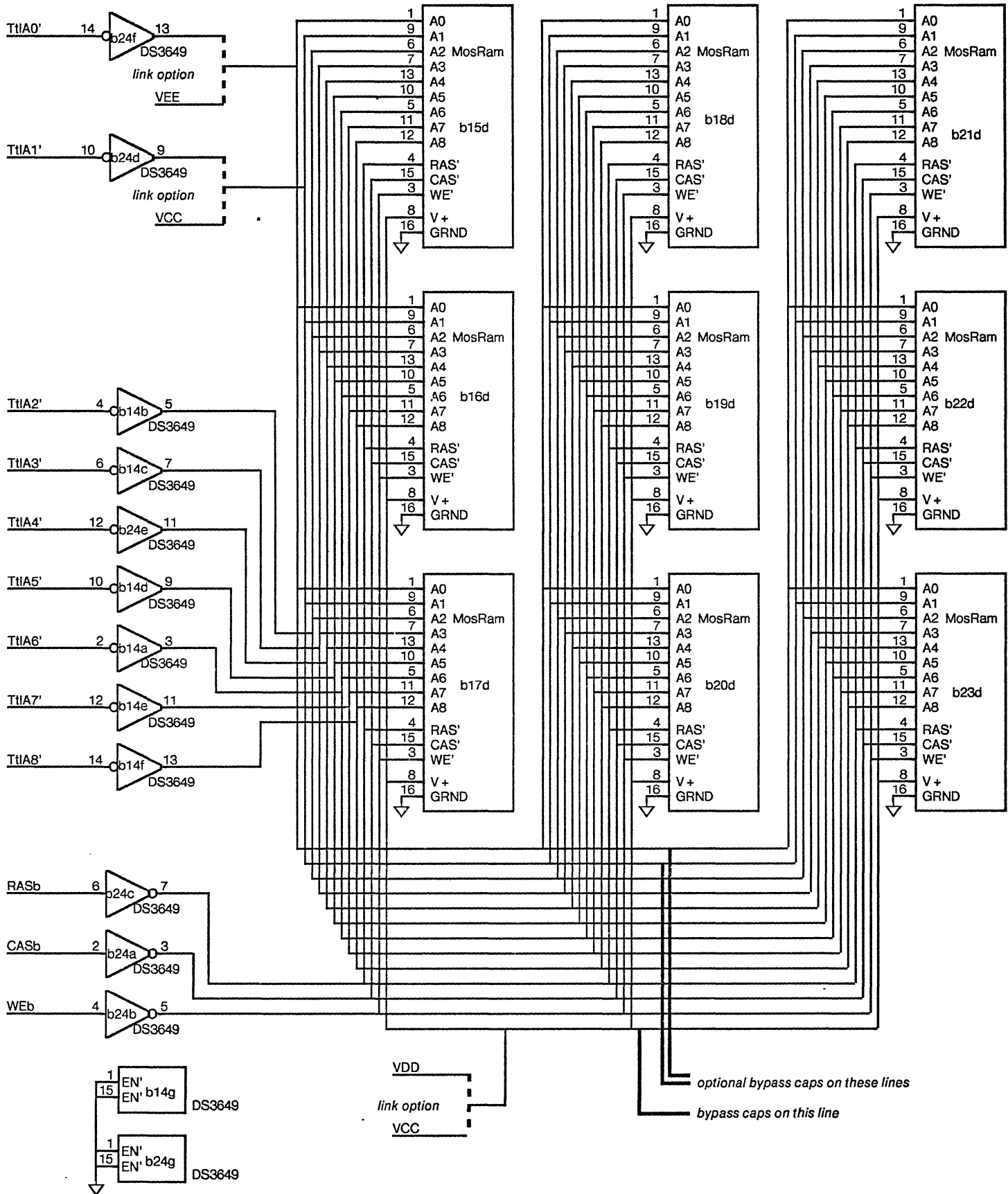


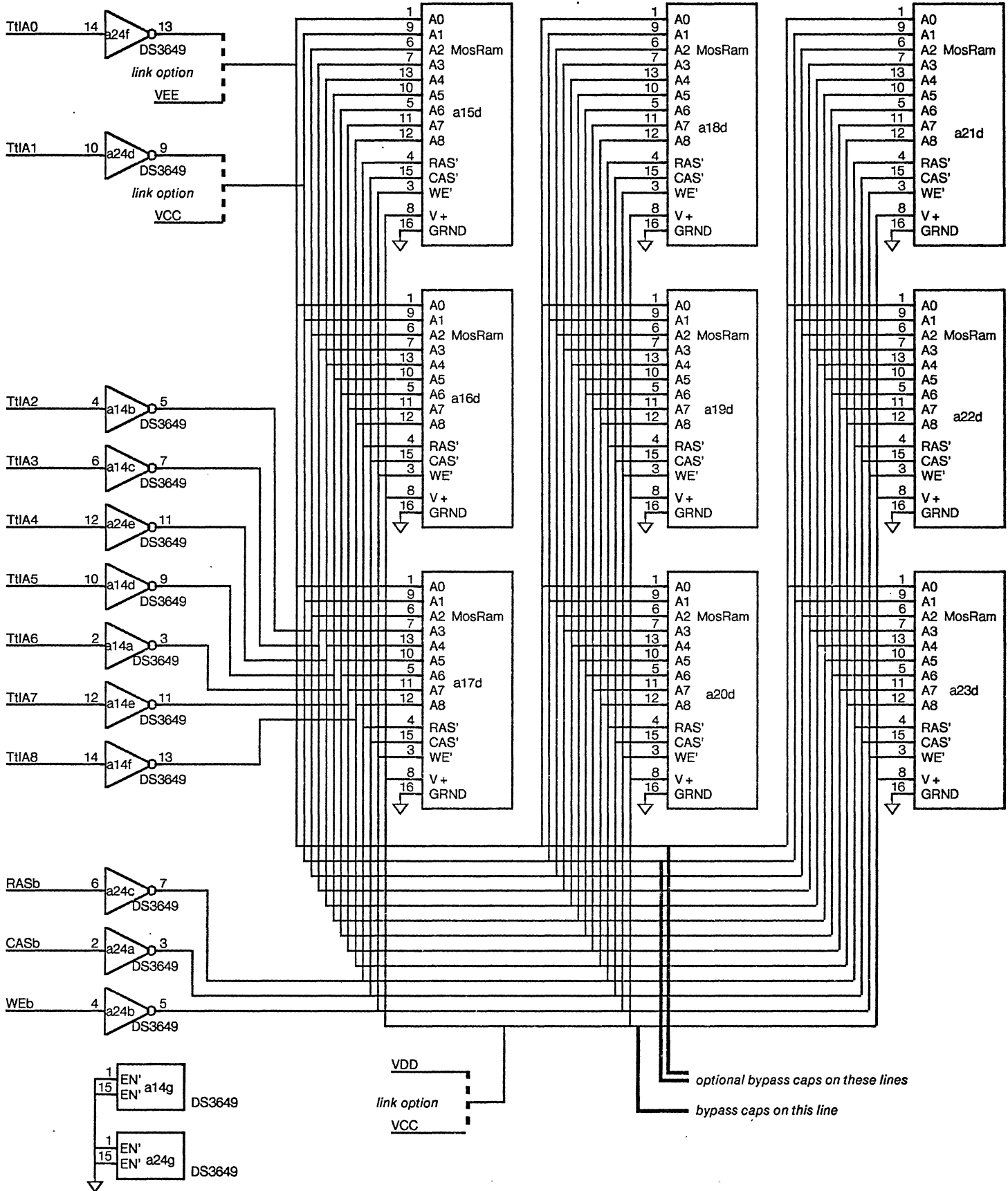


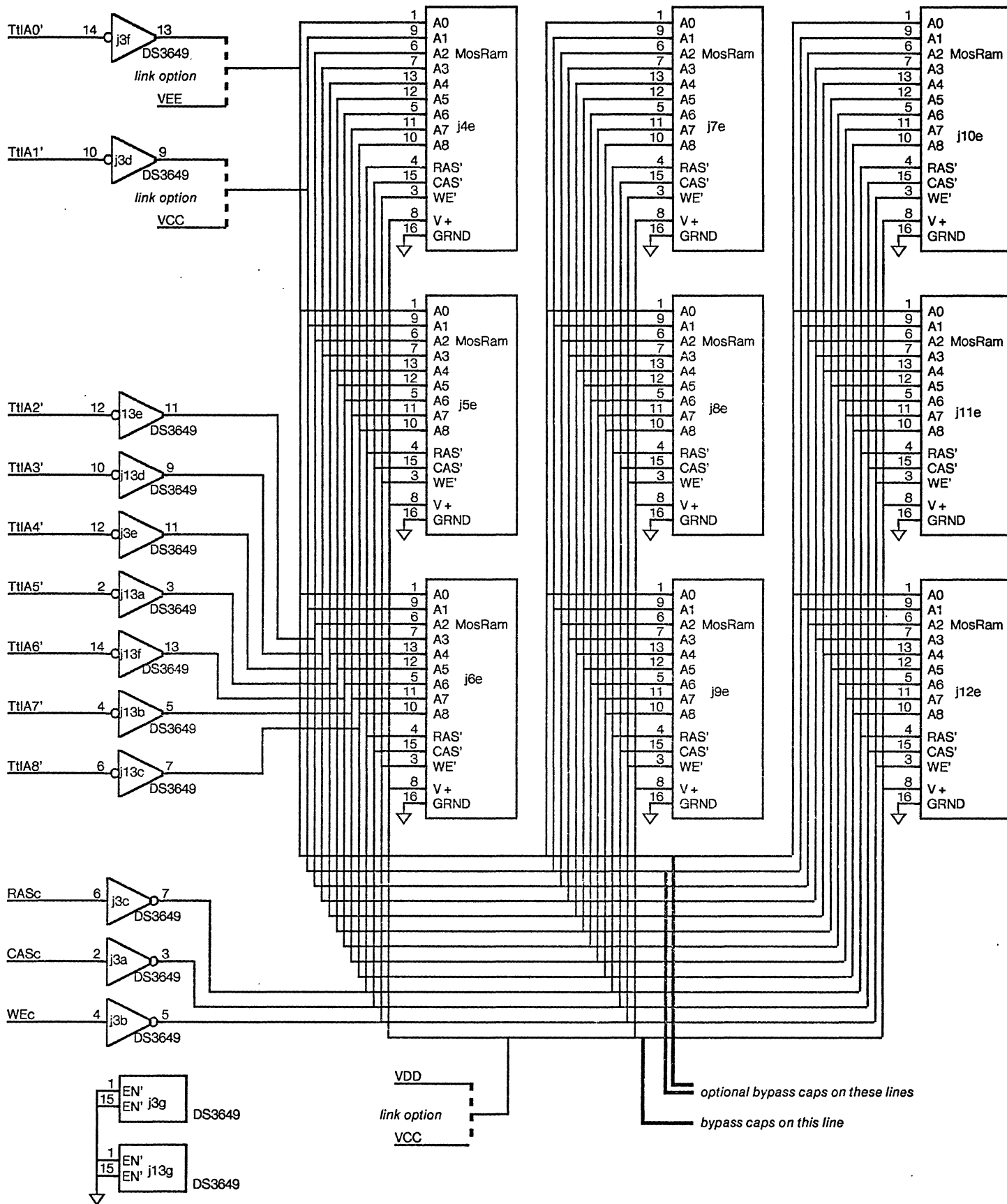


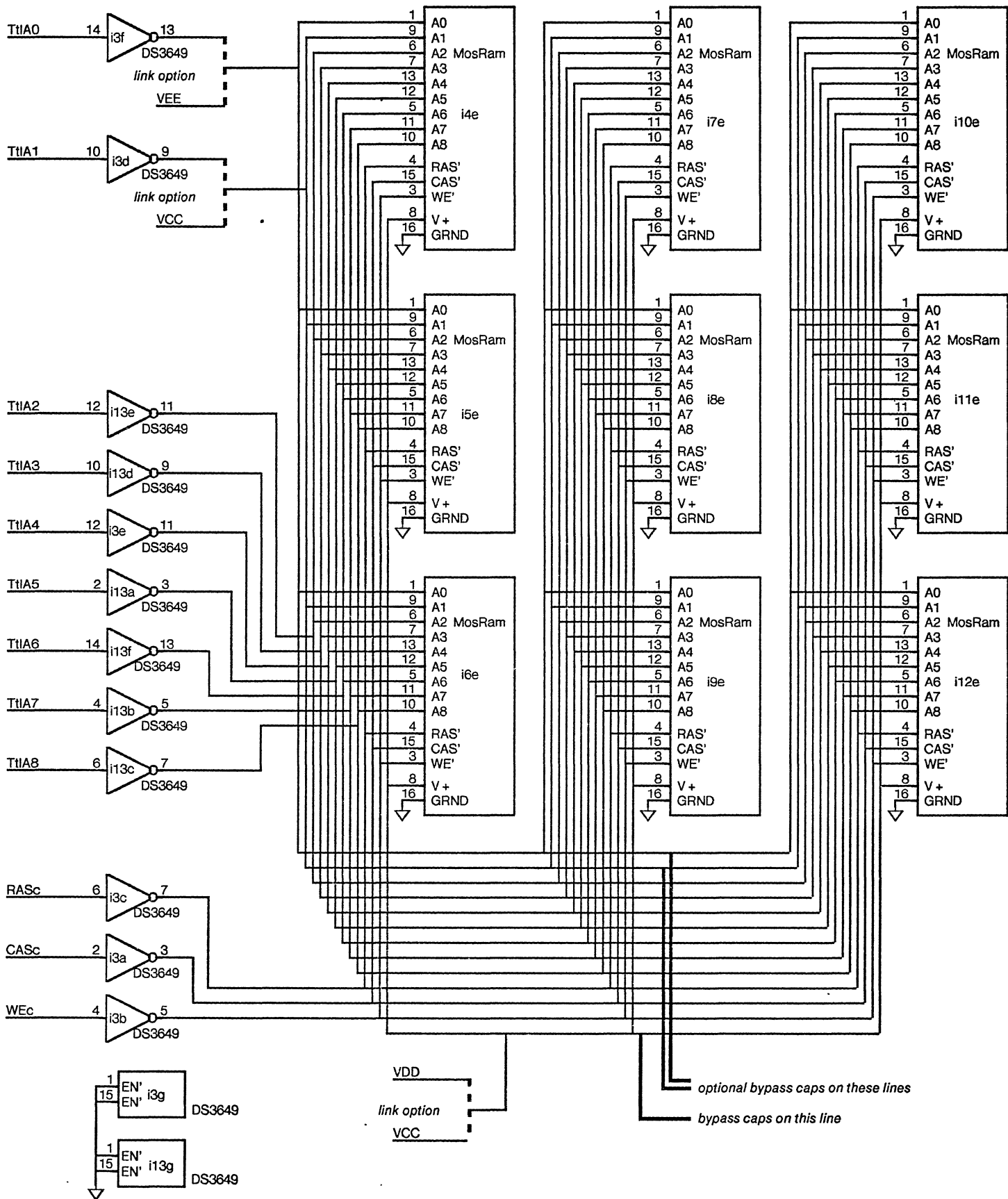


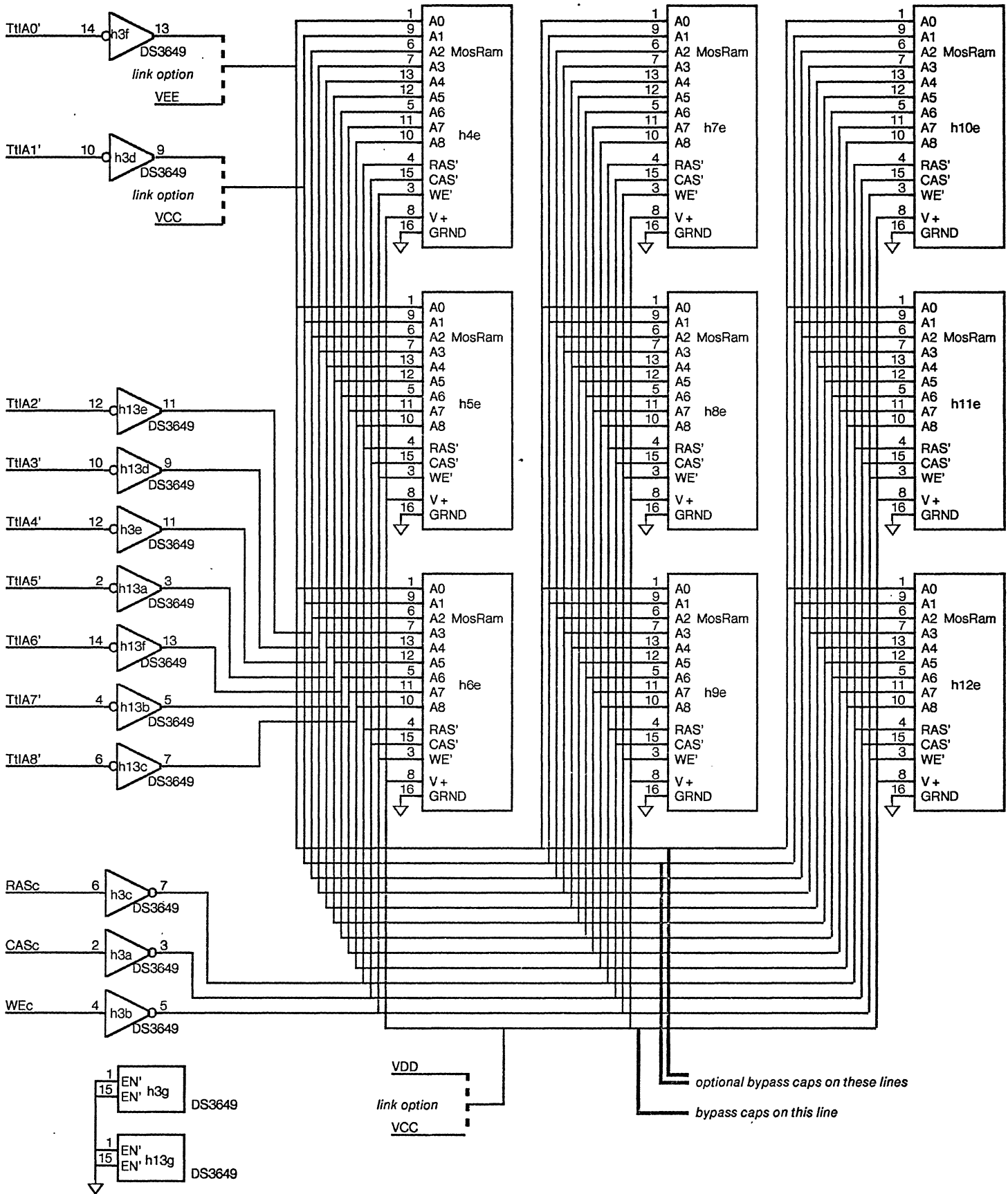


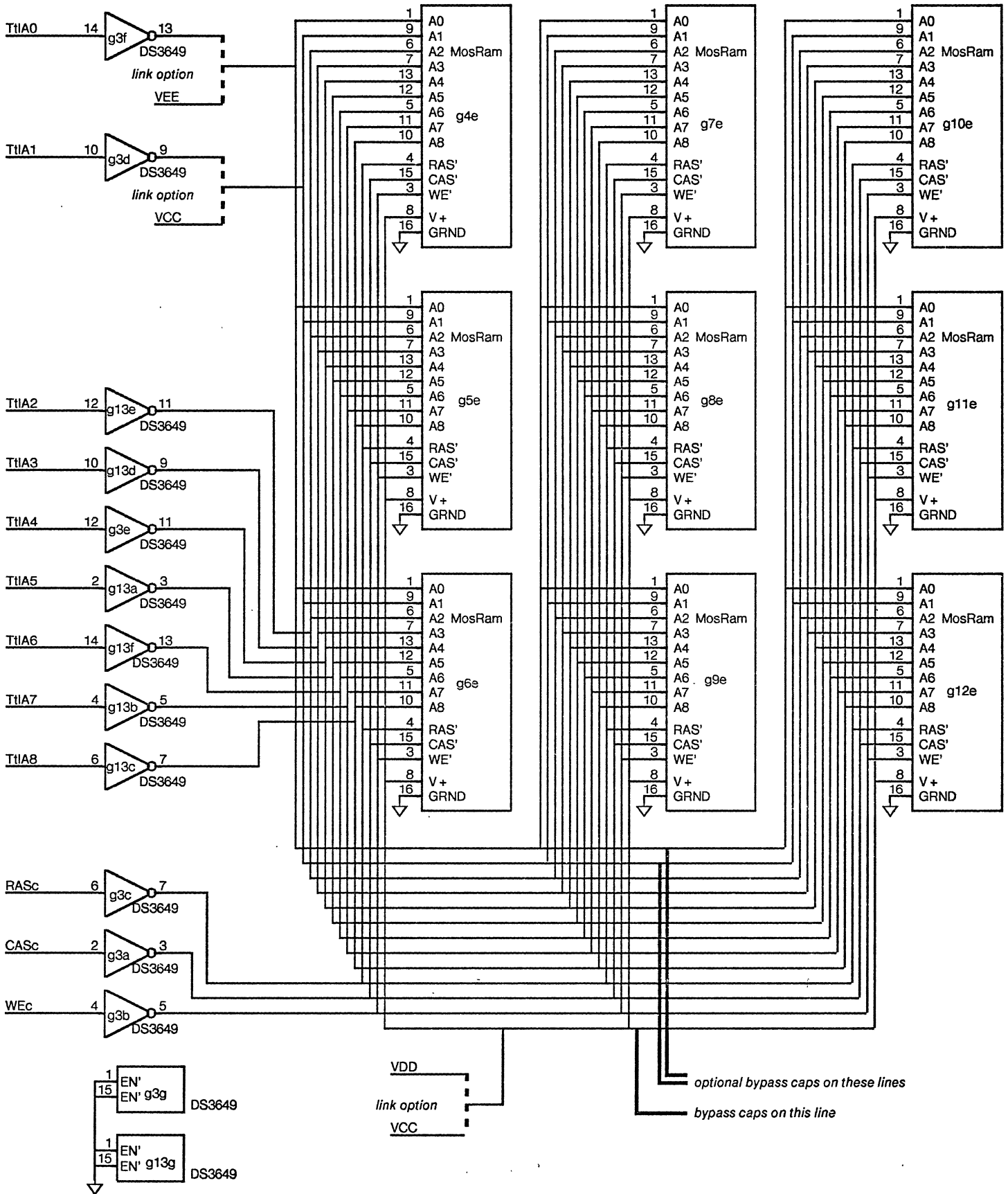


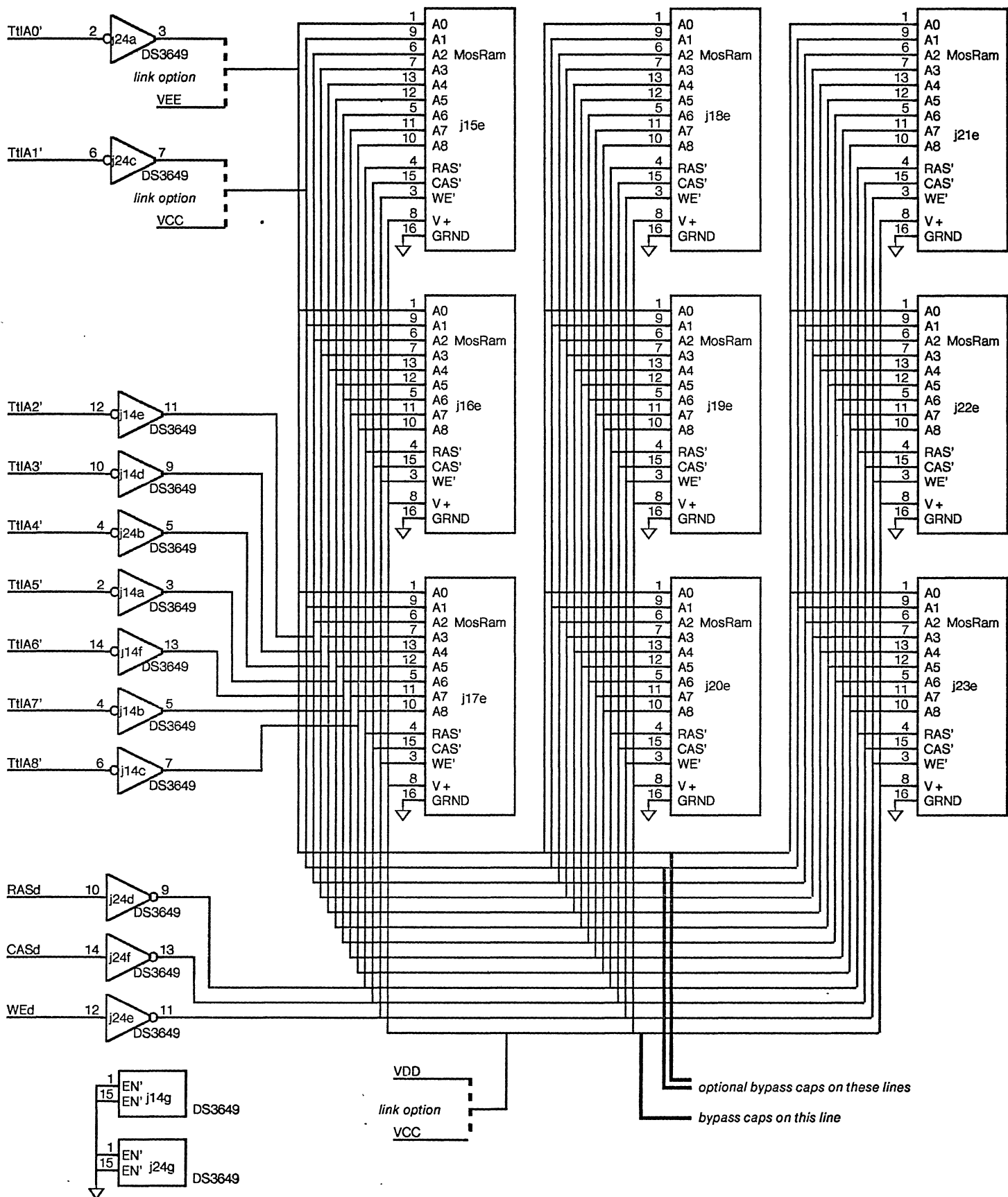


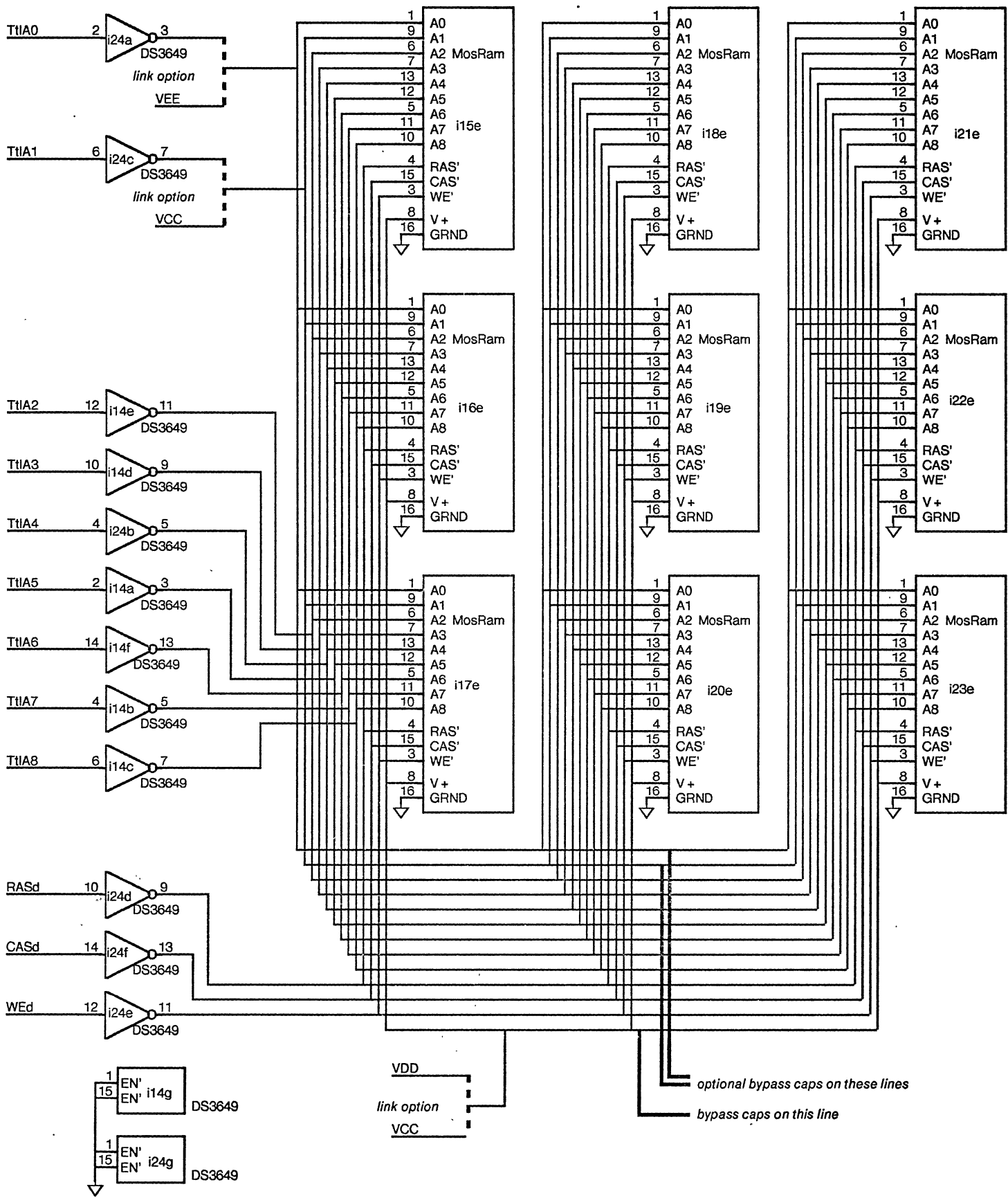


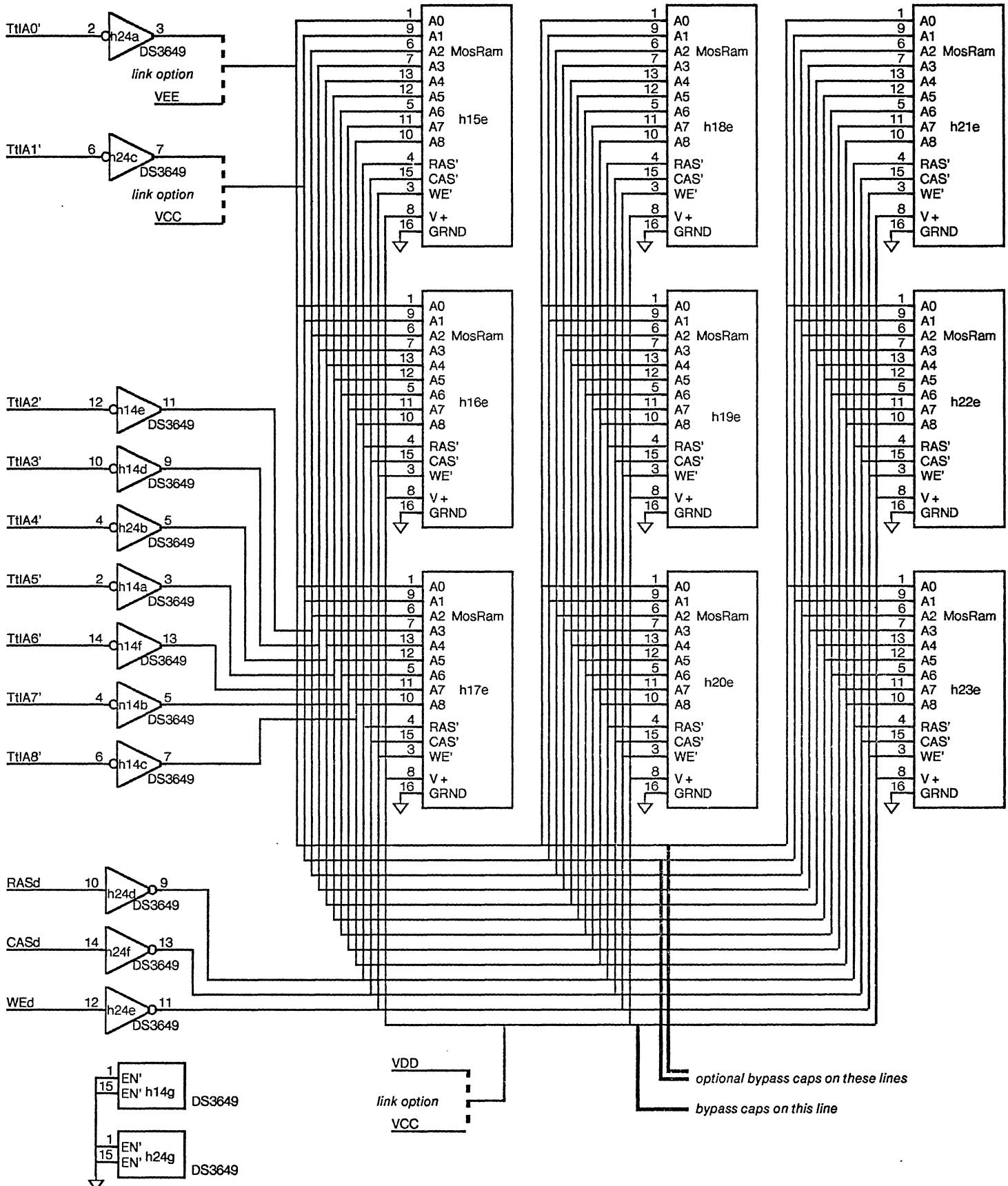


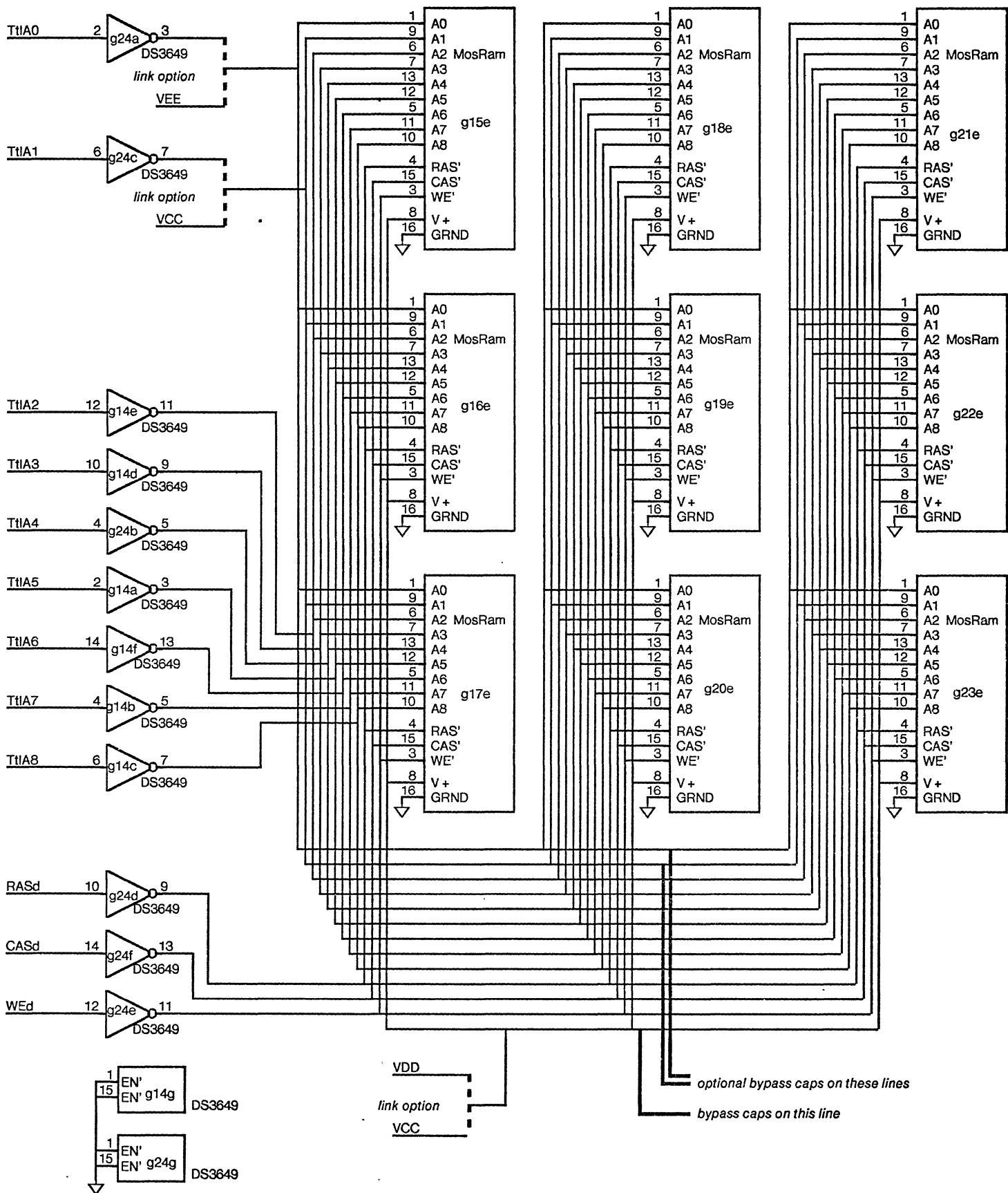












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 PcMsa-Rev-Pa.ps
 COMPONENTS:

DS3649:	13	14	15	16	17	18
	19	20	21	22	23	24
	25	26	27	28		
F16:	1	3				
MC103:	1					
MC124:	4	5	6	7	8	9
	10	11	12			
MC125:	1	2	3	4	5	6
	7	8	9	10	11	12
MC141:	1	2				
MC176:	1	4	5	6	7	8
	9	10	11	12		
MC210:	1					
MosRam:	4	5	6	7	8	9
	10	11	12	13	14	15
	16	17	18	19	20	21
	22	23	24	25	26	27
	28					
N166:	4	5	6	7	8	9
	10	11	12			
S174:	1	2	12			
S374:	1	2	4	5	6	7
	8	9	10	11		
TERM:	1	2	3	4	5	6
	7	8	9	10	11	12

SIGNAL NAMES:

+	1(1)	2(1)	3(1)	4(1)	5(1)	6(1)
	7(1)	8(1)	9(1)	10(1)	11(1)	12(1)
	13(1)	14(1)	15(1)	16(1)	17(1)	18(1)
	19(1)	20(1)	21(1)	22(1)	23(1)	24(1)
	25(1)	26(1)	27(1)	28(1)		
+3a:	4(2)	5(2)	6(1)	12(1)		
+3b:	6(1)	7(2)	12(1)			
+3c:	8(2)	9(2)	12(1)			
+3d:	10(2)	11(2)	12(1)			
a25Vbb:	6(3)	7(2)				
a2Vbb:	4(3)	5(2)				
c25Vbb:	3(5)					
CASa:	3(1)	13(1)	14(1)	15(1)	16(1)	
CASb:	3(1)	17(1)	18(1)	19(1)	20(1)	
CASc:	3(1)	21(1)	22(1)	23(1)	24(1)	
CASd:	3(1)	25(1)	26(1)	27(1)	28(1)	
ChipsAreA!:	1(1)					
ChipsAreB!:	1(1)					
ChipsAreX!:	1(1)					
CLK.ms0Even!:	1(1)					
d25Vbb:	1(1)	3(3)				
d26Vbb:	3(6)					
d2Vbb:	3(3)					
e24True:	2(1)					
e2Vbb:	12(2)					
e4True:	2(1)					
ECI:	1(1)	2(3)				
EcIn.0!:	12(1)					
EcIn.1!:	12(1)					
EcOut.0!:	12(1)					
EcOut.1!:	12(1)					
EcOut.4!:	12(1)					
EcOut.5!:	12(1)					
EnabOuta:	1(1)	4(1)	10(1)	12(1)		
EnabOutb:	1(1)	6(1)	8(1)	12(1)		
f23True:	2(1)					
f25Vbb:	2(1)					
f2Vbb:	2(1)					
f3True:	1(1)					
g25Vbb:	2(1)					
g2Vbb:	1(2)					

Gnd:	1(1)	2(1)	3(1)	4(1)	5(1)	6(1)
	7(1)	8(1)	9(1)	10(1)	11(1)	12(1)
	13(1)	14(1)	15(1)	16(1)	17(1)	18(1)
	19(1)	20(1)	21(1)	22(1)	23(1)	24(1)
	25(1)	26(1)	27(1)	28(1)		
GND:	4(4)	5(4)	6(4)	7(4)	8(4)	9(4)
	10(4)	11(4)	12(12)			
h25Vbb:	3(5)					
i25Vbb:	3(3)	12(2)				
i2Vbb:	1(1)	3(4)	9(1)			
InCKc:	1(1)					
j25Vbb:	3(5)					
j26Vbb:	3(5)					
l25Vbb:	10(3)	11(2)				
l2Vbb:	8(3)	9(1)				
LoadEcOut'!:	1(1)					
LoadSinE!:	1(1)					
LoadSoutE'!:	1(1)					
M0!:	1(1)					
Mb0:	1(1)					
MemAd.0!:	3(1)					
MemAd.1!:	3(1)					
MemAd.2!:	3(1)					
MemAd.3!:	3(1)					
MemAd.4!:	3(1)					
MemAd.5!:	3(1)					
MemAd.6!:	3(1)					
MemAd.7!:	3(1)					
MemAd.8!:	3(1)					
MemCAsa!:	3(1)					
MemCAsb!:	3(1)					
MemRAsa!:	3(1)					
MemRAsb!:	3(1)					
MemWEa!:	3(1)					
MemWEb!:	3(1)					
Mod0SinEn':	1(1)					
Mod0StrEn':	1(1)					
OutCKa:	2(1)	4(2)	5(2)	12(1)		
OutCKb:	2(1)	6(2)	7(2)	12(1)		
OutCKc:	1(1)	8(2)	9(2)	12(1)		
OutCKd:	2(1)	10(2)	11(2)	12(1)		
preClk2Sout:	1(2)					
RASa:	3(1)	13(1)	14(1)	15(1)	16(1)	
RASb:	3(1)	17(1)	18(1)	19(1)	20(1)	
RASc:	3(1)	21(1)	22(1)	23(1)	24(1)	
RASd:	3(1)	25(1)	26(1)	27(1)	28(1)	
ShiftEcOut!:	1(1)					
ShiftLoad':	1(1)	2(3)				
ShiftSinE!:	1(1)					
ShiftSoutE!:	1(1)					
SI:	1(1)	2(3)				
Sin.00!:	4(1)					
Sin.01!:	4(1)					
Sin.02!:	5(1)					
Sin.03!:	5(1)					
Sin.04!:	6(1)					
Sin.05!:	6(1)					
Sin.06!:	7(1)					
Sin.07!:	7(1)					
Sin.08!:	8(1)					
Sin.09!:	8(1)					
Sin.10!:	9(1)					
Sin.11!:	9(1)					
Sin.12!:	10(1)					
Sin.13!:	10(1)					
Sin.14!:	11(1)					
Sin.15!:	11(1)					
SinClkc':	1(1)					
SLa:	2(1)	4(2)	5(2)	12(1)		
SLb:	2(1)	6(2)	7(2)	12(1)		
SLc:	1(1)	8(2)	9(2)	12(1)		
SLd:	2(1)	10(2)	11(2)	12(1)		
S0:	1(2)	2(3)				
Sout.00!:	4(1)					
Sout.01!:	4(1)					
Sout.02!:	5(1)					

Sout.03!:	5(1)					
Sout.04!:	6(1)					
Sout.05!:	6(1)					
Sout.06!:	7(1)					
Sout.07!:	7(1)					
Sout.08!:	8(1)					
Sout.09!:	8(1)					
Sout.10!:	9(1)					
Sout.11!:	9(1)					
Sout.12!:	10(1)					
Sout.13!:	10(1)					
Sout.14!:	11(1)					
Sout.15!:	11(1)					
Tt1A0:	3(1)	14(1)	16(1)	18(1)	20(1)	22(1)
	24(1)	26(1)	28(1)			
Tt1A0':	3(1)	13(1)	15(1)	17(1)	19(1)	21(1)
	23(1)	25(1)	27(1)			
Tt1A1:	3(1)	14(1)	16(1)	18(1)	20(1)	22(1)
	24(1)	26(1)	28(1)			
Tt1A1':	3(1)	13(1)	15(1)	17(1)	19(1)	21(1)
	23(1)	25(1)	27(1)			
Tt1A2:	3(1)	14(1)	16(1)	18(1)	20(1)	22(1)
	24(1)	26(1)	28(1)			
Tt1A2':	3(1)	13(1)	15(1)	17(1)	19(1)	21(1)
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Tt1A7:	3(1)	14(1)	16(1)	18(1)	20(1)	22(1)
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	23(1)	25(1)	27(1)			
Tt1CKa':	1(1)	2(1)				
Tt1CKb':	1(1)	2(1)				
Tt1CKc':	1(1)					
Tt1CKd':	1(1)	2(1)				
VCC:	13(2)	14(2)	15(2)	16(2)	17(2)	18(2)
	19(2)	20(2)	21(2)	22(2)	23(2)	24(2)
	25(2)	26(2)	27(2)	28(2)		
VDD:	13(1)	14(1)	15(1)	16(1)	17(1)	18(1)
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	25(1)	26(1)	27(1)	28(1)		
VEE:	13(1)	14(1)	15(1)	16(1)	17(1)	18(1)
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	25(1)	26(1)	27(1)	28(1)		
WEa:	3(1)	13(1)	14(1)	15(1)	16(1)	
WEb:	3(1)	17(1)	18(1)	19(1)	20(1)	
WEc:	3(1)	21(1)	22(1)	23(1)	24(1)	
WEd:	3(1)	25(1)	26(1)	27(1)	28(1)	