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LETTERS TO THE EDITOR

NOVEL PHASE-LOCKED LOOPS WITH ENHANCED LOCKING CAPABILITIES†

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1. INTRODUCTION

Phase-locked loops (PLLs) are used in a large number of electronic devices, for instance, television sets, cellular telephones, synthesizers, oscillators, radar systems, to name a few. There is a good number of references devoted to the subject of PLLs (see, e.g., references [1–12] and the references therein).

A PLL is essentially a non-linear oscillator that locks its frequency and phase to those of the input applied to it. A standard PLL is shown in Figure 1. The components of the PLL are the phase detector (PD), loop filter (LF), and voltage controlled oscillator (VCO). The scalar-valued input to the PLL is

$$r(t) = A_i \sin(\omega_i t + \phi_i(t)) + \tilde{n}_i(t), \tag{1}$$

for all $t \geqslant 0$, where $A_i > 0$ is the input amplitude, $\omega_i > 0$ and $\phi_i(t) \in \mathbb{R}$ are the input frequency and the input phase, respectively, and $\tilde{n}_i(t) \in \mathbb{R}$ is the input noise. Without loss of generality, equation (1) can be written as

$$r(t) = A_i[\sin(\omega_i t + \phi_i(t)) + n_i(t)], \tag{2}$$

for all $t \geqslant 0$. The scalar-valued output of the PLL is

$$v(t) = A_o \cos(\omega_o t + \phi_o(t) + \phi_n(t)), \tag{3}$$

for all $t \geqslant 0$, where $A_o > 0$ is the output amplitude, $\omega_o > 0$ and $\phi_o(t) \in \mathbb{R}$ are the output frequency and the output phase, respectively, and $\phi_n(t) \in \mathbb{R}$ is the phase noise.

PLLs are required to (1) achieve

$$\omega_o t + \phi_o(t) + \phi_n(t) \approx \omega_i t + \phi_i(t), \tag{4}$$

for all t after a finite time $t^* > 0$, where in this case the output frequency and phase are locked to those of the input; and (2) achieve locking fast (small t^*). It can happen that a PLL does not achieve locking (stability problem) or achieves it after a long time. These are certainly undesirable behaviors of PLLs which should be eliminated by careful design.

In this note, a novel PLL is proposed that outperforms the standard PLL in two respects: it has a very large acquisition range and achieves locking very fast. The reason for the superior performance of the proposed PLL is a non-linear filter added to the loop.

† Patent pending.

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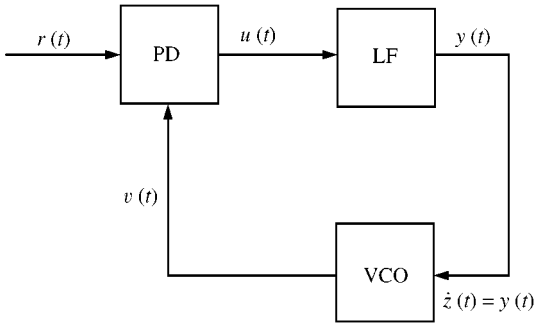

Figure 1. A standard PLL the components of which are: phase detector (PD), loop filter (LF), and voltage controlled oscillator (VCO). The input to the PLL is $t \mapsto r(t)$ and its output is $t \mapsto v(t)$.

2. A MATHEMATICAL MODEL OF PHASE-LOCKED LOOPS

A first step to the study of a PLL is to obtain a mathematical model that describes its dynamics. In particular, it is desirable to obtain a model for the evolution of a quantity of interest called the *frequency-phase error*. This quantity is defined as

$$\phi_e(t) := (\omega_o - \omega_i)t + \phi_o(t) - \phi_i(t) + \phi_n(t), \tag{5}$$

for all $t \geqslant 0$. Locking is achieved when $\phi_e(t) \approx 0$ for all t after a finite time $t^* > 0$.

A mathematical model of a PLL can be obtained when the dynamics of its components are known. In this section, the components of a standard PLL are described first. Then, a useful mathematical model of the PLL is derived by which the evolution of the frequency-phase error can be determined conveniently.

The components of the PLL in Figure 1 described in the following.

2.1. PHASE DETECTOR

A widely used phase detector (PD) is a multiplier. Having $r(\cdot)$ and $v(\cdot)$ in equations (2) and (3), respectively, the scalar-valued output of the phase detector is

$$u(t) = r(t)\, v(t) = K_d\,[\sin(\omega_i t + \phi_i(t)) + n_i(t)]\cos(\omega_o t + \phi_o(t) + \phi_n(t)), \tag{6}$$

for all $t \geqslant 0$, where $K_d > 0$ is the phase detector gain which depends on the input and output amplitudes (see, e.g., references [1, 12]). The output $u(\cdot)$ can be written as

$$\begin{aligned} u(t) = &-\tfrac{1}{2} K_d \sin(\phi_e(t)) + \tfrac{1}{2} K_d \sin((\omega_i + \omega_o)t + \phi_i(t) + \phi_o(t) + \phi_n(t)) \\ &+ K_d n_i(t) \cos(\omega_o t + \phi_o(t) + \phi_n(t)), \end{aligned} \tag{7}$$

for all $t \geqslant 0$. The first term in equation (7) is the low-frequency component of the phase detector output and the last two terms are the high-frequency components of the output.

2.2. LOOP FILTER

The loop filter (LF) is a single-input–single-output linear system that follows the phase detector. This system should be a low-pass filter in order to suppress the high-frequency components of $u(\cdot)$ — the last two terms in equation (7). This is an important role of the LF:

the more the high-frequency components of $u(\cdot)$ are suppressed, the better the PLL performs. The output of the LF can be written as

$$y(t) = -\tfrac{1}{2} K_d h(t) * \sin(\phi_e(t)) + \eta(t), \tag{8}$$

for all $t \geqslant 0$, where $h(\cdot)$ denotes the impulse response of the LF, $*$ denotes the convolution operator, and $\eta(\cdot)$ is the high-frequency component of the filter output given by

$$\eta(t) = K_d h(t) * [\tfrac{1}{2} \sin((\omega_i + \omega_o)t + \phi_i(t) + \phi_o(t) + \phi_n(t)) + n_i(t) \cos(\omega_o t + \phi_o(t) + \phi_n(t))]. \tag{9}$$

When the LF is an effective low-pass filter, $\eta(\cdot)$ is negligible.

Commonly used LFs have the transfer functions (see, e.g., references [1, 12])

$$H_1(s) = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2)s}, \quad H_2(s) = \frac{K_f(1 + \tau_2 s)}{1 + \tau_1 s}, \quad H_3(s) = \frac{1 + \tau_2 s}{\tau_1 s}, \tag{10}$$

for all $s \in \mathbb{C}$, where $\tau_1 > 0$, $\tau_2 > 0$, and $K_f > 0$ are parameters to be determined to make the LF a low-pass filter and achieve certain design objectives.

The state-space representation of the LF is

$$\dot{x}(t) = Ax(t) + bu(t), \quad x(0) =: x_0, \tag{11a}$$

$$y(t) = cx(t) + du(t), \tag{11b}$$

for all $t \geqslant 0$. In equations (11), for all $t \in \mathbb{R}$, the state vector of the filter $x(t) \in \mathbb{R}^n$ and the input $u(t)$ and the output $y(t)$ are those in equation (6) and (8), respectively; the coefficient matrices of the filter are $A \in \mathbb{R}^{n \times n}$, $b \in \mathbb{R}^n$, $c \in \mathbb{R}^{1 \times n}$, and $d \in \mathbb{R}$. As an example of the state-space representation, consider that of $H_3(s)$:

$$\dot{x}(t) = u(t), \quad x(0) =: x_0, \tag{12a}$$

$$y(t) = \left(\frac{1}{\tau_1}\right) x(t) + \left(\frac{\tau_2}{\tau_1}\right) u(t), \tag{12b}$$

for all $t \geqslant 0$.

2.3. VOLTAGE CONTROLLED OSCILLATOR

The voltage controlled oscillator (VCO) is a special component of PLLs. The input to the VCO is $y(\cdot)$ in equation (11b). Let

$$\dot{z}(t) := y(t), \tag{13}$$

for all $t \geqslant 0$. With this definition, the output phase is

$$\phi_o(t) = K_o z(t), \tag{14}$$

for all $t \geqslant 0$, where $K_o > 0$ is the VCO gain. The reason for equations (13) and (14) is that there is an integrator in the VCO which generates the output phase. The output of the VCO is $v(\cdot)$ in equation (3).

Thus far the dynamics of the components of PLLs are described. Using equations (11), (6), (13), and (14), a non-linear mathematical model of PLLs can be written as

$$\dot{x}(t) = Ax(t) + bK_d[\sin(\omega_i t + \phi_i(t)) + n_i(t)]\cos(\omega_o t + K_o z(t) + \phi_n(t)), \quad x(0) =: x_0, \tag{15a}$$

$$\dot{z}(t) = cx(t) + dK_d[\sin(\omega_i t + \phi_i(t)) + n_i(t)]\cos(\omega_o t + K_o z(t) + \phi_n(t)), \quad z(0) =: z_0 = \phi_o(0)/K_o, \tag{15b}$$

for all $t \geqslant 0$. The mathematical model in equations (15) provides a useful and convenient tool for simulating the dynamics of PLLs. By solving the system (15) (numerically), the evolution of the frequency-phase error can be determined via

$$\phi_e(t) = (\omega_o - \omega_i)t + K_o z(t) - \phi_i(t) + \phi_n(t), \tag{16}$$

for all $t \geqslant 0$. As stated earlier, a PLL achieves locking when $\phi_e(t) \approx 0$ for all t after a finite time $t^* > 0$.

3. NOVEL PHASE-LOCKED LOOPS WITH NON-LINEAR FILTERS

The contribution of this note, which is the design of a novel PLL with enhanced locking capabilities, is unveiled in this section. The proposed PLL is shown in Figure 2. This PLL is essentially the same as that in Figure 1, except that the LF is followed by a non-linearity N. The non-linearity N or the series connection of the LF with N is called the *non-linear filter*. The PLL in Figure 2 is denoted by NPLL.

The non-linearity N is chosen as one of the following functions

$$N(y) = K_n \tanh\left(\frac{y}{\varepsilon}\right), \quad N(y) = \frac{K_n y}{\varepsilon + |y|}, \tag{17a,b}$$

for all $y \in \mathbb{R}$, where $K_n > 0$ and $0 < \varepsilon < 1$. The graphs of N in equations (17) are depicted in Figure 3. It is straightforward to show that by decreasing ε the slope of N at the origin increases.

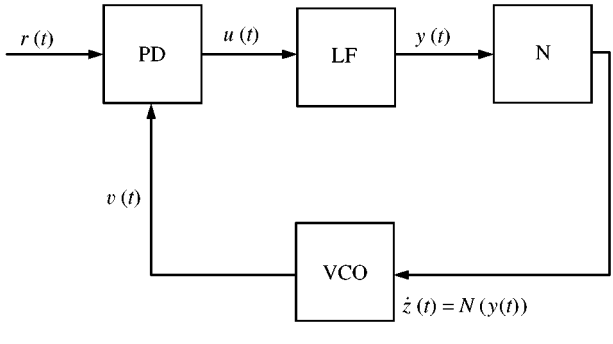

Figure 2. The NPLL in which the LP is followed by the non-linearity N.

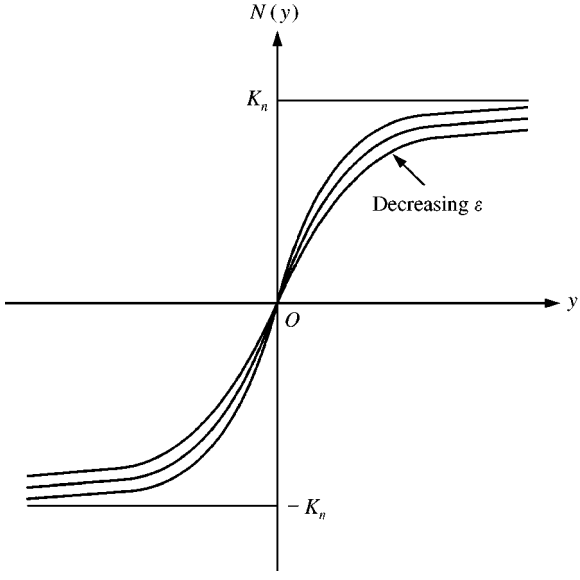

Figure 3. The graphs of the non-linearity N in equations (17). By decreasing ε the slope of N at the origin increases.

The behavior of the NPLL can be determined quantitatively by simulating its mathematical model. This model, which is obtained from equations (15), is

$$\dot{x}(t) = Ax(t) + bK_d[\sin(\omega_i t + \phi_i(t)) + n_i(t)]\cos(\omega_o t + K_o z(t) + \phi_n(t)), \quad x(0) =: x_o, \tag{18a}$$

$$y(t) = cx(t) + dK_d[\sin(\omega_i t + \phi_i(t)) + n_i(t)]\cos(\omega_o t + K_o z(t) + \phi_n(t)), \tag{18b}$$

$$\dot{z}(t) = N(y(t)), \quad z(0) =: z_0 = \phi_o(0)/K_o, \tag{18c}$$

for all $t \geqslant 0$. Simulation of the system (18) provides evidence that, due to the non-linearity N, the NPLL outperforms the standard PLL: (1) the NPLL has a large acquisition range, i.e., it can achieve locking in situations where the standard PLL cannot; and (2) The NPLL achieves locking much faster than the PLL.

It should be pointed out that non-linearities somewhat similar to those in equations (17) were introduced in control laws that achieve robust and simultaneous tracking (locking) for a group of systems in finite time (see reference [13]). Such non-linear control laws were successfully used to control biaxial (also known as XY) positioning tables (see reference [14]).

4. PERFORMANCE OF NPLLS

In this section, the performance of the NPLL is examined carefully for different conditions and is compared to that of the standard PLL.

An example of the standard PLL is chosen from reference [1], where the LF is $H_3(s)$ in equation (10). To this PLL the non-linearity in equation (17a) is added in order to make the NPLL. Using the state-space representation of $H_3(s)$ in equations (12), the mathematical

models of the PLL and NPLL are obtained as

$$\dot{x}(t) = K_d[\sin(\omega_i t + \phi_i(t)) + n_i(t)]\cos(\omega_o t + K_o z(t) + \phi_n(t)), \quad x(0) =: x_0, \tag{19a}$$

$$y(t) = \left(\frac{1}{\tau_1}\right)x(t) + \left(\frac{\tau_2}{\tau_1}\right)K_d[\sin(\omega_i t + \phi_i(t)) + n_i(t)]\cos(\omega_o t + K_o z(t) + \phi_n(t)), \tag{19b}$$

$$\text{for PLL: } \dot{z}(t) = y(t), \quad z(0) =: z_0 = \phi_o(0)/K_o, \tag{19c}$$

$$\text{for NPLL: } \dot{z}(t) = K_n \tanh\left(\frac{y(t)}{\varepsilon}\right), \quad z(0) =: z_0 = \phi_o(0)/K_o, \tag{19d}$$

for all $t \geqslant 0$, where equations (19a) and (19b) are standard by both the standard PLL and NPLL.

The parameters of the PLL, which are chosen from reference [1], are

$$K_d = 0{\cdot}2\,\text{V}, \quad K_o = 260\,\text{rad/(s V)}, \tag{20a}$$

$$\tau_1 = 0{\cdot}17\,\text{s}, \quad \tau_2 = 0{\cdot}08\,\text{s}. \tag{20b}$$

The parameters of the non-linearity N are chosen as

$$K_n = 1\,\text{V}, \quad \varepsilon = 0{\cdot}1\,\text{V}. \tag{21}$$

Having the system (19)–(21) set-up, several (numerical) tests are carried out.

Test 1: Let

$$\text{frequencies: } \omega_i = \omega_o = 6280\,\text{rad/s}, \tag{22a}$$

$$\text{input phase: } \phi_i(t) = 0, \tag{22b}$$

$$\text{input noise: } n_i(t) = 0{\cdot}01\sin 100t, \tag{22c}$$

$$\text{phase noise: } \phi_n(t) = 0{\cdot}001\sin 1000t, \tag{22d}$$

for all $t \geqslant 0$. With this set-up and the initial conditions $x_0 = 0$ and $z_0 = 0{\cdot}01$ s V, equations (19)–(21) are solved numerically to obtain the time histories of the frequency-phase error $t \mapsto \phi_e(t)$ for the standard PLL and NPLL via equation (16). These time histories are depicted in Figure 4. It is evident that the frequency-phase error of the NPLL locks to zero much faster than that of the PLL.

Test 2: Let

$$\text{frequencies: } \omega_i = \omega_o = 6280\,\text{rad/s}, \tag{23a}$$

$$\text{input phase: } \phi_i(t) = 0{\cdot}1\sin 10t, \tag{23b}$$

$$\text{input noise: } n_i(t) = 0{\cdot}01\sin 100t, \tag{23c}$$

$$\text{phase noise: } \phi_n(t) = 0{\cdot}001\sin 1000t, \tag{23d}$$

for all $t \geqslant 0$. With this set-up and the initial conditions $x_0 = 0$ and $z_0 = 0{\cdot}01$ s V, equations (19)–(21) are solved numerically to obtain the time histories of the frequency-phase error $t \mapsto \phi_e(t)$ for the standard PLL and NPLL via equation (16). These time histories are depicted in Figure 5. It is evident that the frequency-phase error of the NPLL locks to zero where as that of the PLL cannot do so.

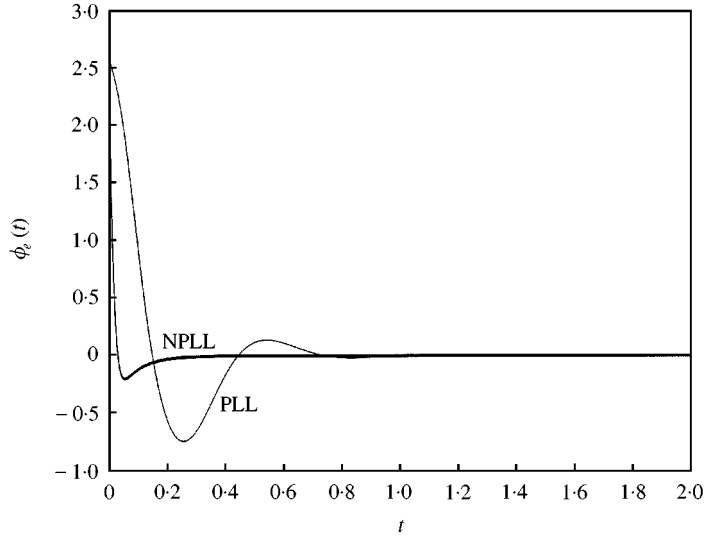

Figure 4. The time histories of the frequency-phase error $t \mapsto \phi_e(t)$ in Test 1. The NPLL achieves locking much faster than the standard PLL.

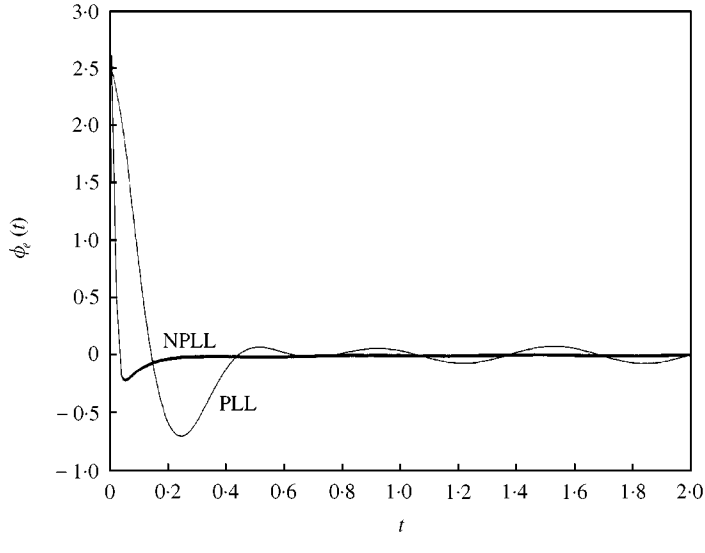

Figure 5. The time histories of the frequency-phase error $t \mapsto \phi_e(t)$ in Test 2. The NPLL can achieve locking where as the standard PLL cannot do so.

Test 3: Let

$$\text{frequencies:} \quad \omega_i = 6280 \text{ rad/s}, \quad \omega_o = 6255 \text{ rad/s}, \tag{24a}$$

$$\text{input phase:} \quad \phi_i(t) = 0{\cdot}01 \sin 10t, \tag{24b}$$

$$\text{input noise:} \quad n_i(t) = 0{\cdot}01 \sin 100t, \tag{24c}$$

$$\text{phase noise:} \quad \phi_n(t) = 0{\cdot}001 \sin 1000t, \tag{24d}$$

for all $t \geqslant 0$. With this set-up and the initial conditions $x_0 = 0$ and $z_0 = 0{\cdot}01$ s V, equations (19)–(21) are solved numerically to obtain the time histories of the frequency-phase error $t \mapsto \phi_e(t)$ for the standard PLL and NPLL via equation (16). These time histories are depicted in Figure 6. It is evident that the frequency-phase error of the NPLL locks to zero much faster than that of the PLL.

Test 4: Let

$$\text{frequencies:} \quad \omega_i = 6280\,\text{rad/s}, \quad \omega_o = 6250\,\text{rad/s}, \tag{25a}$$

$$\text{input phase:} \quad \phi_i(t) = 0{\cdot}05 \sin t, \tag{25b}$$

$$\text{input noise:} \quad n_i(t) = 0{\cdot}01 \sin 100t, \tag{25c}$$

$$\text{phase noise:} \quad \phi_n(t) = 0{\cdot}001 \sin 1000t, \tag{25d}$$

for all $t \geqslant 0$. With this set-up and the initial conditions $x_0 = 0$ and $z_0 = 0{\cdot}01$ s V, equations (19)–(21) are solved numerically to obtain the time histories of the frequency-phase error $t \mapsto \phi_e(t)$ for the standard PLL and NPLL via equation (16). These time histories are depicted in Figure 7. It is evident that the frequency-phase error of the NPLL locks to zero where as that of the PLL cannot do so.

Test 5: Let

$$\text{frequencies:} \quad \omega_i = 6280\,\text{rad/s}, \quad \omega_o = 6290\,\text{rad/s}, \tag{26a}$$

$$\text{input phase:} \quad \phi_i(t) = 0{\cdot}05 \sin 10t, \tag{26b}$$

$$\text{input noise:} \quad n_i(t) = 0{\cdot}01 \sin 100t, \tag{26c}$$

$$\text{phase noise:} \quad \phi_n(t) = 0{\cdot}001 \sin 1000t, \tag{26d}$$

for all $t \geqslant 0$. With this set-up and the initial conditions $x_0 = 0$ and $z_0 = 0{\cdot}01$ s V, equations (19)–(21) are solved numerically to obtain the time histories of the frequency-phase error

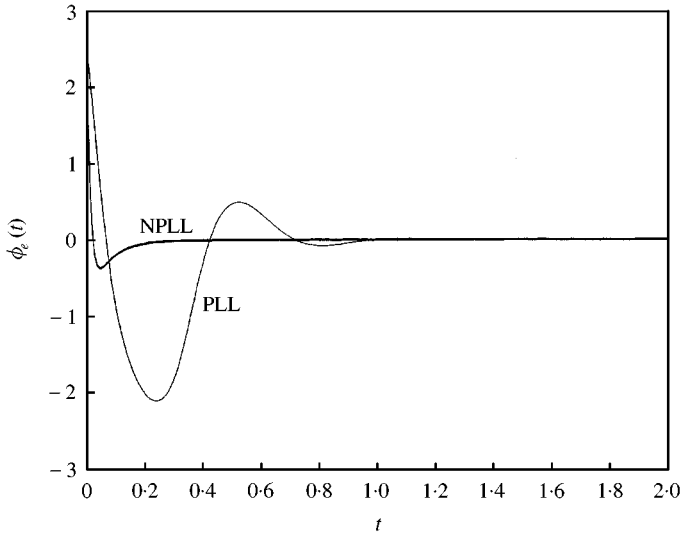

Figure 6. The time histories of the frequency-phase error $t \mapsto \phi_e(t)$ in Test 3. The NPLL achieves locking much faster than the standard PLL.

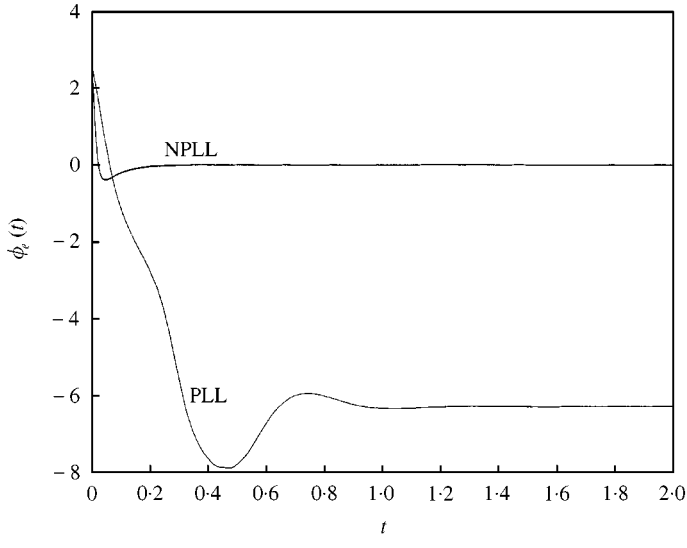

Figure 7. The time histories of the frequency-phase error $t \mapsto \phi_e(t)$ in Test 4. The NPLL can achieve locking where as the standard PLL cannot do so.

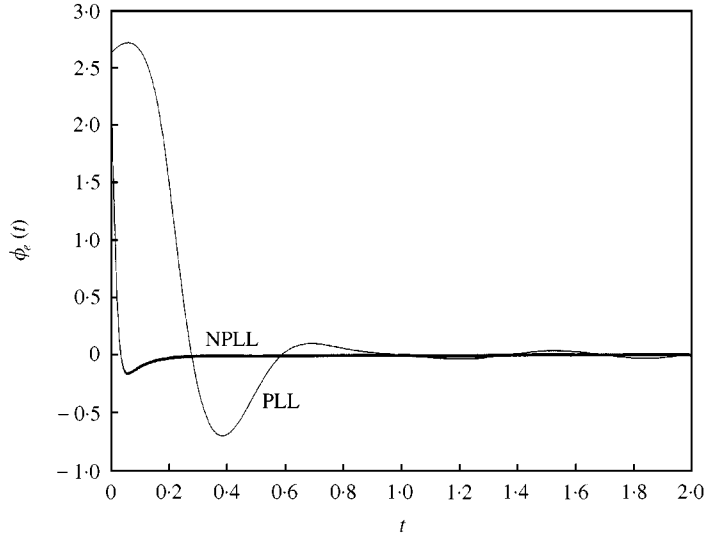

Figure 8. The time histories of the frequency-phase error $t \mapsto \phi_e(t)$ in Test 5. The NPLL achieves locking much faster than the standard PLL.

$t \mapsto \phi_e(t)$ for the standard PLL and NPLL via equation (16). These time histories are depicted in Figure 8. It is evident that the frequency-phase error of the NPLL locks to zero much faster than that of the PLL. It should be added that for the output frequency $\omega_o = 6291$ rad/s, the frequency-phase error of the NPLL locks to zero where as that of the PLL cannot do so.

Test 6: Let

$$\text{frequencies:} \quad \omega_i = 6280\,\text{rad/s}, \quad \omega_o = 6200\,\text{rad/s}, \tag{27a}$$

$$\text{input phase:} \quad \phi_i(t) = 0{\cdot}1 \sin 10t, \tag{27b}$$

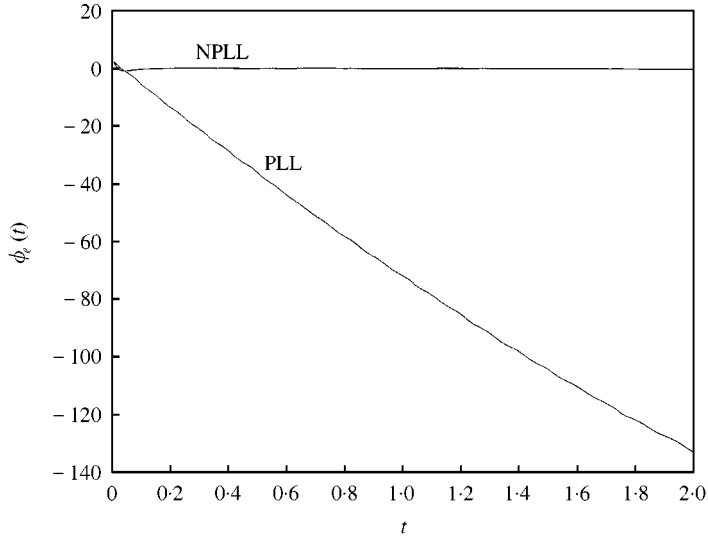

Figure 9. The time histories of the frequency-phase error $t \mapsto \phi_e(t)$ in Test 6. The NPLL can achieve locking where as the standard PLL cannot do so.

$$\text{input noise:} \quad n_i(t) = 0{\cdot}01 \sin 100t, \tag{27c}$$

$$\text{phase noise:} \quad \phi_n(t) = 0{\cdot}001 \sin 1000t, \tag{27d}$$

for all $t \geqslant 0$. With this set-up and the initial conditions $x_0 = 0$ and $z_0 = 0{\cdot}01$ s V, equations (19)–(21) are solved numerically to obtain the time histories of the frequency-phase error $t \mapsto \phi_e(t)$ for the standard PLL and NPLL via equation (16). These time histories are depicted in Figure 9. It is evident that the frequency-phase error of the NPLL locks to zero where as that of the PLL cannot do so.

5. CONCLUSIONS

In his note, a novel PLL is introduced. The proposed PLL, denoted by NPLL, incorporates a nonlinear filter in its loop. The NPLL outperforms the standard PLL: (1) it has a large acquisition range, i.e., it can achieve locking in situations where the standard PLL cannot; for instance, when the input and output frequencies are very different from each other; and (2) it achieves locking much faster than the PLL. The superior performance of the NPLL is due to the non-linear filter in its loop. Results of many tests, only six of which are reported in this note, show the superior performance of the NPLL.

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