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DESIGN OF HIGH-PERFORMANCE PHASE-LOCKED LOOPS AND SYNTHESIZERS

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1. INTRODUCTION

Phase-locked loops (PLLs) are used in a large number of electronic devices, for instance, television sets, cellular telephones, synthesizers, oscillators, radar systems, to name a few. There is a good number of references devoted to the subject of PLLs; see, e.g., references [1–12] and the references therein.

A PLL is essentially a non-linear oscillator that locks its frequency and phase to those of the input applied to it. A standard PLL is shown in Figure 1. The components of the PLL are the phase-frequency detector (PFD), loop filter (LF), and voltage-controlled oscillator (VCO). The scalar-valued input to the PLL is

$$r(t) = A_i P_i(\omega_i t + \phi_i(t)) + n_i(t), \tag{1}$$

for all $t \geqslant 0$, where $A_i > 0$ is the input amplitude, $\omega_i > 0$ and $\phi_i(t) \in \mathbb{R}$ are the input frequency and the input phase, respectively, $P_i : \mathbb{R} \to \mathbb{R}$ is a periodic function of period $T_i = 2\pi/\omega_i$, and $n_i(t) \in \mathbb{R}$ is the input noise. The scalar-valued output of the PLL is

$$v(t) = A_o P_o(\omega_o t + \phi_o(t) + \phi_n(t)), \tag{2}$$

for all $t \geqslant 0$, where $A_o > 0$ is the output amplitude, $\omega_o > 0$ and $\phi_o(t) \in \mathbb{R}$ are the output frequency and the output phase, respectively, $P_o : \mathbb{R} \to \mathbb{R}$ is a periodic function of period $T_o = 2\pi/\omega_o$, and $\phi_n(t) \in \mathbb{R}$ is the phase noise.

PLLs are required to: (1) achieve

$$\omega_o t + \phi_o(t) + \phi_n(t) \approx \omega_i t + \phi_i(t), \tag{3}$$

for all t after a finite time $t^* > 0$, where in this case the output frequency and phase are locked to those of the input; (2) achieve locking fast (small t^*). It can happen that a PLL does not achieve locking (stability problem) or achieves it after a long time. These are certainly undesirable behaviors of PLLs which should be eliminated by careful design.

In this note, a novel PLL is proposed that performs extremely well: it has a large acquisition range and achieves locking fast. In particular, it outperforms the standard PLL in achieving locking fast. The superior performance of the proposed PLL is due to the PFD and a non-linear filter added to the loop.

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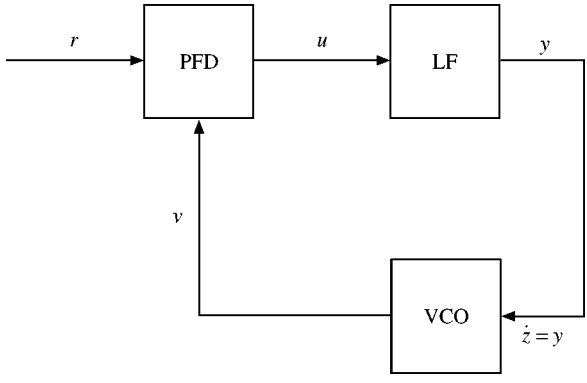

Figure 1. A standard PLL the components of which are PFD (phase-frequency detector), LF (loop filter), and VCO (voltage-controlled oscillator). The input to the PLL is $t \mapsto r(t)$ and its output is $t \mapsto v(t)$.

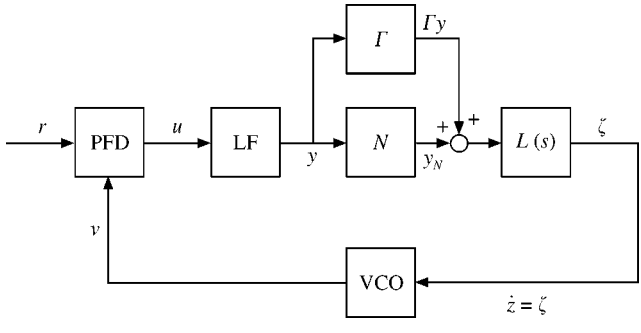

Figure 2. The NPLL in which the parallel connection of the non-linear element N and the constant gain Γ succeeds the LF and is followed by the low-pass filter $L(s)$.

2. NOVEL PHASE-LOCKED LOOPS WITH NON-LINEAR FILTERS

The contribution of this note, which is the design of a novel PLL with enhanced locking capabilities, is unveiled in this section. The proposed PLL is shown in Figure 2. In this PLL, the parallel connection of a non-linear element N and a constant gain Γ succeeds the LF and is followed by a low-pass filter $L(s)$. The non-linear element N, or the parallel connection of N and Γ, or the parallel connection of N and Γ connected serially to $L(s)$, or the series connection of the LF to the parallel connection of N and Γ connected serially to $L(s)$ is called the *non-linear filter*. The PLL in Figure 2 is denoted by NPLL. Note that if the loop containing N is disconnected and Γ and $L(s)$ are set equal to 1, then the NPLL becomes the standard PLL.

A first step to the study of the NPLL is to obtain a mathematical model that describes its dynamics. In particular, it is desirable to obtain a model for the evolution of a quantity of interest called the *frequency-phase error*. This quantity is defined as

$$\phi_e(t) := (\omega_o - \omega_i)t + \phi_o(t) - \phi_i(t) + \phi_n(t), \tag{4}$$

for all $t \geqslant 0$. Locking is achieved when $\phi_e(t) \approx 0$ for all t after a finite time $t^* > 0$.

A mathematical model of the NPLL can be obtained when the dynamics of its components are known. In this section, the components of the NPLL are first described.

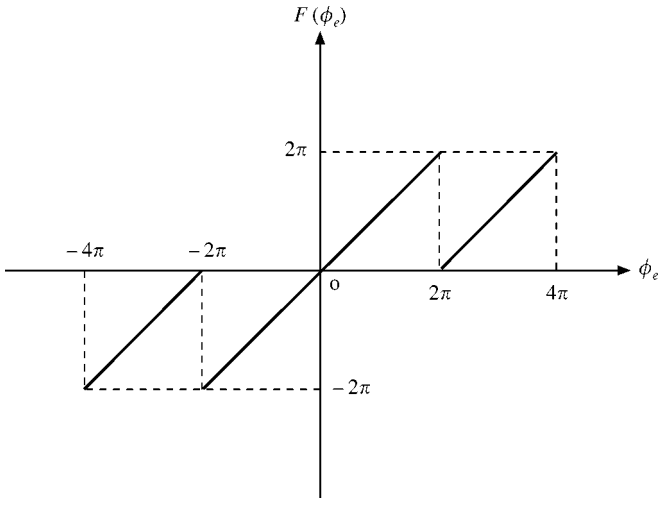

Figure 3. The graph of the average of the non-linear function F corresponding to the PFD.

Then, a useful mathematical model of the NPLL is derived by which the evolution of the frequency-phase error can be determined conveniently.

The components of the NPLL in Figure 2 are described in the following.

2.1. PHASE-FREQUENCY DETECTOR (PFD)

A widely used phase detector is the PFD which has a large acquisition range. The PFD is usually used in charge pump PLLs (see, e.g., references [1, 12, 13]). Having $r(\cdot)$ and $v(\cdot)$ in equations (1) and (2), respectively, the scalar-valued output of the PFD can be written as

$$u(t) = -K_d F(\phi_e(t)) + K_d n_d(t), \tag{5}$$

for all $t \geqslant 0$, where $K_d > 0$ is the PFD gain which depends on the input and output amplitudes (see, e.g., references [1, 12, 13]), $F : \mathbb{R} \to \mathbb{R}$ is a non-linear function, and $K_d n_d(t) \in \mathbb{R}$ is the high-frequency component of the PFD output. The function F has a complicated form in general; however, the graph of its average is that depicted in Figure 3 (see, e.g., references [1, 12, 13]).

2.2. LOOP FILTER (LF)

The LF is a single-input single-output linear system that follows the PFD. This system should be a low-pass filter in order to suppress the high-frequency component of $u(\cdot)$—the second term in equation (5). This is an important role of the LF: the more the high-frequency component of $u(\cdot)$ is suppressed, the better the NPLL performs. The output of the LF filter can be written as

$$y(t) = -K_d h(t) * F(\phi_e(t)) + K_d h(t) * n_d(t), \tag{6}$$

for all $t \geqslant 0$, where $h(\cdot)$ denotes the impulse response of the LF and $*$ denotes the convolution operator.

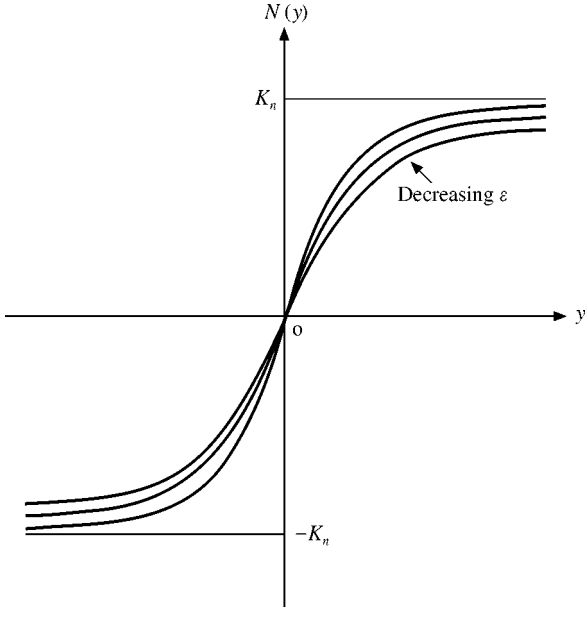

Figure 4. The graphs of the non-linear element N in equation (9). By decreasing ε the slope of N at the origin increases.

A commonly used LF has the transfer function (see, e.g., references [1, 12, 13])

$$H(s) = \frac{1 + \tau_2 s}{\tau_1 s}, \tag{7}$$

for all $s \in \mathbb{C}$, where $\tau_1 > 0$ and $\tau_2 > 0$ are parameters to be determined to make the LF a low-pass filter and achieve certain design objectives. The state space representation of $H(s)$ is

$$\dot{x}(t) = u(t), \quad x(0) =: x_0, \tag{8a}$$

$$y(t) = \left(\frac{1}{\tau_1}\right)x(t) + \left(\frac{\tau_2}{\tau_1}\right)u(t), \tag{8b}$$

for all $t \geqslant 0$. In equations (8), for all $t \geqslant 0$, the state $x(t) \in \mathbb{R}$ and the input $u(t)$ and the output $y(t)$ are those in equations (5) and (6), respectively.

2.3. NON-LINEAR ELEMENT N

The non-linear element N is chosen as one of the following functions:

$$N(y) = K_n \tanh\left(\frac{y}{\varepsilon}\right), \qquad N(y) = \frac{K_n y}{\varepsilon + |y|}, \tag{9a, b}$$

for all $y \in \mathbb{R}$, where $K_n > 0$ and $0 < \varepsilon < 1$. The graphs of N in equations (9) are depicted in Figure 4. It is straightforward to show that by decreasing ε the slope of N at the origin increases.

The scalar-valued output of N is

$$y_N(t) = N(y(t)), \tag{10}$$

for all $t \geqslant 0$. Since for a superior performance ε should be chosen small, the slope of N is large at the origin. Therefore, inputs to N with small amplitudes are amplified significantly. This statement is also true for the high-frequency component of the LF output—the second term in equation (6). Thus, $y_N(\cdot)$ can be quite noisy, and a low-pass filter must be placed after N.

2.4. CONSTANT GAIN Γ

The constant gain $0 \leqslant \Gamma \leqslant 1$ is connected to N in parallel. The importance of Γ is explained later.

2.5. LOW-PASS FILTER $L(s)$

The filter $L(s)$ is a single-input single-output low-pass filter that suppresses the high-frequency component of $y_N(\cdot)$. The transfer function of this filter is

$$L(s) = \frac{1}{1 + s/\alpha}, \tag{11}$$

for all $s \in \mathbb{C}$, where $\alpha > 0$ is the filter cut-off frequency. The state space representation of $L(s)$ is

$$\dot{\zeta}(t) = -\alpha\zeta(t) + \alpha y_N(t), \qquad y_L(t) = \zeta(t), \tag{12a, b}$$

for all $t \geqslant 0$, where the state $\zeta(t) \in \mathbb{R}$ and the output $y_L(t) \in \mathbb{R}$.

2.6. VOLTAGE-CONTROLLED OSCILLATOR (VCO)

The VCO is a special component of PLLs. The input to the VCO is $y_L(\cdot) = \zeta(\cdot)$ in equation (12b). Let

$$\dot{z}(t) := \zeta(t), \tag{13}$$

for all $t \geqslant 0$. With this definition, the output phase is

$$\phi_o(t) = K_o z(t), \tag{14}$$

for all $t \geqslant 0$, where $K_o > 0$ is the VCO gain. The reason for equations (13) and (14) is that there is an integrator in the VCOs which generates the output phase. The output of the VCO is $v(\cdot)$ in equation (2).

Thus far the dynamics of the components of the NPLL are described. Referring to Figure 2 and using equations (5), (8), (9a), (10), (12a), (13), and (14), a *non-linear*

mathematical model of the NPLL can be written as

$$\dot{x}(t) = -K_d F((\omega_o - \omega_i)t + K_o z(t) - \phi_i(t) + \phi_n(t)) + K_d n_d(t), \quad x(0) =: x_0, \tag{15a}$$

$$y(t) = \left(\frac{1}{\tau_1}\right)x(t) + \left(\frac{\tau_2}{\tau_1}\right)[-K_d F((\omega_o - \omega_i)t + K_o z(t) - \phi_i(t) + \phi_n(t)) + K_d n_d(t)], \tag{15b}$$

$$\dot{\zeta}(t) = -\alpha\zeta(t) + \alpha\left[\Gamma y(t) + K_n \tanh\left(\frac{y(t)}{\varepsilon}\right)\right], \quad \zeta(0) =: \zeta_o, \tag{15c}$$

$$\dot{z}(t) = \zeta(t), \qquad z(0) =: z_o = \phi_o(0)/K_o, \tag{15d}$$

for all $t \geqslant 0$. The mathematical model in equations (15) provides a useful and convenient tool for simulating the dynamics of the NPLL and determining its behavior quantitatively. By solving system (15) (numerically), the evolution of the frequency-phase error can be determined via

$$\phi_e(t) = (\omega_o - \omega_i)t + K_o z(t) - \phi_i(t) + \phi_n(t), \tag{16}$$

for all $t \geqslant 0$. As stated earlier, the NPLL achieves locking when $\phi_e(t) \approx 0$ for all t after a finite time $t^* > 0$.

In order to compare the locking capabilities of the NPLL to those of the standard PLL, the mathematical model of the PLL should be simulated along with system (15). This model, which is obtained from equations (15), consists of equations (15a) and (15b) and

$$\dot{z}(t) = y(t), \qquad z(0) =: z_0 = \phi_o(0)/K_o, \tag{17}$$

for all $t \geqslant 0$.

Simulation of the mathematical models of the NPLL and PLL provides evidence that, due to the non-linear element N and the low-pass filter $L(s)$, the NPLL outperforms the standard PLL in achieving locking fast.

It should be pointed out that non-linearities somewhat similar to those in equations (9) are introduced in control laws that achieve robust and simultaneous tracking (locking) for a group of systems in finite time; see reference [14]. Such non-linear control laws are successfully used to control biaxial (also known as XY) positioning tables; see reference [15]. A different NPLL design is proposed in reference [16], where the phase detector is of the multiplier type. The NPLL in reference [16] is the one in Figure 2 with $\Gamma = 0$ and $L(s) = 1$.

3. PERFORMANCE OF THE NPLL

In this section, the performance of the NPLL is examined carefully and is compared to that of the standard PLL.

Let

$$\text{Input frequency} \qquad \omega_i = 200\,000 \times 2\pi \text{ rad/s}, \tag{18a}$$

$$\text{PFD gain} \qquad K_d = 1 \text{ V}, \tag{18b}$$

$$\text{Function } F \qquad \text{Depicted in Figure 3}, \tag{18c}$$

$$\text{Parameters of the LF} \qquad \tau_1 = 500 \times 10^{-6}\,\text{s}, \quad \tau_2 = 50 \times 10^{-6}\,\text{s}, \tag{18d}$$

$$\text{Parameters of the nonlinear element } N \qquad K_n = 1\,\text{V}, \quad \varepsilon = 0{\cdot}1\,\text{V}, \tag{18e}$$

$$\text{Gain of the feedforward loop} \qquad \Gamma = 1, \tag{18f}$$

$$\text{Cut-off frequency of the low-pass filter } L(s) \qquad \alpha = 125\,000\,\text{l/s}, \tag{18g}$$

$$\text{VCO gain} \qquad K_o = 130\,000\,\text{rad/(s V)}. \tag{18h}$$

With this set-up several (numerical) tests are carried out by simulating the mathematical models of the NPLL and PLL.

3.1. TEST 1

Let

$$\text{Output frequency} \qquad \omega_o = 200\,000 \times 2\pi\,\text{rad/s}, \tag{19a}$$

$$\text{Input phase} \qquad \phi_i(t) = 0{\cdot}1 \sin 1000t, \tag{19b}$$

$$\text{High-frequency component of the PFD output} \qquad n_d(t) = \sin(400\,000 \times 2\pi t), \tag{19c}$$

$$\text{Phase noise} \qquad \phi_n(t) = 0{\cdot}001 \sin\,100\,000t, \tag{19d}$$

for all $t \geqslant 0$. With this set-up and the initial conditions $x_o = 0$ and $z_o = 0{\cdot}00001$ s V, equations (15) and (17) are solved numerically to obtain the time histories of the frequency-phase error $t \mapsto \phi_e(t)$ for the standard PLL and NPLL via equation (16). These time histories are depicted in Figure 5. It is evident that the frequency-phase error of the NPLL locks to zero much faster than that of the PLL.

3.2. TEST 2

Let

$$\text{Output frequency} \qquad \omega_o = 180\,000 \times 2\pi\,\text{rad/s}, \tag{20a}$$

$$\text{Input phase} \qquad \phi_i(t) = 0, \tag{20b}$$

$$\text{High-frequency component of the PFD output} \qquad n_d(t) = \sin(380\,000 \times 2\pi t), \tag{20c}$$

$$\text{Phase noise} \qquad \phi_n(t) = 0{\cdot}001 \sin\,100\,000t, \tag{20d}$$

for all $t \geqslant 0$. With this set-up and the initial conditions $x_0 = 0$ and $z_0 = 0$, equations (15) and (17) are solved numerically to obtain the time histories of the frequency-phase error $t \mapsto \phi_e(t)$ for the standard PLL and NPLL via equation (16). These time histories are depicted in Figure 6. It is evident that the frequency-phase error of the NPLL locks to zero much faster than that of the PLL.

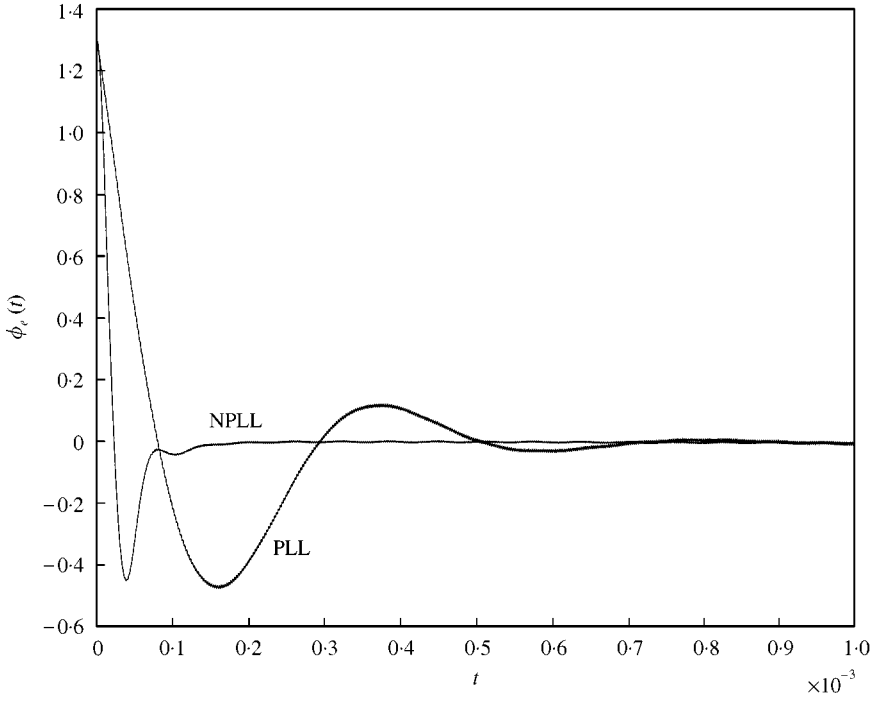

Figure 5. The time histories of the frequency-phase error $t \mapsto \phi_e(t)$ in Test 1. The NPLL achieves locking much faster than the standard PLL.

3.3. TEST 3

Let

$$\text{Output frequency} \qquad \omega_o = 225\,000 \times 2\pi \text{ rad/s}, \tag{21a}$$

$$\text{Input phase} \qquad \phi_i(t) = 0, \tag{21b}$$

$$\text{High-frequency component of the PFD output} \qquad n_d(t) = \sin(425\,000 \times 2\pi t), \tag{21c}$$

$$\text{Phase noise} \qquad \phi_n(t) = 0{\cdot}001 \sin 100\,000t, \tag{21d}$$

for all $t \geqslant 0$. With this set-up and the initial conditions $x_0 = 0$ and $z_0 = 0{\cdot}00001$ sV, equations (15) and (17) are solved numerically to obtain the time histories of the frequency-phase error $t \mapsto \phi_e(t)$ for the standard PLL and NPLL via equation (16). These time histories are depicted in Figure 7. It is evident that the frequency-phase error of the NPLL locks to zero much faster than that of the PLL.

4. USEFUL REMARKS

In this section, some insightful remarks regarding the performance, structure, and applications of the NPLL are given.

(1) The large acquisition range of the NPLL is due to the PFD, which performs better than other types of phase detectors; see, e.g., references [1, 12, 13] for a detailed discussion.

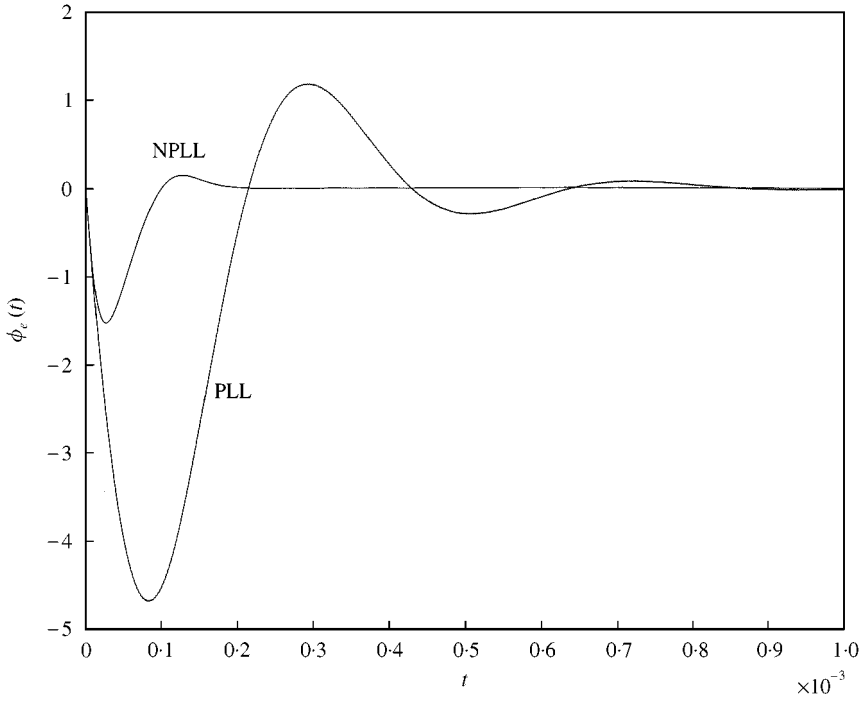

Figure 6. The time histories of the frequency-phase error $t \mapsto \phi_e(t)$ in Test 2. The NPLL achieves locking much faster than the standard PLL.

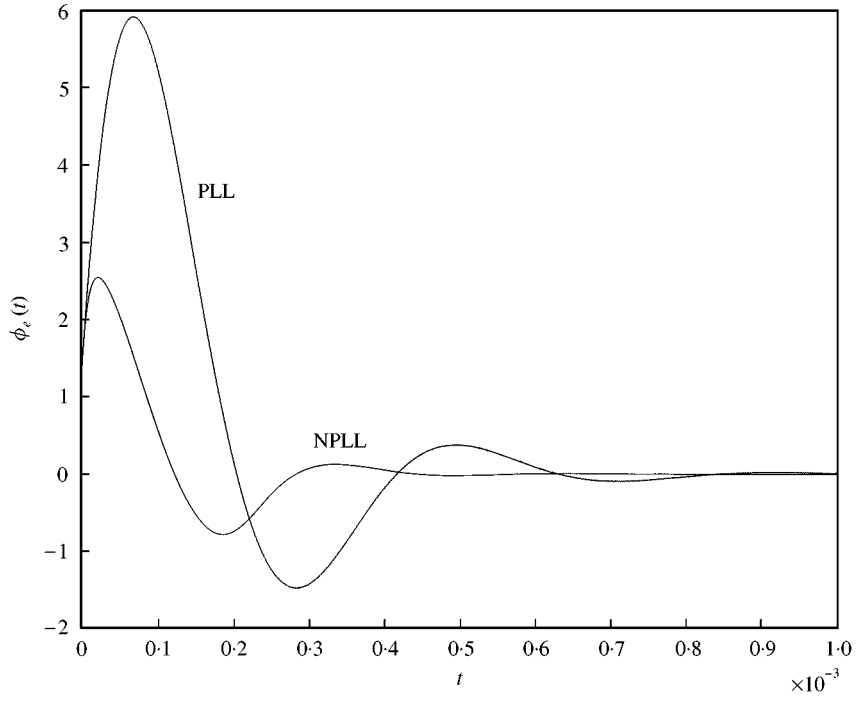

Figure 7. The time histories of the frequency-phase error $t \mapsto \phi_e(t)$ in Test 3. The NPLL achieves locking much faster than the standard PLL.

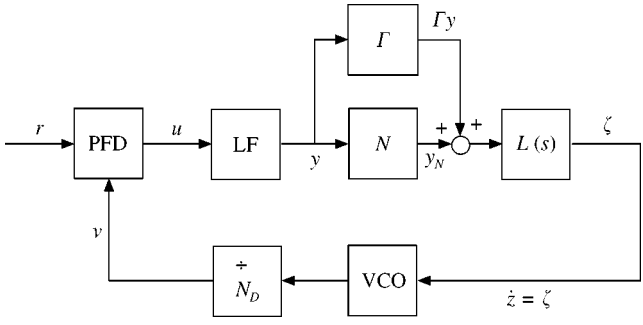

Figure 8. A frequency synthesizer made based on the NPLL. A divider with the dividing factor N_D succeeds the VCO.

(2) Let the loop containing the constant gain Γ be disconnected. In this case, the NPLL with the non-linear element N performs very well in locking the frequency-phase error $\phi_e(\cdot)$ to zero fast, when $|\omega_o - \omega_i|$ is small. However, it performs poorly in locking $\phi_e(\cdot)$ to zero when $|\omega_o - \omega_i|$ is large, such that locking may not be achieved at all. Next, let the loop containing Γ be connected, set $\Gamma = 1$ and $L(s) = 1$, and let the loop containing N be disconnected. In this case, the NPLL, which becomes the standard PLL, locks $\phi_e(\cdot)$ to zero even when $|\omega_o - \omega_i|$ is large; however, it cannot do so fast. Thus, both N and Γ connected in parallel are necessary to guarantee that the NPLL has a large acquisition range and achieves locking very fast.

(3) The non-linear element N can be realized as an integrated circuit; see, e.g., reference [13, p. 14] for such a realization.

(4) The PFD in the NPLL in Figure 2 can be replaced by other types of phase detectors. For different phase detectors, $0 \leqslant \Gamma \leqslant 1$ and $L(s)$ should be retuned. For instance, if a phase detector of the multiplier type replaces the PFD, then Γ should be set equal to zero.

(5) A synthesizer can be made based on the NPLL. Such a synthesizer is shown in Figure 8. The synthesizer is essentially the NPLL in which a divider with the dividing factor N_D succeeds the VCO. The synthesizer achieves locking when

$$\frac{\omega_o t + \phi_o(t) + \phi_n(t)}{N_D} \approx \omega_i t + \phi_i(t), \tag{22}$$

for all t after a finite time $t^* > 0$.

5. CONCLUSIONS

In this note, a novel phase-locked loop (PLL) is introduced. The proposed PLL, denoted by NPLL, incorporates a non-linear element and a low-pass filter in its loop. The NPLL performs extremely well: it has a large acquisition range and achieves locking fast. In particular, it outperforms the standard PLL in achieving locking fast. The superior performance of the NPLL is due to the phase-frequency detector (PFD), the non-linear element and the constant gain connected to it in parallel, and the low-pass filter following them. The addition of the low-pass filter is necessary in order to remove the excessive noise from the output phase. Results of many tests, only three of which are reported in this note, show the superior performance of the NPLL. A synthesizer based on the NPLL is also proposed.

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