Available online at www.sciencedirect.com
ScienceDirect
Thermochimica Acta 455 (2007) 95–99
thermochimica acta
www.elsevier.com/locate/tca

Thermal analysis of high power GaN-based LEDs with ceramic package

Lianqiao Yang, Sunho Jang, Woongjoon Hwang, Moowhan Shin *

Department of Materials Science & Engineering, Myong Ji University, Yongin 449-728, Republic of Korea

Available online 30 November 2006

Abstract

In this paper we present thermal analysis of three kinds of ceramic package designs for high power LEDs. The analysis was made by transient thermal measurement and thermal simulation using the Finite Volume Method. The three ceramic packages under investigation employ same configuration of GaN-based chip, but they have different size and distribution of thermal vias. Three designs of LED packages resulted in significantly different thermal behaviors. Thermal behaviors, described as thermal resistance, of the three packaging designs were compared and evaluated as functions of bulk thermal resistance, spreading resistance, and surface roughness. The deviation between the simulated results and measured data were attributed to the different surface roughness in the interfaces between the packaging components. It was demonstrated that the junction temperature decreases with the effective contact area ratio in the LED packages.

Keywords: Light emitting diode (LED); Ceramic package; Transient thermal resistance; Finite volume method (FVM); Spreading/constriction resistance; Contact thermal resistance

1. Introduction

High power GaN-based light emitting diodes (LEDs) keep attracting researchers' interests due to their significant impacts on solid-state illumination industry. However, thermal problem is still a bottleneck to limit the stability, reliability, and lifetime of LEDs [1–4]. Therefore, effective thermal design LED packages with low thermal resistance is critical to improve the performance of LEDs [5].

It is known that there are two general design rules for the high power operation of LED; one is the size and distribution of heat slug and the other is the thermal conductivity and shape of package mold. Changing heat slug size changes the heat path and the spreading/constriction thermal resistance has to be taken into consideration [6,7]. The package materials for the LEDs must fulfill various requirements, including high thermal conductivity, high mechanical strength and stiffness, and high chemical inertness. One of important package materials of LEDs is the epoxy resin with easiness of processing in mold [8]. However, the disadvantages of the epoxy resin are lack of chemical stability, moisture-proof ability, and relatively bad thermal properties which can limit inherent performance of LED chips. Ceramic materials with high thermal conductivity, good environment stability, and high moisture-proof ability have been widely used in modern electronic packaging [9] and can be regarded as a primary candidate for a package material of high power LEDs.

In this paper, we investigated the thermal behavior of three types of ceramic package designs for high power LEDs with different size and distribution of thermal vias. The investigation was made by the transient thermal measurement [10] and thermal simulation with commercialized finite volume method (FVM) program, FLOTHERM. The effective contact area in the package design was correlated with the thermal performance of the LED. The simulation results were compared with the experimental data and the implication is discussed.

2. Transient thermal measurement

Three types of ceramic package designs for the high power GaN-based blue LEDs were investigated. The schematic of the LED packages is shown in Fig. 1. Type I has a single silver thermal via with a diameter of 1.47 mm, type II has 16 thermal silver vias with a diameter of 0.43 mm. Type III has an upper layer with 16 thermal vias in a diameter of 0.26 mm and a lower layer with 9 thermal vias in a diameter of 0.5 mm. The two layers are connected with Ag plate with a thickness of 0.02 mm.

Transient thermal measurements with Transient Thermal Tester (T3Ster, MicReD Ltd.) were performed to investigate the thermal behavior of the LED packages. T3Ster captures the thermal transients in real time, records the cooling/heating curve. It

* Corresponding author. Tel.: +82 31 330 6465; fax: +82 31 330 6457.
E-mail address: mwshin@mju.ac.kr (M. Shin).

0040-6031/$ – see front matter © 2006 Elsevier B.V. All rights reserved.
doi:10.1016/j.tca.2006.11.019

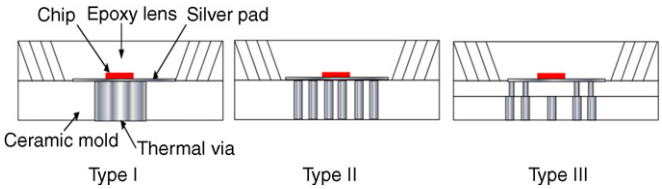

Fig. 1. Schematic of three types of ceramic package designs.

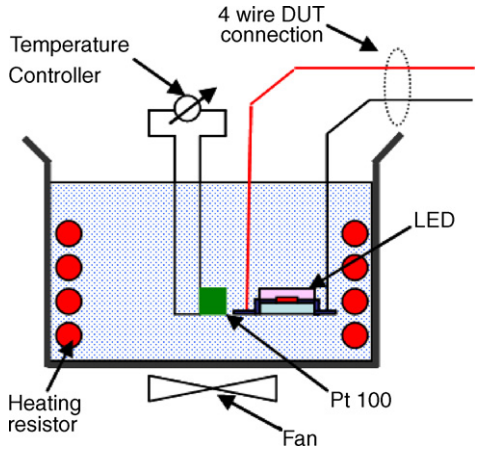

Fig. 2. Schematic of experimental set up for calibration in a liquid bath.

evaluates the cooling/heating curve to derive the thermal characteristics. Based on the thermal R–C network and structure function theory, the heat path can be determined quantitatively [11,12]. The measurement was made in the following procedures. The first step was to get the K factor, a ratio between the forward voltage and the junction temperature change, which is known as a temperature sensitive parameter (TSP). All the thermal measurements were made in liquid bath as shown in Fig. 2. For the K factor calibration, 10 mA sensor current was used in the temperature range of 20–50 °C with an increasing step of 10 °C. The thermal resistance was measured after driving the samples with 350 mA current for 10 min at the liquid temperature of 25 °C. The extracted input powers from experiment were 1.139 W, 1.123 W, and 1.136 W for the package types I, II, and III, respectively.

3. Analytical and numerical simulations for LEDs

Thermal modeling of the LED packages was done in FLOTHERM. FLOTHERM includes a computational fluid dynamics (CFD) solver, which carries out a full 3D solution of the Navier–Stokes equations for mass, momentum and energy conservation using the finite volume technique. The conservation equations in the general form are as follows for mass, momentum, and thermal energy, respectively [13]:

$$\left[\frac{\partial \rho}{\partial t} + v \cdot \nabla \rho\right] = -\rho \nabla \cdot v \tag{1}$$

$$\rho\left[\frac{\partial v}{\partial t} + v \cdot \nabla v\right] = -\nabla p + \rho g - \left(\frac{2}{3}\right) \cdot \nabla(\mu \nabla \cdot v) + 2\nabla \cdot (\mu S) \tag{2}$$

$$\rho c_P \left[\frac{\partial T}{\partial t} + v \cdot \nabla T\right] = \nabla \cdot (K \nabla T) - \left(\frac{2}{3}\right) \cdot \mu(\nabla \cdot v)^2 + 2(\mu S : S) + \beta T \cdot \frac{Dp}{Dt} \tag{3}$$

where ρ is the density, v the velocity vector, p the pressure, t the time, g the gravity, μ the viscosity, k the thermal conductivity, S the strain rate tensor, T the absolute temperature, and β is the expansiveness.

The modeled LED packages have the same dimensions as the real packages. The package is composed of GaN blue chip, silicon die attach, lead frame, ceramic mold, silver thermal vias, and epoxy lens as shown in Fig. 1. Detailed structure of epilayers in the chip was simplified and the effect of gold wire was not considered in modeling. Thermal conductivities of employed packaging materials are listed in Table 1. Thermal conductivities are assumed to be independent of temperature due to relatively small temperature change during the whole experiment procedure.

As a boundary condition during thermal simulation, heat transfer coefficient (h, W/m^2 °C) is important to ensure the accurate result [14]. In our simulation, heat transfer coefficient was calculated by FLOTHERM based on CFD, and parameters of the liquid oil, instead of air, using in the measurement was input in FLOTHERM. The thermal conductivity, viscosity, and density of the liquid oil are 0.11 W/m °C, 3.88 mPa s, and 900 kg/m^3, respectively. The heating power extracted from the experiment was used for the simulation process. The temperature of the liquid oil was set to 25 °C as in the measurement.

4. Results and discussion

The K factors were calculated based on Eq. (4) and the results for the three types of packages are shown in Fig. 3. The obtained K factors are 1.543 mV/°C, 1.485 mV/°C, and 2.053 mV/°C for package types I, II, and III, respectively.

$$K = \frac{\Delta D_{TJ}}{\Delta D_{VF}} \tag{4}$$

Table 1
Thermal conductivity of LED packaging materials

	Material				
	GaN chip	Silicon die attach	Ceramic mold	Silver thermal via and lead frame	Epoxy lens
Thermal conductivity (W/m °C)	65.6	0.2	3	400	0.68

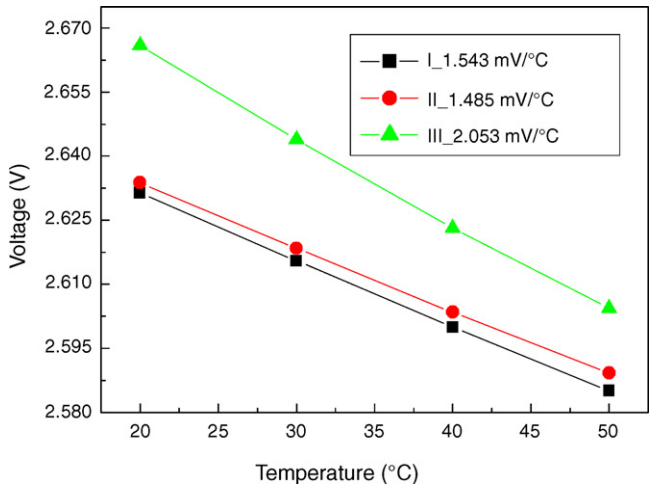

Fig. 3. Forward voltage vs. temperature plot for the calculation of the *K* factor.

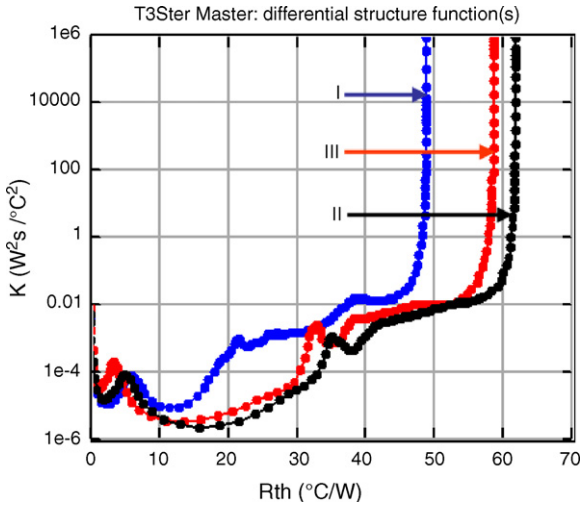

Fig. 4. Differential structure functions for package types I, II, and III.

where ΔD_{TJ} is the change of junction temperature of LED, and ΔD_{VF} is the change of forward voltage in LED.

The structure functions obtained from the transient thermal measurement were shown in Fig. 4. And the simulation result of type I obtained from FLOTHERM was shown in Fig. 5. Under the same conditions, the measured thermal resistances were 48.9 °C/W, 61.8 °C/W, and 58.5 °C/W for the package types I, II, and III, respectively. And calculated thermal resistances from the simulation were 45.5 °C/W, 49.8 °C/W, and 57.2 °C/W, respectively. From both the experiment and the simulation results, we can find that the package type I exhibits the best thermal performance. However, different from the simulation result, the experimental results indicate a higher thermal resistance from the type II than that from type III. The disagreement can be explained by a thorough analysis of structure of thermal vias and their effective contact areas with heat sink.

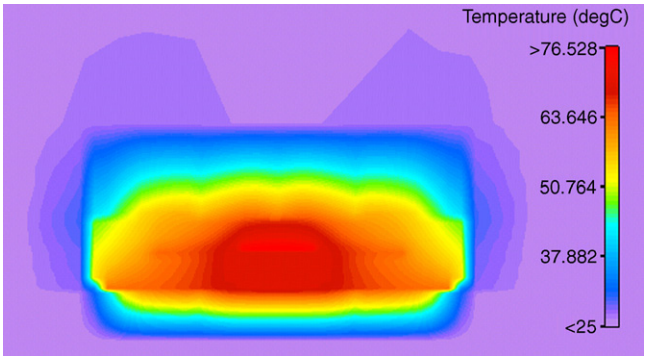

Fig. 5. Simulated temperature distribution of LED package (type I) at 350 mA.

For the three kinds of package design, the main difference is the size and distribution of thermal vias as shown in Fig. 1. The thickness of the thermal vias are 0.44 mm, 0.56 mm, for type I and type II packages, respectively, and 0.23 mm and 0.31 mm for the first layer and the second layer of type III package. The total areas of thermal vias are 1.70 mm^2, 2.28 mm^2 for type I and II, respectively, and 0.85 mm^2 and 1.77 mm^2 for the first layer and the second layer of type III. As the silver has much higher thermal conductivity than ceramic mold and epoxy lens, it is reasonable to regard the thermal vias as a main path for heat dissipation generated from the p–n junction of a chip. We may expect a decreasing thermal resistance from type III to type I to type II if we only consider the thermal resistance of the bulk material that can be calculated with Eq. (5).

$$R_{th} = \frac{t}{(K \cdot A)} \tag{5}$$

where R_{th} is the thermal resistance, t the thickness, K the thermal conductivity and A is the cross-sectional area. We also need to investigate the contribution of spreading thermal resistance to the total thermal resistance of package. When the heat flows across an interface between two components with different areas, constriction/spreading thermal resistance should be considered [6,7] as was described in Fig. 6. The parameters "*a*" and "*b*" are radius or equivalent radius of two different parts with different sizes. The "*q*" is the heat flux passing through the heat path from "*a*" to "*b*", "*t*" the thickness of the bigger part in the heat path. Here we define contact area ratio as *a*/*b*. The term, constriction, is used to describe the case where heat flows into a narrower region (area ratio smaller than 1), and spreading is used to describe the opposite case. In this study, only constric-

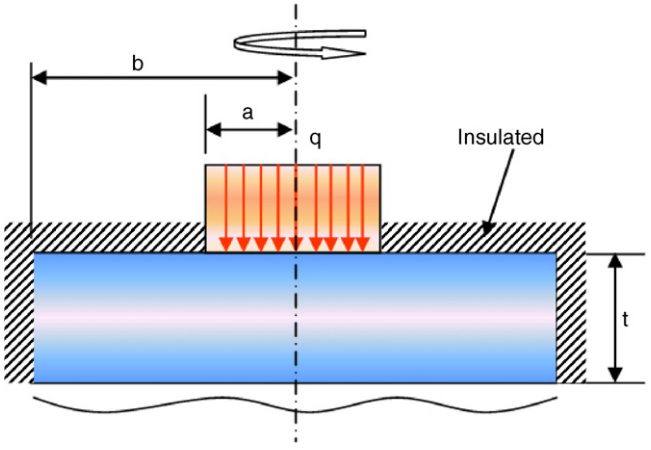

Fig. 6. Thermal modeling of spreading resistance.

tion resistance between the silver pad and via was considered, because the spreading condition is the same for the three cases.

It has been known that the constriction/spreading thermal resistance can be expressed in the following equation [6].

$$\varphi_{ave}(\varepsilon, \tau) = \frac{4}{\sqrt{\pi\varepsilon}} \sum_{n=1}^{\infty} \frac{J_1^2(\lambda_n \varepsilon)\ \tanh(\lambda_n \tau)}{\lambda_n^3 J_0^2(\lambda_n)} \quad (6)$$

where φ_{ave} is the average dimensionless constriction resistance, ε the dimensionless contact area ratio, a/b, τ the dimensionless plate thickness t/b, $J_i(\cdot)$ the Bessel function of the first kind of order I, λ_n the eigenvalue, a, b and t have the same meaning as they are in Fig. 6.

Type II package has 16 thermal vias, so the total constriction resistance should be equal to one constriction resistance divided by 16 since they are thermally in parallel. Type III package has 16 thermal vias in the first layer, and exhibits negligible spreading resistance from first layer to the second layer, as the area ratio is 0.52 and there are 9 thermal vias in parallel. The area ratio between the thermal via and the silver pad are 0.317, 0.027, and 0.01 for package of types I, II, and III, respectively. The constriction thermal resistance from silver pad to thermal via can be calculated by substituting the corresponding contact ratio values into Eq. (6) [6]. And the calculated constriction resistances are 0.24 °C/W, 2.36 °C/W, and 2.41 °C/W for package of types I, II, and III, respectively. As type I package has a single thermal via with a comparable size with the chip size, the constriction thermal resistance of type I is much smaller than types II and III. It is a main reason that type I package resulted in the lowest thermal resistance both in simulation and experiments.

The package type II has a smaller constriction thermal resistance than that of type III, which is a different result from the measurement (Fig. 4). Observation of the contact area between the chip and thermal vias explains the experimental results and clearly demonstrates the significant effect of it on thermal performance of LED package. Fig. 7 is a micrograph of thermal vias in contact with chips for the three different packages. The dotted square is the contact area with chip. It is clearly shown that the contact surface of type II package is with significant roughness compared with other packages. The four thermal vias were designed to be under the chip through thin layer of silver pad with thickness of 80 μm. In addition, one of the thermal vias does not seem to make a physical contact with chip, which does not contribute to an effective heat path. It is worth while noting that the surface roughness is not considered in simulation and results in deviation from the experimental data.

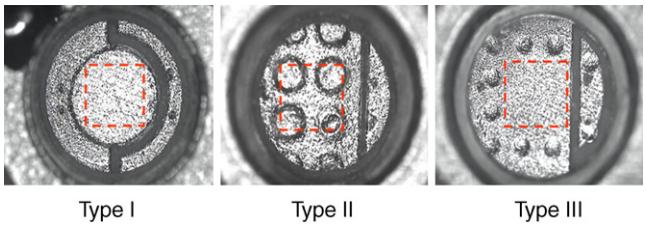

Fig. 7. Micrographs of contact surface of three types of LED packages.

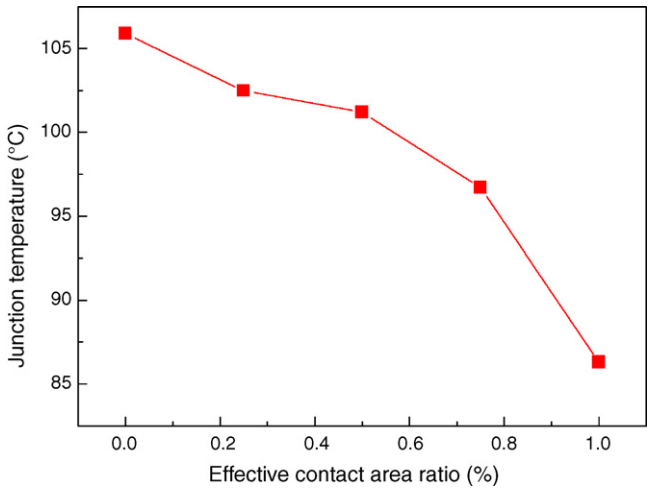

Fig. 8. Junction temperature as a function of effective contact area ratio (type II package).

In order to verify the effect of surface roughness, additional simulation was performed. It was assumed that the contact area is perfectly flat and the contact area is proportional to the number of thermal vias. The boundary condition was set to be same as the earlier simulation. As shown in Fig. 8, the junction temperature, and thus thermal resistance, decreases with the effective contact area. The results demonstrate that the effective surface area is one of important design parameters that must be considered for a reliable thermal simulation for high power LED packages.

5. Conclusion

In this paper, three types of ceramic packaging designs for high power LED were analyzed by transient thermal measurement and simulation. The total thermal resistance is not just determined by the volume ratio of the high thermal conductivity material. It was observed that the constriction thermal resistance and effective contact thermal resistance (related with surface roughness) have great effects on the total thermal resistance of the LED packages. The low constriction thermal resistance by the good distribution of thermal via made the total thermal resistance relatively low. High contact thermal resistance by the rough contact surface induced in the manufacturing process made the higher total thermal resistance. It has been demonstrated that the thermal contact resistance is one of important design parameters for a reliable thermal simulation of LED packages.

Acknowledgement

This work was financially supported by the Korean Institute of Industrial Technology Evaluation and Planning.

References

[1] N. Narendram, Y. Gu, J. Display Technol. 1 (2005) 167.
[2] J. Hu, L. Yang, W.J. Hwang, M.W. Shin, J. Cryst. Growth 288 (2006) 157.
[3] D.A. Jeannotte, L.S. Goldmann, R.T. Howard, R.R. Tummula, E.J. Rymaszewski (Eds.), Microelectronics Packing Handbook, Van Nostrand Reinhold, New York, 1989.

[4] D. Suhir, IEEE Trans. Comput. Hybrids Manuf. Technol. 13 (1990) 940.
[5] B.S. Siegal, Electronics 51 (1978) 121.
[6] S. Lee, S. Song, V. Au, K.P. Moran, Proceedings of the ASME/JSME Thermal Engineering Conference, vol. 4, Boston, MA, September, 1995, pp. 199–206.
[7] M. Grujicic, C.L. Zhao, E.C. Dusel, Appl. Surf. Sci. 246 (2005) 290.
[8] T.M. Alander, P.A. Heino, E.O. Ristolainen, J. Electron. Packaging 125 (2003) 313.
[9] Md. Yusoff, S.C. Noor, L.E.N. Tam, S. Lim, J. Jana, Mater. Proc. Technol. 42 (1994) 95.
[10] G. Farkas, Q. van Voorst Vader, A. Poppe, G. Bognár, IEEE Trans. Comp. Packaging Technol. 28 (1) (2005) 45.
[11] W.J. Hwang, P. Szabo', G. Farkas, M.W. Shin, Proceedings of the 10th International Workshops on Thermal Investigations of ICs and Systems (THERMINIC), Sophia Antipolis, France, September, 2004, pp. 91–95.
[12] V. Sze'kely, T. Van Bien, Solid State Electron. 31 (1988) 1363.
[13] J. Wakil, Microelectron. Reliab. 46 (2006) 380.
[14] T.H. Lee, L. Kim, W.J. Hwang, C.C. Lee, M.W. Shin, Phys. Stat. Sol. (b) 241 (12) (2004) 2681.