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# The performance of compact thermal models for LED package

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ABSTRACT

A method for creating compact thermal models of single-chip and multi-chip LED package is developed and evaluated with good agreement between the finite volume simulation and experimental data. The different compact thermal models for LED package are checked against detail model under 38 boundary conditions. The junction temperature predictions from the single-thermal-resistance model are within 16% for all boundary conditions. And the star-thermal-resistance model gives the most consistent and accurate prediction for the junction temperature, within 5% for all boundary conditions. Based on creating star-thermal-resistance model of single-chip LED package, the compact thermal model of multi-chip LED package is established, in which interacting thermal resistance is taken into account because of the thermal coupling effect between the chips.



## 1. Introduction

As the demands for light output increase, the driving power of the LED package increases continuously. Correspondingly heat dissipation of LED has become more and more important because of its great influence on electrical characteristics, optical characteristics, and reliability [1–4]. If the heat generation inside the LED package cannot be efficiently dissipated, the property of LED will be unstable. The thermal property of LED is usually characterized by thermal resistance, which is determined by the difference of temperature between the junction and the referent node and the power dissipated on it according to JEDEC51-1. Currently, there are several models to predict the junction temperature. The single-thermal-resistance model is limited to predict the junction temperature for a variety of boundary conditions. The junction temperature of LED can be accurately captured by the detail thermal model with sufficient geometric details [5]. Due to the huge computational requirements, it is time-consuming and cost-inefficient for detail thermal model with finite volume method (FVM). Typically, the reduced order modeling such as Proper Orthogonal Decomposition (POD), Fourier Series Expansion, Green Function, can generate a highly accurate full field solution. While the compact modeling such as thermal resistance network can only generate partial information (e.g. $T_J$). The compact thermal model is a reduced order network model comprising a limited number of thermal resistances that connects the junction node to the outer parts of the device. It can accurately predict the junction temperature at different levels [6].

There are some reports on the compact thermal model of single-chip and multi-chip electronic devices. Huang and co-workers presented a compact thermal modeling approach for single-chip device, which was fully parameterized according to design geometries and material physical [7]. Celo and co-workers presented how a reduced parameterized thermal model of multi-chip electronic device can be created based on a parametric model. Many works had not undertaken to generate compact thermal model grounding on the optimization of a resistance network [8,9]. So far, there still has been no report about the application of compact thermal model on LED package.

The heat generated by the active layer of LED is first conducted to the heat sink via chip, and then to MCPCB, at last, dissipated out to the ambient by convection. Strictly speaking, there is also part of heat dissipated via surrounding leadframe, epoxy and lens, but the thermal conductivities of epoxy are so small that such heat dissipation can be ignored without bring much error. Based on the finite volume simulation, we found that approximately 90% of the total heat generated in the active layer was dissipated to the ambient through the metal heat sink. In other words, the remaining portion of the heat was dissipated to the ambient through the other heat flow paths. Until now, the junction temperature of LED package is mainly investigated by the one-dimensional heat flow path, but the accuracy is very limited. Hence, it is essential to develop compact thermal model for accurate prediction of junction temperature. This paper concentrates on the establishment of compact thermal model for both single-chip and multi-chip package, and the capture of 3D heat contribution in LED package. The thermal characteristic of multi-chip LED package is quite different from the single-chip LED package. Currently, there are two different thermal resistance network approaches to predict the junction temperature

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of multi-chip device packages [10]. One method is the average junction-to-ambient thermal resistance defined by Cohen [11].

$$R_{\text{JA-avg}} = \frac{T_{\text{J,avg}} - T_{\text{amb}}}{Q} \tag{1}$$

where $R_{\text{JA-ave}}$ is average junction-to-ambient thermal resistance, $T_{\text{J,avg}}$ is the average junction temperature of multi-chip package, $T_{\text{amb}}$ is the ambient temperature, and $Q$ is the total heat dissipation of multi-chip package. However, the junction temperature of each chip will be largely different if the chips are different in terms of geometry and power dissipation. The junction temperature of some chips will be underestimated by the average junction-to-ambient thermal resistance. The other method is to define the junction-to-ambient thermal resistance on the basis of chip location:

$$R_{\text{JA-}i} = \frac{T_{\text{J},i} - T_{\text{amb}}}{q_i} \tag{2}$$

where $R_{\text{JA-}i}$ is chip-location junction-to-ambient thermal resistance, $T_{\text{J},i}$ is the junction temperature of $i$th chip, $T_{\text{amb}}$ is the ambient temperature, and $q_i$ is the heat dissipation of $i$th chip. The disadvantage of this method is obvious, when one chip is not powered on, but with the neighboring chips powered on, the neighboring chips will heat up the unpowered chip, so the thermal resistance of the unpowered chip would be infinite in terms of Eq. (2). It is of course not true. Therefore, the definition of $R_{\text{JA-}i}$ is not appropriate. The reason is that both methods do not consider the effect of thermal coupling between chips. When the chips operate, the heat flow will influence the temperature of any other chip in the package. It is rather complicated because of the interaction between the temperature rise and the heat transfer among the chips. So it is important to understand the interacting thermal resistance between chips so as to accurately predict the junction temperature of multi-chip module.

In this paper, we established series of compact thermal models for LED package under 38 boundary conditions, which comprise virtually the entire field of realistic environments a package could meet. The temperature and heat flow through each side were calculated by the detail finite volume model in FLOTHERM. The interacting thermal resistance between chips is considered because of thermal coupling effects in multi-chip package. According to temperature and heat flow distribution in the LED package and by changing the resistance minimal cost function and required accuracy, the compact thermal models independent of the imposed boundary conditions are obtained.

## 2. Analytical and simulation compact thermal model for LED package

The compact thermal model is commonly referred to as a "star network". Fig. 1 shows a star-shaped thermal resistance network with convective links to the environment. Fig. 2 shows a typical LED package and its corresponding star thermal network. In this model, the heat flow of the junction equals:

$$q = \sum_{i=1}^{n} \frac{T_{\text{J}} - T_i}{R_i} \tag{3}$$

$$q_i = h_i A_i (T_i - T_0) \tag{4}$$

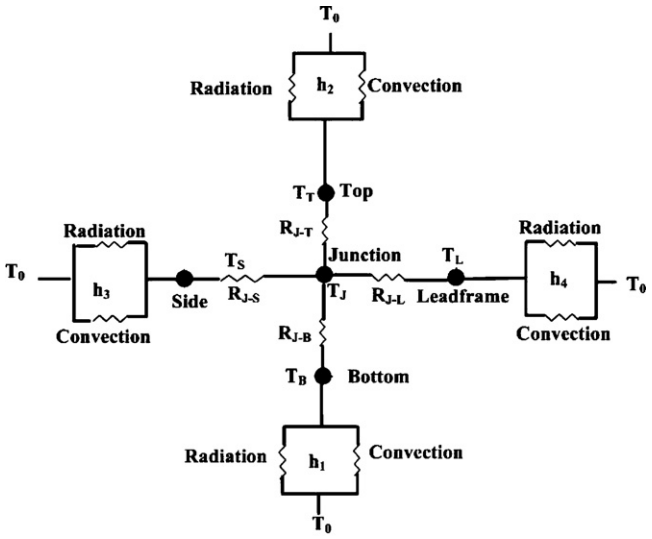


**Fig. 1.** Star-shaped thermal resistance network with convective and radiative links to the environment.

where $R_i$ is the thermal resistance of the $i$th node, $q_i$ is the heat dissipation of the $i$th node, $q$ is the total heat dissipation of active layer, $A_i$ is the surface area of $i$th node, $h_i$ is the heat transfer coefficient of $A_i$, $T_{\text{J}}$ is the junction temperature, $T_i$ is the temperature of $i$th node, and $T_0$ is the ambient temperature. The nodal energy balance equations applied to Fig. 1 lead to

$$\begin{bmatrix} 1/R_1 + 1/R_2 + 1/R_3 + 1/R_4 & -1/R_1 & -1/R_2 & -1/R_3 & -1/R_4 \\ -1/R_1 & 1/R_1 + h_1A_1 & 0 & 0 & 0 \\ -1/R_2 & 0 & 1/R_2 + h_2A_2 & 0 & 0 \\ -1/R_3 & 0 & 0 & 1/R_3 + h_3A_3 & 0 \\ -1/R_4 & 0 & 0 & 0 & 1/R_4 + h_4A_4 \end{bmatrix} \begin{bmatrix} T_{\text{J}} \\ T_1 \\ T_2 \\ T_3 \\ T_4 \end{bmatrix} = \begin{bmatrix} q \\ T_0h_1A_1 \\ T_0h_2A_2 \\ T_0h_3A_3 \\ T_0h_4A_4 \end{bmatrix} \tag{5}$$

The nodal temperatures and heat flow can be easily obtained by finite volume simulation. Thus the thermal resistance of star network can be calculated by Eq. (5). The junction temperature is then calculated using both the detail finite volume model and compact thermal model for each combination of 38 boundary conditions. The junction temperature of compact thermal model for 38 boundary conditions will produce 38 sets of errors, comparing with that of detail finite volume model. To express all of these errors, the following cost function is introduced:

$$Sum\_Cost = \sum_{i=1}^{38} \left[ \frac{T_{\text{J}}^{\text{CM}}(i) - T_{\text{J}}^{\text{FVM}}(i)}{T_{\text{J}}^{\text{FVM}}(i)} \right]^2 \tag{6}$$

To further refine the compact thermal model, the area of compact thermal model is divided into central and remaining part. The thermal resistance, the ratio of central/total area and topology of compact thermal model are optimized for the cost function. With minimal cost function the best compact thermal model can be obtained. It should be noted that reducing the number of nodes in the compact thermal model may cause less accurate. In general, the number of nodes required for getting an accurate compact thermal model depends on the complexity of package.

Based on the compact thermal model of single-chip LED package, we further established the compact thermal model of multi-chip LED package, in which the thermal coupling effect between chips was taken into account. In general, multi-chip package is totally represented by its thermal resistance matrix in the form shown by Eq. (7). $\theta_{\text{JC}}^{nm}$ $(n \neq m)$ in the thermal resistance matrix represents interacting junction-to-case thermal resistance

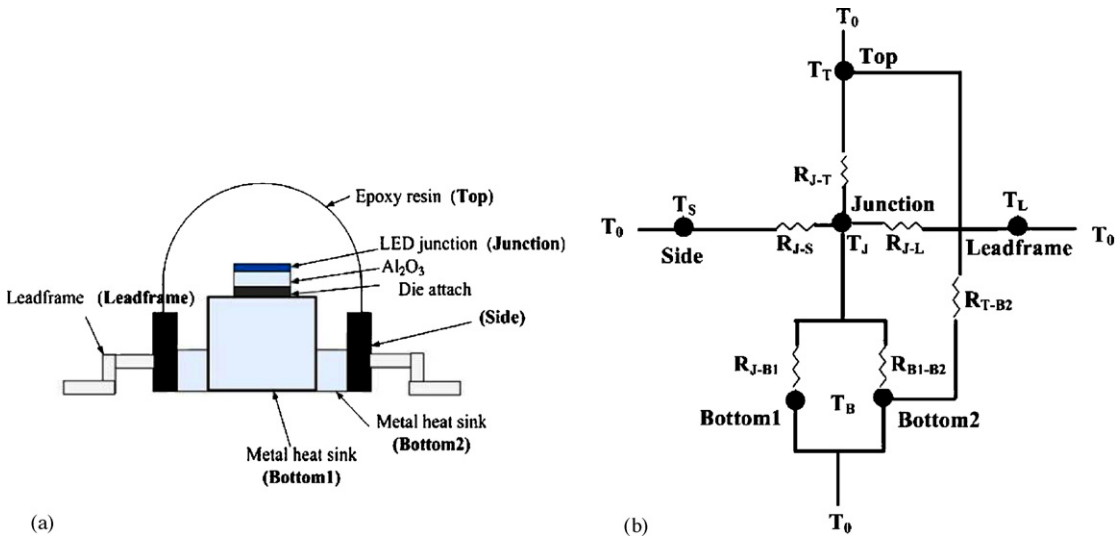


**Fig. 2.** (a) The schematic structure of the LED package and (b) equivalent thermal resistance model for LED package.

between node $n$ and $m$, $\theta_{JC}^{nm}$ describes the self-thermal resistance of the $n$th chip. Multiplying this matrix with vector of combination of $Q_n$ powers applied at the chips, the corresponding junction temperature of all chips can be obtained. $T_C$ is the case temperature of multi-chip package. $T_{Jn}$ is the junction temperature of the $n$th chip.

$$\begin{bmatrix} \theta_{JC}^{00} & \theta_{JC}^{01} & \cdots & \theta_{JC}^{0n} \\ \theta_{JC}^{10} & \theta_{JC}^{11} & \cdots & \theta_{JC}^{1n} \\ \vdots & \vdots & \ddots & \vdots \\ \theta_{JC}^{n0} & \theta_{JC}^{n1} & \cdots & \theta_{JC}^{nn} \end{bmatrix} \begin{bmatrix} Q_0 \\ Q_1 \\ \vdots \\ Q_n \end{bmatrix} + T_C = \begin{bmatrix} T_{J0} \\ T_{J1} \\ \vdots \\ T_{Jn} \end{bmatrix} \tag{7}$$

With $n$ chips in a package, there are $n^2$ thermal resistances present. $n$ self-thermal resistances describe the heat-removal properties from the junction on a chip towards the case. For every chip, there are $n-1$ thermal resistances that represent the effect of thermal coupling from the driven chip to any other chip in the package. The thermal resistance matrix shall be calculated by $n$ thermal simulation. All the thermal resistances of multi-chip model can be obtained by Eq. (7) with the junction temperature and heat flow of chips recorded after simulation.

## 3. Experiments

The thermal behavior of the single-chip and multi-chip LED package were investigated by Transient Thermal Tester (T3Ster, MicRed Ltd.). The optical power of LED was obtained by TERALED. The theoretical framework of evaluation of T3Ster was based on the distribution RC networks [12,13]. T3Ster captured the thermal transient response in real time, recorded the cooling/heating curve and then evaluated the cooling/heating curve to derive the thermal characteristics [14,15]. For temperature sensitive parameter calibration, 1 mA sensitive current was applied in the temperature range of 25–55 °C with an increment of 10 °C. Transient thermal measurement was started to record the cooling curve after driving the single-chip LED package with 350 mA current for 1 min with heatsink temperature kept at 25 °C. One-chip package, two-chip package, and three-chip package were driven by 350 mA, 700 mA, and 1050 mA for 1 min with heatsink temperature kept at 25 °C, respectively.

## 4. Results and discussion

The detail finite volume model of single-chip LED package was created by FLOTHERM. The detail model represents each of the

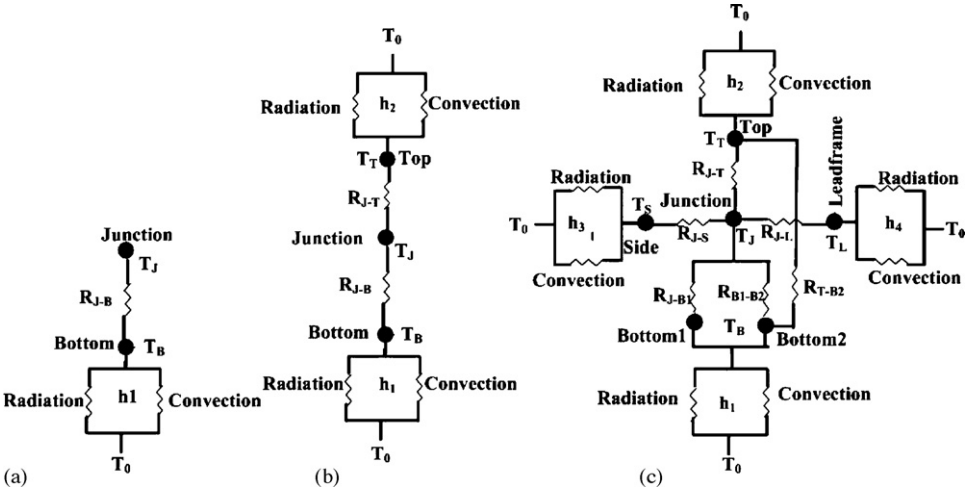


**Fig. 3.** Nodes of the different thermal resistance model with links to environment: (a) one-thermal resistance model; (b) two-thermal resistance model; (c) star-thermal resistance model.

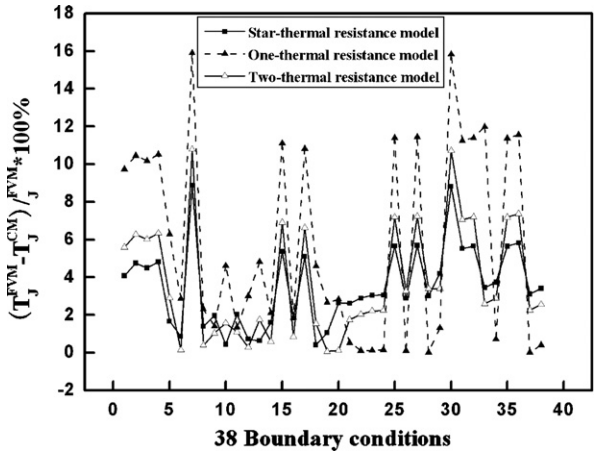


**Fig. 4.** Junction temperature difference between detail and compact thermal model under 38 boundary conditions.

following package, including sub-elements explicitly the die, substrate, die attach, metal heat sink, adhesive, MCPCB, leadframe, silica gel and epoxy resin. Fig. 2(a) shows the schematic structure of the LED package. The junction temperature is 48.3 °C under the simulation with 0.94 W power consumption of chip, rather good agreement with the 47.3 °C experimental measurement. Provided the detail model is correctly validated using the measured data, the detail model can be regarded as accurately representing the package. And then, in term of the accurate detail finite volume model, the compact thermal model can be extracted.

Fig. 3 shows three different topologies of thermal resistance model. The simple one-thermal-resistance model consists of junction-to-bottom thermal resistance (Fig. 3(a)). It is assumed that all the heat generated by the active layer conducted to ambient via the bottom surface. The two-thermal-resistance model consists of junction-to-bottom and junction-to-top thermal resistance (Fig. 3(b)). It will conduct heat flow to the top and bottom surface. Six thermal resistances connecting the junction to the package surface compose the star-thermal-resistance model (Fig. 3(c)). To refine the compact thermal model, the bottom surface is divided into two areas. The bottom1 node is coincident with the inner of bottom surface, the bottom2 node is defined as the remaining portion of total bottom surface. The ratio of bottom1 to total bottom area is 0.03. The heat flow path from junction to bottom can be divided into two parallel heat flow paths. Table 1 shows the thermal resistances of three different topologies for LED package.

The junction temperature of three different topologies was calculated under 38 boundary conditions. Table 2 lists a complete set of 38 boundary conditions which are imposed on the detail finite element model and compact thermal model. Fig. 4 shows the difference of junction temperature between the detail and compact thermal model under 38 boundary conditions. The prediction of one and two-thermal resistance model is not accurate enough under different boundary conditions. The junction temperature prediction from one-thermal-resistance model is within 16% of the detail model. The star-thermal-resistance model gives the most consistent and accurate prediction for the junction temperature, within 5% for all boundary conditions. From Eq. (6), the optimized cost function for one-thermal-resistance model is 0.224. The star-thermal-resistance model produces the lowest cost function value (0.063) among all models. Fig. 4 shows the optimal values of thermal links with the cost function in the predicted junction temperatures on the three topologies of compact models for the LED package. It is to be noted that the cost function is further reduced with the star-thermal-resistance model. The inner-connections among the nodes of network usually can provide further accuracy for redistribution of heat flows. As expected, the more complex thermal resistance model provides better agreement with the detail model compared to the one-thermal-resistance model and two-thermal-resistance model.

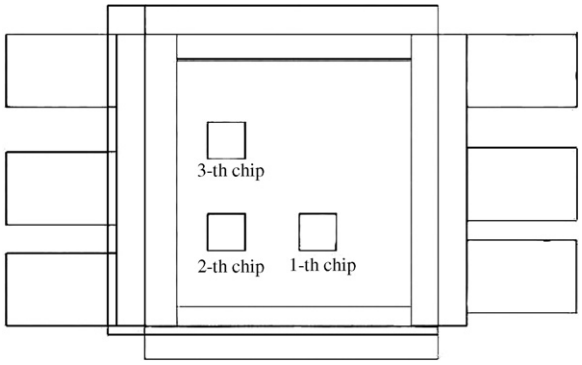


**Fig. 5.** Construction of multi-chip LED package.

According to the compact thermal model of single-chip LED package, it is now possible to establish the thermal resistance network of multi-chip LED package. Since the thermal coupling will influence each other chip, interacting thermal resistance must be considered for compact thermal model of multi-chip module. Fig. 5 demonstrates the construction of multi-chip LED package in FLOTHERM. Resistances $\theta_{JC}^{12}$, $\theta_{JC}^{13}$ and $\theta_{JC}^{23}$ describe the thermal coupling effect among the neighboring chips. The power is applied on the 1st, 2nd and 3rd chip sequentially. Then the junction temperatures are captured in each chip by both experiment and simulation. The junction temperature for a two-chip package or three-chip package is defined by the average junction temperature of all chips in the package. The interacting thermal resistance of neighboring chips is 26.8 K/W, 26.7 K/W and 28.0 K/W for $\theta_{JC}^{12}$, $\theta_{JC}^{23}$ and $Q_{JC}^{13}$, respectively. The interaction between the 1st chip and 2nd chip is quite same as the interaction between 2nd chip and 3rd chip. This can be explained by the same size and space between them. Since the space between 3rd chip and 1st chip is different from others, $\theta_{JC}^{13}$ is larger than $\theta_{JC}^{12}$ and $\theta_{JC}^{23}$. The compact thermal model of multi-chip LED package is based on validated detail model. The validity of Eq. (7) for establishing the compact thermal model is verified by the coincidence between the thermal measurement and simulation. Also, Kim and co-workers have analyzed the side effects in thermal characterization of multi-chip LED package by Eq. (7) [16]. The junction temperature rise of multi-chip LED package is shown in Fig. 6, from which one can see the steady state is roughly reached after 10 s. It is clear that the junction temperature rise of three-chip LED is

**Table 1**
Thermal resistances of three different topologies for LED package.

| One-thermal resistance model | | Two-thermal resistance model | | Star-thermal resistance model | |
|---|---|---|---|---|---|
| $R_{J-B}$ | 9.0 K/W | $R_{J-B}$ | 9.3 K/W | $R_{J-B1}$ | 7.4 K/W |
| – | – | $R_{J-T}$ | 257.1 K/W | $R_{J-T}$ | 819.4 K/W |
| – | – | – | – | $R_{J-S}$ | 769.6 K/W |
| – | – | – | – | $R_{J-L}$ | 3088.1 K/W |
| – | – | – | – | $R_{B1-B2}$ | 2.0 K/W |
| – | – | – | – | $R_{T-B2}$ | 16.2 K/W |

**Table 2**
Device may encounter in practical 38 boundary conditions.

| BC | $h_{TOP}$ (W/m$^2$ K) | $h_{BOTTOM}$ (W/m$^2$ K) | $h_{SIDE}$ (W/m$^2$ K) | $h_{LEAD}$ (W/m$^2$ K) |
|---|---|---|---|---|
| 1 | 10,000 | 10 | 10 | 100 |
| 2 | 10 | 10,000 | 10 | 100 |
| 3 | 10,000 | 10 | 10 | 1,000 |
| 4 | 10 | 10,000 | 10 | 1,000 |
| 5 | 1 | 10,000 | 1 | 10,000 |
| 6 | 10,000 | 1 | 1 | 10,000 |
| 7 | 500 | 10 | 10 | 1,000 |
| 8 | 1,000 | 10 | 10 | 1,000 |
| 9 | 10 | 500 | 10 | 1,000 |
| 10 | 10 | 1,000 | 10 | 1,000 |
| 11 | 500 | 10 | 10 | 100 |
| 12 | 1,000 | 10 | 10 | 100 |
| 13 | 10 | 500 | 10 | 100 |
| 14 | 10 | 1,000 | 10 | 100 |
| 15 | 200 | 200 | 200 | 1,000 |
| 16 | 50 | 50 | 50 | 1,000 |
| 17 | 200 | 200 | 200 | 10,000 |
| 18 | 100 | 100 | 100 | 10,000 |
| 19 | 50 | 50 | 50 | 10,000 |
| 20 | 10 | 10 | 10 | 10,000 |
| 21 | 1E+8 | 1E+8 | 1E+8 | 1E+8 |
| 22 | 30 | 30 | 30 | 30 |
| 23 | 50 | 50 | 50 | 50 |
| 24 | 100 | 100 | 100 | 100 |
| 25 | 100 | 100 | 100 | 500 |
| 26 | 100 | 1 | 100 | 1,000 |
| 27 | 1 | 100 | 100 | 1,000 |
| 28 | 100 | 100 | 100 | 1,000 |
| 29 | 1,000 | 1,000 | 1000 | 1,000 |
| 30 | 10 | 10 | 10 | 100 |
| 31 | 10 | 10 | 10 | 1,000 |
| 32 | 10 | 10 | 10 | 50,000 |
| 33 | 100 | 10 | 10 | 100 |
| 34 | 100 | 10 | 10 | 1,000 |
| 35 | 10 | 100 | 10 | 100 |
| 36 | 10 | 100 | 10 | 1,000 |
| 37 | 100 | 100 | 10 | 100 |
| 38 | 100 | 100 | 10 | 1,000 |

highest and the one-chip LED is lowest. Fig. 7 shows the cumulative structure function obtained by T3Ster measurement for one-chip, two-chip and three-chip packages. By comparing the cumulative structure function, a simplified RC model of multi-chip LED packaged can be obtained. The junction-to-ambient thermal resistance is 16.9 K/W for the one-chip package, and is reduced to 10.5 K/W and 8.6 K/W for the two-chip and three-chip packages, respectively. For the one-chip package, the junction-to-chip thermal resistance is 3.1 K/W, and chip-to-Cu slug 13.7 K/W. For the two-chip package, the junction-to-chip thermal resistance is 1.7 K/W, and chip-to-Cu slug 6.9 K/W. For the three-chip package, the junction-to-chip thermal resistance is 1.2 K/W, and chip-to-Cu slug 4.7 K/W. The increase in the number of chips results in the decrease of thermal resistance. The trend is influenced by electrical series resistance and the optical efficiency of multi-chip package with the power dissipation and the temperature. The experimental results are coincident with the theoretic analysis [17]. Table 3 exhibits good agreement among the detail model, compact thermal model and experimental measurement for junction temperature prediction for different number of chips. The measurement values of the junction temperature for one-chip package and two-chip package are lowest. The probable reason may be due to the underestimate of the radiative

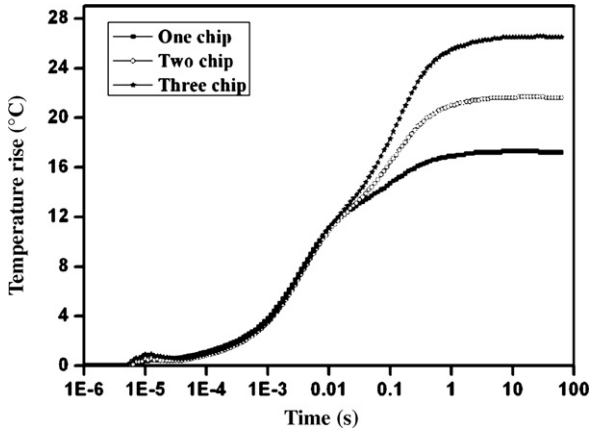


**Fig. 6.** Junction temperature rise of multi-chip LED package.

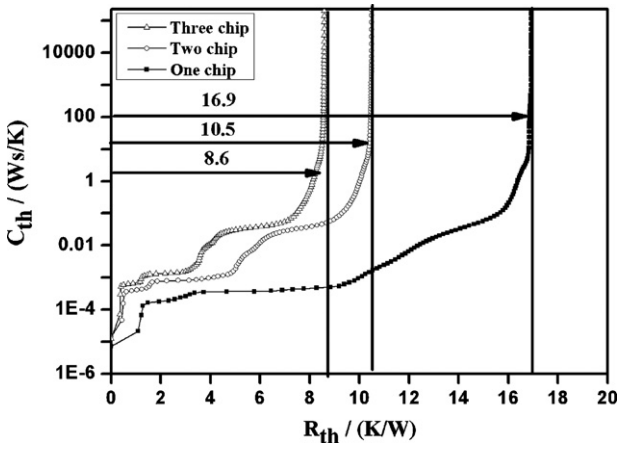


**Fig. 7.** Cumulative structure functions of one-chip, two-chip and three-chip package.

**Table 3**
Comparison of measured and simulated junction temperatures.

| | Power dissipation (W) | $T_J$ (°C) | $T_J^{CM}$ (°C) | $T_J^{FVM}$ (°C) |
|---|---|---|---|---|
| Three-chip | 3.169 | 51.5 | 47.8 | 49.7 |
| Two-chip | 2.123 | 46.6 | 48.5 | 46.8 |
| One-chip | 1.052 | 42.0 | 42.4 | 42.4 |

and convective heat transfer from the surface of compact modeling and finite volume modeling. However, three-chip package for the compact modeling yields lowest prediction of junction temperature. The probable reason is that the interacting thermal resistance between chips is underestimated because of the strong thermal coupling effects in three-chip package.

## 5. Conclusion

A method for creating compact thermal model of single-chip and multi-chip LED package is developed and evaluated. Three different compact thermal models derived from the detail finite volume model are experimentally validated. The one-thermal-resistance model and two-thermal-resistance model are unable to accurately capture the junction temperature. And the star-thermal-resistance model under 38 boundary conditions is proved to accurately predict the junction temperature. Based on the star-thermal-resistance model of single-chip LED package, the compact thermal model of multi-chip LED package with thermal coupling effect among chips taken into account is established. The simulation results show good agreement with experimental measurement.

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