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Fabrication, characterization and modeling of single-crystal thin film calorimeter sensors

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ABSTRACT

Thin film based nanocalorimetry is a powerful tool to investigate nanosystems from a thermal point of view. However, nanocalorimetry is usually limited to amorphous or polycrystalline samples. Here we present a device that allows carrying out experiments on monocrystalline silicon. The monocrystalline silicon layer consists of the device layer from a silicon-on-insulator wafer and lies on a low-stress free-standing silicon nitride membrane. We applied a number of characterization techniques to determine the purity and quality of the silicon layer. All these techniques showed that the silicon surface is as pure as a standard silicon wafer and that it is susceptible to standard surface cleaning procedures. Additionally, we present a numerical model of the nanocalorimeter, which highlights that the silicon layer acts as a thermal plate thereby significantly improving thermal uniformity. This nanocalorimeter constitutes a promising device for the study of single-crystal Si surface processes and opens up an exciting new field of research in surface science.

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1. Introduction

By measuring the heat involved in reactions and physical transformations, calorimetry provides unique information about these processes. Many problems in nanoscience and materials engineering involving surface or near-surface phenomena can significantly benefit from this information. For example, in microelectronics, nanosized transistors depend on the interaction between silicon and a thin metallic contact [1], or on how damage induced by ion implantation interacts with dopants [2]. In chemistry, catalysis reactions occurring at surfaces are of great interest in many industrial processes. In order to study these surface phenomena, a calorimetric sensor featuring an ordered surface and sufficient sensitivity to measure reactions involving small amounts of material would be of great benefit.

Nanocalorimetry has proven most valuable in research on a wide variety of nanoscale systems during the last decade. Phenomena such as melting point depressions [3], glass transitions in polymers [4] and glass forming liquids [5], melting of self-assembled organic monolayers [6], magnetic transition in thin layers of nickel [7], and annealing of ion-implantation-induced damage [8,9] were investigated using the technique. All these experiments were carried out using devices based on free-standing low-stress silicon nitride membranes (SiN_x). On top of the membrane, a metal strip is patterned to heat the sample and to measure its temperature [10,11]. The sample under investigation can be deposited on the metal strip if it does not affect the electrical properties of the strip, but usually, it is deposited on the other side of the membrane, in correspondence with the heating strip. The technique has been used *in situ* with a wide variety of deposition techniques such as evaporation, sputtering, as well as ion implantation [3–9], to avoid exposure to ambient pressure and to allow carrying out measurements at low temperature and a short time after or even during deposition [3].

However, one important limitation still arises: the sample is deposited on an amorphous or polycrystalline surface, which restricts the deposited layer itself to be amorphous or polycrystalline. The observed processes may thus be significantly influenced by the microstructure of the substrate. In this article, we present a nanocalorimeter (NC) device featuring a patterned thin layer of monocrystalline silicon (c-NC). This device will allow the investigation of numerous physical processes in which the monocrystalline

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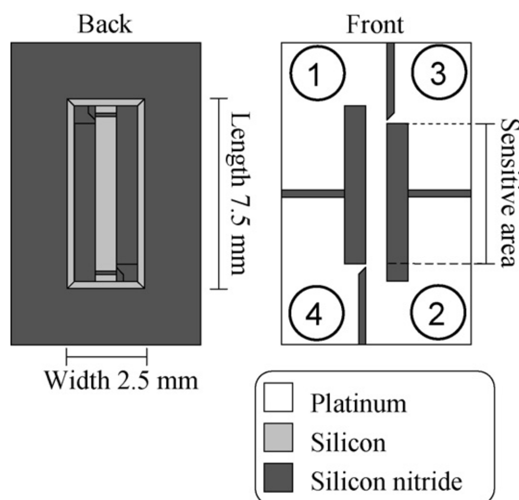

Fig. 1. Front and back views of the nanocalorimeter device. Current is supplied between contacts 1 and 2 while the voltage drop is measured between contacts 3 and 4.

Si surface plays a predominant role such as implantation damage annealing [8,9], 2D-to-3D strain driven transition in heteroepitaxial layers [12], agglomeration of ultra thin silicide films [13], and self-assembly of nanostructures on an ordered surface [14]. We present the c-NC fabrication technique and discuss its performances based on finite-element simulations and measurement examples. We will show that the c-Si, which offers an ordered monocrystalline and atomically flat surface, also acts as a thermal plate, therefore leading to a much more uniform temperature profile than in conventional NC devices.

2. Device operation

The c-NC device is compatible with conventional NC device operation explained in detail in Ref. [15]. Fig. 1 shows a schematic view of the front and back sides of the device. The sample is heated by supplying an electrical current through the platinum strip connected to pads 1 and 2. Simultaneously the voltage drop is measured by sensing point contacts that are connected to pads 3 and 4. The region of the metal strip that lies between these contacts is the part of the sensor that measures the heat capacity and will further be referred to as the *sensitive area*. The power dissipated in the sensitive area is calculated from the voltage and current measurements ($P = VI$).

The *average temperature* of the sensitive area is calculated from its resistance, $R = V/I$ which depends on temperature. The relationship between the resistance R and the temperature T is obtained by mounting a NC next to a thermocouple in a furnace for a calibration procedure. NC resistance and temperature are measured while the furnace temperature is changed at a rate slow enough to ensure thermal uniformity between the thermocouple and the NC. This procedure however cannot be used above $\sim$200 °C because the device supporting frame, made of c-Si, becomes conductive and alters the resistance measurement of the strip, a situation that does not happen during fast temperature scanning of the device [11]. In experiments carried out at higher temperatures, one therefore has to rely on data extrapolation for the temperature calibration. The accuracy of the calibration will be discussed in Section 5.

Prior to high temperature experiments and before temperature calibration the NCs are annealed to temperatures above the maximum experimental temperature because high temperature scans can alter the electrical properties of the heater strip. These changes influence the temperature calibration and temperature accuracy and might eventually cause device failure. One minute rapid thermal annealing of the device in inert atmosphere (N_2 or Ar) clearly improves device stability of the device and limits the effects mentioned above. Further stabilization can be achieved by performing a large number (500–3000) of heating cycles in high vacuum (<10^{-6} Torr) prior to the experiments. A similar annealing procedure is presented in Ref. [11].

3. Device fabrication

Sarro et al. created a micro-device featuring a silicon island on a SiN_x membrane as well [16]. Their fabrication process however requires that the silicon island is heavily n-doped and might not be suitable for silicon layer thinner than 100 nm because of etch rate uniformity. Our process yields a silicon island as pure, as smooth and as thin as the SOI device layer. The operation principle is also quite different, our design aiming at fast scanning nanocalorimetry.

A detailed description of conventional NC fabrication as well as of the calculations necessary to extract the evolution of the heat capacity of the specimen during a temperature scan can be found in Refs. [10,15]. Here, we detail the additional processing steps required for fabricating a c-NC. All steps are schematically represented in Fig. 2. The process starts with a double-side-polished silicon-on-insulator (SOI) wafer with a (1 0 0) orientation. The device layer can actually consist of any material (e.g. Si_xGe_{1-x}, $0 \le x \le 1$) that is compatible with the SiN_x deposition process. For the devices characterized below, the handle, buried oxide, and device layers are, respectively, 300 μm, 1 μm, and 330 nm thick. A 250 nm thick layer of low-stress, high density SiN_x (200 MPa tensile stress) is deposited on both sides of the SOI wafer by low-pressure chemical vapor deposition (Fig. 2a). The layer is deposited at 850 °C and 170 mTorr at a rate of 3 nm/min using $SiCl_2H_2$ and NH_3 gases at a flow of 57 and 13 sccm, respectively.

The subsequent steps consist in depositing and patterning the metal strip (here made of Pt). These steps are similar to those described by Karmouch et al. [10], except that the Ti adhesion layer is replaced by Cr because of its resistance against subsequent hydrofluoric acid (HF) etching steps (Fig. 2b).

A cavity is then etched from the backside of the NC (Fig. 2c). A photoresist mask is patterned, aligned with the metal pattern on the front side. The SiN_x layer is removed by reactive ion etching (RIE) using SF_6 and He flowing at 26 and 14 sccm, respectively, and setting the power of the plasma to 250 W. The oxide is removed in HF and a cavity in the Si handle is anisotropically wet etched using a tetramethylammonium hydroxide (TMAH) solution. This etch will stop on the buried oxide. The exposed oxide layer is subsequently removed using HF etching (Fig. 2d).

The last step in the fabrication process consists in patterning the silicon strip. Photoresist (Shipley S1813) is carefully deposited at the bottom of the cavity, spin-coated at 3000 rpm for 30 s and soft-baked at 115 °C for 90 s. Exposure to UV light is carried out using a shadow mask. While exposure might be blurred due to the distance between the shadow mask and the bottom of the cavity, the photoresist offers sufficient contrast to result in a well-defined pattern. The photoresist is developed in a liquid solution (Shipley MF-319) for 90 s (Fig. 2e). Silicon is then etched by RIE using SF_6 flowing at 26 sccm at a power of 100 W for 14 min. In these conditions, silicon is etched at a rate at least five times higher than SiN_x thus providing sufficient selectivity to etch entirely the silicon layer without damaging the membrane. The remaining photoresist is first dissolved in acetone, then in N-methyl pyrolidinone for 5 min and is finally completely removed in an O_2 plasma at 300 W for 20 min (Fig. 2f). Extra HF etching can be carried out just before

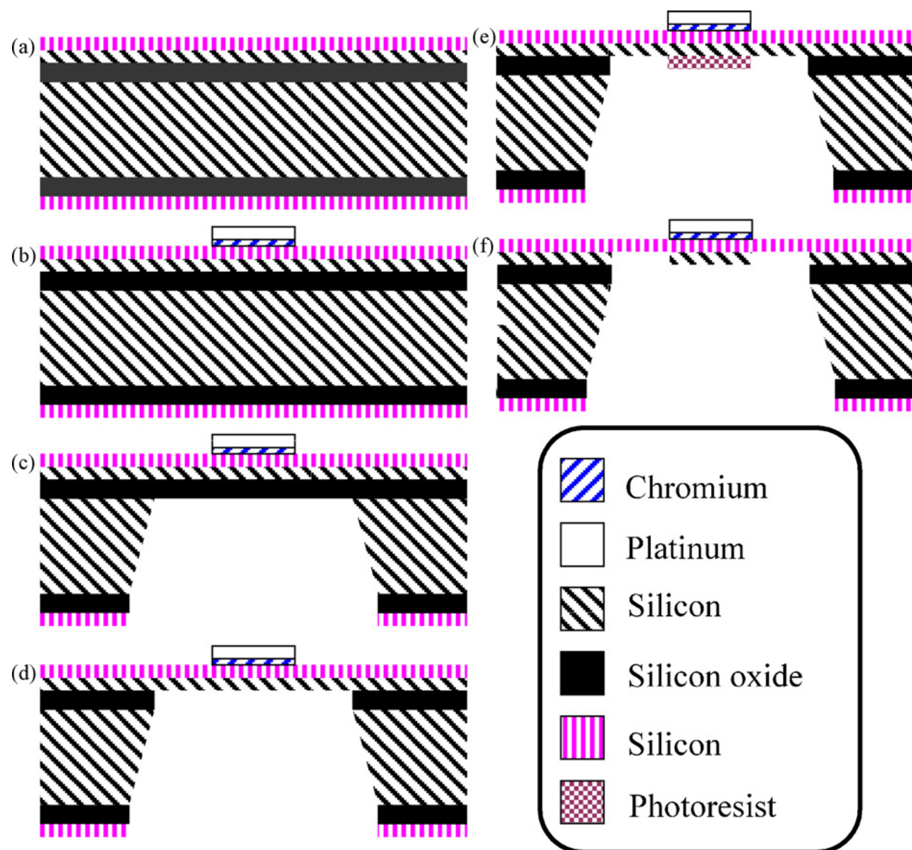

Fig. 2. Cross-sectional view of the c-NC at different steps in the fabrication procedure.

in vacuo experiments to remove the oxide produced by the O_2 plasma.

4. Experimental procedures

Rutherford backscattering spectrometry (RBS) measurements were performed with a 2 MeV He^+ beam directed perpendicularly onto the c-Si sample through a 300 μm slit placed in front of the specimen. Backscattered ions were collected on a detector that was placed at a backscattering angle of 170°.

Scanning electron microscopy (SEM), Auger electron spectroscopy (AES), and electron backscattering diffraction (EBSD) measurements were performed in an Omicron NanoTechnology Nanoprobe system. For all the experiments we used an electron beam generated by the ZEISS UHV Gemini column operated at 15 kV, using a 90 μm aperture yielding a sample current of approximately 3nA. SEM images were recorded using the in-lens secondary electron detector (SED) of the Gemini column. The Auger electrons emitted by the specimen were analyzed using a hemispherical electron analyzer that was operated in constant retard ratio (CRR) mode. For the EBSD measurements the sample was tilted over 70° with respect to the incident electron beam, the Kikuchi patterns were recorded with an Oxford instruments Nordlys detector and indexed using the HKL CHANNEL 5 software. *In situ* sputter cleaning of the c-NC was performed using a FIG-5CE focused ion gun from Physical Electronics mounted on the NanoSAM system. Ar^+ ions were incident on the specimen at an angle of approximately 32° with respect to the surface and at a typical current density of 0.55 $\mu A/cm^2$.

Atomic force microscopy (AFM) images were acquired in tapping mode under ambient conditions using an extended Dimension 3100 scanning probe microscope and Nanoscope IIIa controller (Digital Instruments/Veeco, Santa Barbara, CA) using a NanoWorld Arrow cantilever.

Infrared (IR) photography was carried out with an Infratec VarioCAM infrared camera. The camera is equipped with a microbolometer focal plane array detector of 384 × 288 pixels that has a spectral range off 7.5 μm to 14 μm. Using an optomechanic interpolating function the resolution was increased to 768 × 576 pixels which yields an effective resolution of 300 μm. To prevent air from flattening the temperature profile and to prevent NC oxidation, measurements were carried out in high vacuum (better than 10^{-6} Torr). All photographs were taken through a ZnSe window that is transparent to IR radiation. For these specific measurements, we were interested in the temperature profile rather than in absolute temperatures. Therefore, the software settings of the camera (emissivity and transmissivity) were adjusted so the average temperature indicated by the camera corresponds, within 10 °C, to the temperature calculated from the Pt strip resistance (Section 6). Experiments regarding the precision of the temperature measurement are described in the next section.

5. Characterization

In this section we show that the c-NC has a well-defined and well aligned silicon strip of quality comparable to that of a standard silicon wafer and that the device is susceptible to standard surface treatments. We will further demonstrate the excellent temperature uniformity and accuracy of the device at high temperature.

5.1. Structural and compositional characterization

Fig. 3 presents a polarized-light micrograph of the patterned Si strip located on the backside of the NC and, through the SiN_x, the

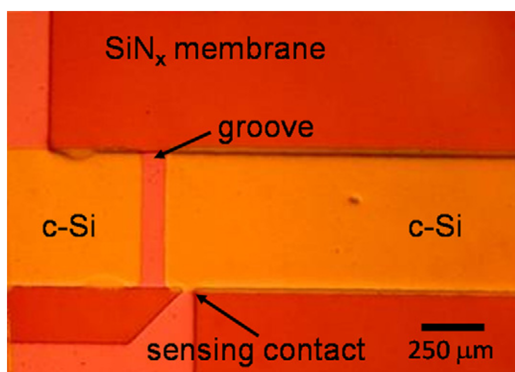

Fig. 3. Optical micrograph of a c-NC near one end of the Pt strip with a voltage sensing contact point (pale orange) and the 330 nm c-Si layer (yellow) featuring a groove (see text for details). Pt and c-Si are on opposite sides of the SiN_x transparent membrane (dark orange). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

metallic pattern that features a triangular contact point for voltage measurement. The Si strip comprises grooves near each end also represented schematically in Fig. 1. The purpose and design of these grooves will be discussed in Section 6.

RBS measurements (not shown) with a collimated beam were carried out on regions corresponding to the c-Si/SiN_x/metal stack and off this region, confirming the complete Si removal away from the metallic strip region while the expected layer thicknesses are obtained along the strip.

The c-Si surface after NC fabrication and upon chemical cleaning as well as sputter cleaning has been characterized using SEM, AES, EBSD and AFM. Fig. 4 shows AES spectra of the c-Si strip after NC fabrication, after a 40 s dip in buffered oxide etch (BOE) HF (1%) and after 30 min of Ar^+ sputter cleaning. As confirmed by SEM measurements (not shown), the NC is stable against the HF-dip as well as the Ar^+ sputter process. We performed AES measurements on different spots on the c-Si strip. The spectra shown in Fig. 4 are representative for the entire strip. The spectrum from the as-fabricated NC shows the predominant presence of oxygen related to the native oxide found on Si substrates, which is also evidenced

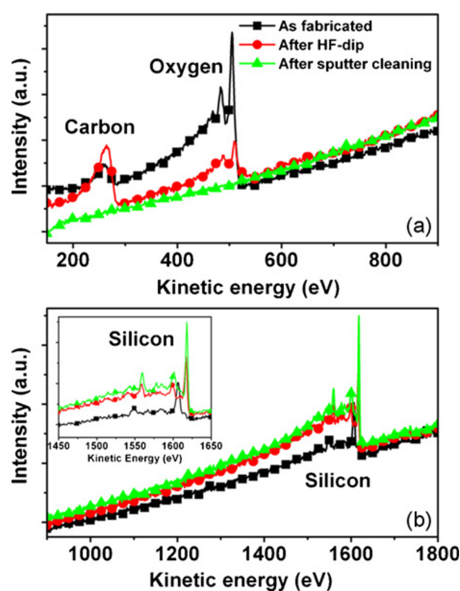

Fig. 4. AES spectra from the Si strip after fabrication of the calorimeter (■), after the HF-dip (HF–BOE 7:1, 40 s) (●) and after Ar^+ sputter cleaning (▲), showing the carbon and oxygen signals (a) and the silicon KLL signal (b). The inset of (b) is a zoom on the Si signal.

by the Si KLL peak at 1606 eV [17]. No other impurities other than carbon and oxygen could be detected after fabrication. Moreover, the oxygen and carbon signals are comparable to those that one would find on a standard Si wafer before surface treatment. After the HF-dip, the carbon signal increases. This is the result of a relative increase of the atomic concentration of carbon on the surface as most of the oxide is removed by the chemical treatment. A small oxygen peak remains visible in the spectrum because of the limited etching time in the diluted HF solution. The most intense Si KLL line can now be found at 1617 eV, which corresponds to Auger electron emission from pure silicon [17]. The oxide related Si KLL line has dropped below the detection limit. Upon *in situ* sputter cleaning, both carbon and oxygen are completely removed and one is left with an atomically clean silicon surface over the entire c-Si strip.

To assess the crystalline quality of the silicon in the strip, we applied EBSD. Fig. 5 shows a Kikuchi pattern that is representative for the complete c-Si strip. The obtained Kikuchi patterns could all be positively indexed as Si with a (1 0 0) orientation, as shown in Fig. 5b. The EBSD pattern in Fig. 5 was acquired after NC fabrication. Although its quality might slightly increase after the HF-dip and after sputter cleaning because of the removal of the oxide and carbon layer, the quality of the Kikuchi pattern in Fig. 5 is already extremely good and corresponds well to what can be expected from a standard monocrystalline Si wafer.

The c-Si surface was further characterized using AFM (Fig. 6). To perform these measurements the SiN_x membrane was removed from the silicon frame using adhesive tape. This manipulation induces millimeter scale ripples due to the membrane removal method or resulting from the actual stress in the multilayer. These ripples however, occur on a scale much larger than the micrograph scale and therefore do not influence the result of the measurement. After fabrication, the RMS surface roughness measured by AFM (5 μm × 5 μm) is 0.1 nm. A 1 min dip in a diluted HF solution (1%) results in an enhanced surface roughness (0.3 nm RMS), similar to what is observed for standard Si(1 0 0) wafers [18].

The AFM, EBSD, AES and SEM characterization of the c-NCs after fabrication, upon HF treatment and after Ar^+ sputter cleaning demonstrate that the c-Si strip is atomically flat, is of good crystalline quality, shows no other impurities than those that can be found on off-the-shelf silicon wafers and is susceptible to standard surface treatments used in Si processing and research. Hence, the fabricated c-NCs form a promising device for the investigation of process on single-crystal Si surfaces. Moreover, the fabrication process can easily be adapted to the fabrication of NCs with different surfaces, with the advent of opening up an exciting new field of research in surface science.

5.2. Temperature uniformity and device accuracy

An important characteristic of a NC is its temperature uniformity across the sensitive area, as this will affect the temperature resolution achievable during measurement. Here, we estimate this uniformity from experimental considerations while we present finite-element simulations in the subsequent section. Upper and lower limits are obtained from experimental measurements of the recrystallization peak of amorphous silicon and from the width of an Al melting peak. The Al melting peak further allows determining the accuracy of the temperature and heat capacity scales.

5.2.1. Recrystallization of a-Si

The heat release during recrystallization of c-Si after ion implantation was measured. A layer of the c-Si strip was amorphized by ion implantation: 5 Si/nm^2 were implanted at 80 keV in 42 min in vacuum (<10^{-6} Torr) while holding the sample holder at room temperature (RT). The NC temperature was monitored during

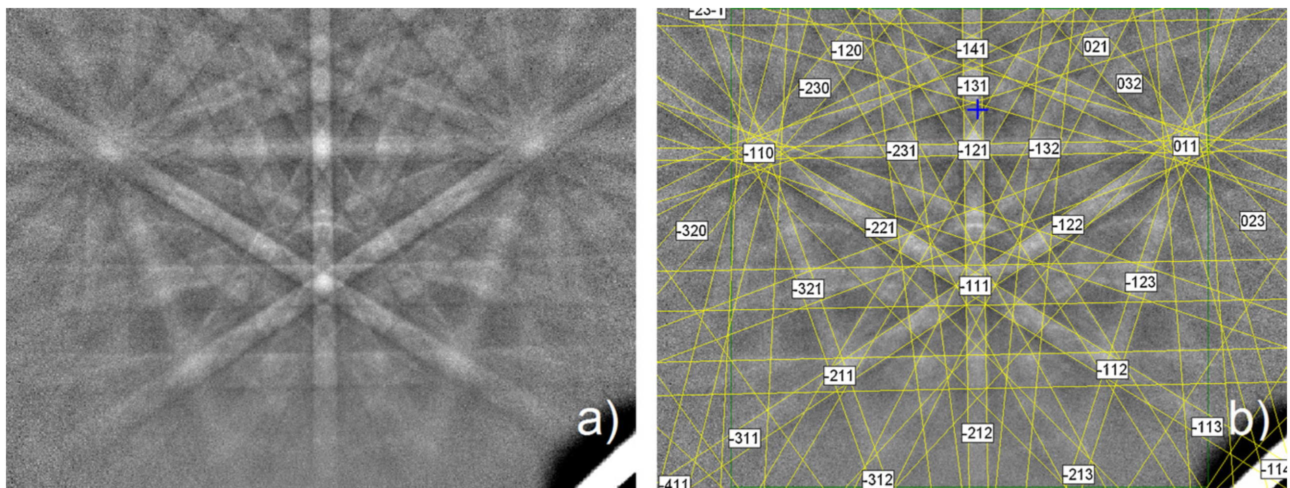

Fig. 5. (a) EBSD image taken on the c-Si strip. The Kikuchi patterns could be positively indexed as Si with a (1 0 0) orientation, as shown in panel (b), all over the strip.

implantation using the Pt strip resistance, confirming only a small temperature increase (<5 °C) due to ion beam energy deposition. An implantation mask was used to implant a band of 200 μm in width along the middle of the c-Si strip. The implanted area was thus 1.1 mm^2. According to SRIM 2008 simulations [19] less than 1% of the implanted ions reached the SiN_x membrane since the typical implantation depth at 80 keV is 113 nm and less than 2% of the implanted ions penetrate further than 200 nm while the nominal thickness of the Si layer is 330 nm. This ensures that the signal comes from the silicon sample and not from the SiN_x membrane.

Temperature scans were performed *in situ* from RT to 920 °C in 7 ms, at heating rates decreasing during the scan from 2×10^5 to 0.8×10^5 °C/s. Fig. 7 shows the heat release difference between the implanted and non-implanted NC ΔH per unit temperature as a function of temperature, resulting from the implantation damage annealing during the first scan. Heat release was extracted using the method described in Ref. [15]. Note that the signal is positive for the exothermic reaction process studied. All heat was released during the first scan after implantation: no measurable amount of heat being released during subsequent scans. Fig. 7 shows a uniform heat release from 200 to 600 °C that is attributed to the structural relaxation of the amorphous layer [9,20]. Following that stage, a peak extending from 600 to 900 °C arises due to the solid-phase epitaxial recrystallization of the amorphous layer. The increase in recrystallization temperature compared to standard differential scanning calorimetry scans (DSC) [20] is due to the higher scanning rates used in nanocalorimetry.

The high temperature edge of the recrystallization peak can be used to estimate the thermal uniformity at high temperature. Since the recrystallization process is thermally activated, the heat release rate rises exponentially with temperature and drops to zero when the entire amorphous layer has recrystallized. If the temperature was completely uniform, the peak would drop abruptly to zero once the complete layer has recrystallized. The derivative of the heat capacity would in that case yield a negative delta function. For a non-uniform temperature profile, the derivative shows a (negative) peak of which the width gives an estimate for the temperature uniformity. For the data in Fig. 7 the full width at half maximum of this peak is 37 °C. Assuming a Gaussian temperature distribution, this yields a temperature uniformity with a standard deviation better than 16 °C at around 900 °C. This value represents an upper limit for the temperature uniformity. Firstly, such an exothermic reaction might amplify temperature differences because the regions at higher temperature will release heat at higher rates, further increasing the temperature difference with regions at lower temperature. Usually, a faster scanning rate should translate into a more uniform temperature resulting from lower conductive losses, but in this case, we are considering local heating that is accelerated by further local heat release. Secondly, the experimental data are smoothed in order to remove the high frequencies noise [15] which can cause additional peak broadening.

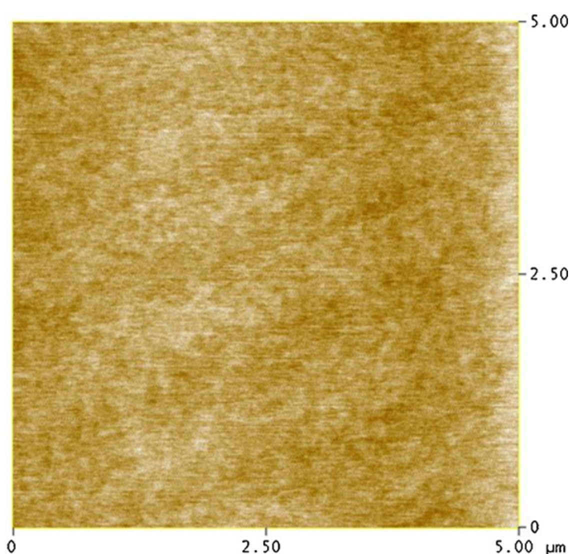

Fig. 6. AFM plot of the c-Si strip surface. Black-to-white scale is 5 nm.

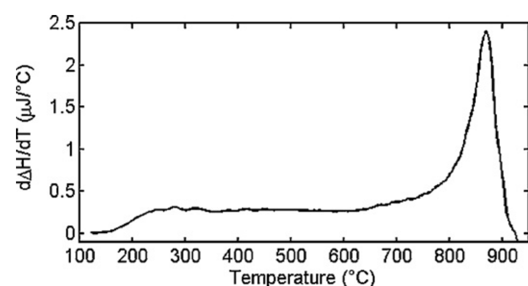

Fig. 7. Heat release per unit temperature after amorphization of the top part of the c-Si strip by implanting 5 Si/nm^2 at 80 keV.

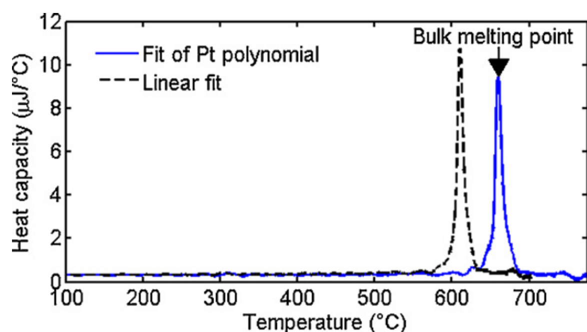

Fig. 8. Heat capacity and melting peak from a 60 nm Al layer deposited on SiO_2 on a c-NC. The black dashed curve is obtained by considering a relationship $R(T)$ extrapolated linearly above 200 °C while the blue solid curve considers an extrapolation based on the temperature dependence of bulk Pt resistivity. The arrow indicates the melting point of bulk Al which is 660.32 °C. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

5.2.2. Melting point of Al

Another primary concern is the accuracy of the temperature calibration $R(T)$ at high temperature. In the Section 2 we explained that calibration can only be performed for temperatures lower than ~200 °C. We therefore rely on an extrapolation for the temperature calibration at higher temperatures. Here we explore two extrapolation methods. The first one consists in extrapolating the calibration data linearly and will further be referred to as *linear fit*. The second consists in finding the best fit of the calibration data with the following equation:

$$R(T) = a\rho_{Pt}(T) + b \quad (1)$$

where a and b are free parameters and $\rho_{Pt}(T)$ is the tabulated polynomial (4th order) for the temperature dependence of the resistivity of bulk platinum. This method will further be referred to as *polynomial fit* although only two free parameters are fitted.

In order to prevent the Al layer from reacting with the Si strip, we first deposit 60 nm of silicon oxide on the whole membrane by sputtering a Si target in an oxygen-rich atmosphere. Al was then deposited *ex situ* by e-beam evaporation at a rate of 0.3 nm/s at a base pressure of 2×10^{-7} Torr using a shadow mask. The deposited layer has an area of $2.12 \pm 0.04\ mm^2$. RBS measurements performed on a sample situated next to the NC during the deposition indicate a thickness of 58 ± 3 nm, assuming an Al bulk density of $2.70\ g/cm^3$.

The c-NC was transferred in air to a vacuum chamber with a base pressure better than 10^{-6} Torr for the temperature scans. The Al layer is thick enough as to minimize size effect such as melting point depression that is usually observed for layers thinner than 40 nm [21] or surface effects like oxidation which does not extend above 3.5 nm in Al films [22]. Scans were performed at an average heating rate of 1.3×10^5 °C/s. To reduce the noise 20 scans were averaged. The resulting heat capacity curves, considering the linear and polynomial $R(T)$ calibration extrapolation described above, are reported in Fig. 8 which reveals a uniform heat capacity on which the melting peak is superimposed. When using the polynomial fit the Al melting peak is found at 659 ± 1 °C, in excellent agreement with the tabulated value of 660.32 °C [23]. The extrapolation based on the linear fit yields a temperature which is 50–60 °C lower than the tabulated value. Similar experiments carried out on standard NC (also with a SiO_2 protective layer) show that the Pt polynomial fit extrapolation method offers a precision usually better than 20 °C with rare cases leading to an error to up to 40 °C. For nanocalorimeters that are fabricated in the same batch the Al melting points always seem to come out within 5 °C from one another. The variation in temperature precision between batches is larger and depends on the quality of the Pt heating strip. Slightly different properties of the Pt metallization will result in a different heater resistance *versus* temperature relations–that might also deviate slightly from the tabulated relation for bulk Pt. The few experiments carried out on c-NC indicate that these differences between NCs are smaller when a c-Si strip is present and that absolute temperature accuracy is better. Long term use will have to reveal if this better precision for c-NC is related to the more homogeneous temperature profile (see further) and therefore better annealing conditions for the Pt heater during pre-experimental stabilization, or rather to the fact that the average temperature corresponds better to the actual temperature when dealing with a more homogeneous temperature profile. Before additional verification of the temperature precision on c-NCs it is safer to assume an uncertainty of 20 °C on the temperature scale at high temperature.

Rather than relying on extrapolations of $R(T)$, this Al deposition procedure can be carried out after an experiment in order to reduce the uncertainty on temperature by adding the Al melting point to the calibration data acquired at lower temperatures. Moreover, since devices fabricated in the same batch usually have very similar characteristics, the same Al melting point data can be used to calibrate c-NCs.

From the heat capacity obtained during the experiment, the Al thickness can be calculated using two independent approaches. The first one consists in evaluating the average heat capacity value from 100 to 200 °C and dividing this by the specific heat and deposited area. The second consists in integrating the melting peak from 630 to 690 °C in order to get the heat of fusion and dividing by the specific heat of fusion and deposited area. The nanocalorimetry measurement returns a thickness of 63 ± 5 nm according to heat capacity while the heat of fusion yields a thickness of 60 ± 2 nm, in excellent agreement with RBS data confirming that the accuracy of the heat capacity scale is better than 10%.

The measurement shown in Fig. 8 further allows estimating the temperature uniformity over the c-Si strip. The full width at half maximum of the Al melting peak is 13 °C (σ = 5.5 °C assuming a Gaussian temperature distribution). While this number gives a direct indication of the temperature uniformity, it can be affected by a number of effects, one of them being that an endothermic process such as melting tends to slow the heating rate of hot regions first, and thus decreases the width of the temperature distribution during melting. Here, the heating rate is decreased by a factor of two during melting and it can therefore reduce the apparent temperature uniformity by a factor two as well. Another factor that could improve the apparent temperature uniformity of the device is the actual presence of Al which acts like an additional thermal plate that represent 30% of the contribution to thermal conductivity of the Si strip. The estimated standard deviation for the temperature uniformity of 5.5 °C should therefore be regarded as a lower limit that can be off by a factor two.

It should be pointed out that melting peak measurements on c-NC devices produce a more symmetric melting peak compared to standard NC which always exhibit a high temperature tail that is attributed to material melting on each side of the strip [24]. As discussed in the next section, the c-Si layer acts as a thermal plate, making the temperature laterally more uniform which significantly decreases the effects causing this tail.

6. Finite-element simulations

In order to study the temperature profile, namely outside the sensitive area, and to develop a better understanding of the operation of our device, we carried out finite-element 2D simulations. In the first subsection, we describe the model used and compare the simulations with IR measurements of the temperature profile. In the second subsection, the model is applied to investigate the tem-

Table 1
Thermal conductivities and heat capacity at room temperature and their temperature dependence coefficient of the materials forming part of the c-NC.

	C_p (J g^{-1} K^{-1})	1st C_p coef. (J g^{-1} K^{-2})	2nd C_p coef. (J g^{-1} K^{-3})	k (W m^{-1} K^{-1})	λ (W m^{-1} K^{-2})	μ (W m^{-1} K^{-3})
Pt	0.132 [28]	–	–	44.89 [24][b]	–	–
SiN_x	0.80 ± 0.01[a]	7.88×10^{-4}[c]	-3.46×10^{-7}[c]	2.7 ± 0.1[a]	$1.0 \pm 0.1 \times 10^{-2}$[a]	–
Si	0.7 [27]	7.88×10^{-4} [27]	-3.46×10^{-7} [27]	149 [31]	-4.57×10^{-1} [30]	2.61×10^{-4} [30]

[a] This work.
[b] Scaled according to Franz–Wiedemann law.
[c] Assumed to be equal to Si.

perature uniformity for different device designs and for different types of measurements.

6.1. Model description

Our model realistically represents the different components of the actual experimental setup. We modeled a constant current source that supplies power to the heater/sensor. The current flowing through the metallic strip heater is distributed according to the resistivity of each element, which depends on its temperature. The relation between the temperature and resistivity for a single element is obtained by scaling calibration data while assuming that the Pt heater properties are uniform throughout the film. The geometry of the system was represented by a rectangular mesh of 20 μm × 10 μm as shown in Fig. 9 or 20 μm × 1 μm depending on the smallest details to render. To avoid the simulation from running out of bounds, the largest time step used was 0.2 μs. For every simulation the mesh size and time step were changed by an order of magnitude to ensure that our solution is not mesh dependent. In order to speed up the simulation, only the membrane and the sides of the cavity are considered. Simulated area boundaries are forced to stay at RT to represent the effect of the silicon frame surrounding the cavity whose heat capacity is more than 1000 times larger than that of the membrane. Because the thicknesses of the membrane and of the layered structure of the device are small (less than 0.63 μm) compared to the smallest thermal diffusion length of the system (1 μm in 10 μs for SiN_x) temperature deviations between the top and bottom of the sensitive area are expected to be negligible in the considered time interval (several milliseconds per scan). 2D simulations are therefore sufficient to grasp all important effects of thermal conductivity on device performance.

The quantity of each material constituting the simulated NC was obtained from RBS measurements. These measurements yield the number of atoms per cm^2. To extract thickness values, the bulk density of each material is assumed except in the case of SiN_x since its density varies depending on the deposition method. For SiN_x

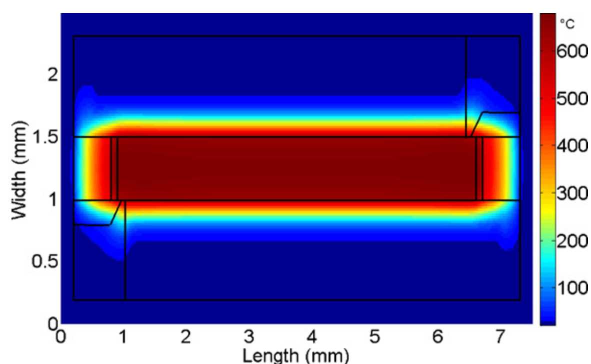

Fig. 9. Typical temperature profile from a c-NC reaching an average temperature of 660 °C in the sensitive area, as determined from a 2D finite-element solution of the heat equation considering a mesh consisting of 93 750 nodes. (Length and width axes not to scale for clarity.) Superimposed black lines represent the device geometry as shown in Fig. 1.

we assumed that the nominal deposited thickness is correct. The density deduced from this assumption and RBS measurement was calculated to be 2.8 g/cm^3.

All thermal parameters used in the simulation are shown in Table 1. The model has four adjustable parameters: the RT thermal conductivity k_{SiN_x}, the slope of the relation between thermal conductivity and temperature that is assumed to be linear λ_{SiN_x}, the specific heat C_{p,SiN_x} of the SiN_x membrane, and the emissivity ε which we consider constant for the whole surface. These parameters were adjusted to account for the fact that the properties of the SiN_x film can slightly vary depending on the deposition technique. Heat losses generated by ambient gas were neglected since we always carry out measurements at vacuum better than 10^{-6} Torr. It has a significant influence at ambient pressure. k_{SiN_x}, λ_{SiN_x} and ε are related to the rate at which heat is lost to the environment and can be adjusted independently from C_{p,SiN_x}. This was carried out by heating the c-NC until it reaches steady-state temperature and by comparing the steady-state temperature achieved in the simulation. The parameters were adjusted accordingly. This procedure has been repeated for several temperatures. The temperature reached by the device in steady-state only depends on the rate at which heat is lost to the environment and not on the heat capacity, leaving the three mentioned parameters to adjust. The low temperature steady-state temperature profile gives us k_{SiN_x} near RT, medium range temperature yields λ_{SiN_x}, and high temperature profiles allow us to estimate ε. The RT value of k_{SiN_x} was estimated to be 2.7 ± 0.1 W m^{-1} K^{-1}, in fairly good agreement with reported values of 2.41 W m^{-1} K^{-1} [25]. λ_{SiN_x} was estimated to $1.0 \pm 0.1 \times 10^{-2}$ W m^{-1} K^{-2}, about 40% higher than the value reported in Ref. [26] which was obtained at significantly lower temperatures (between 50 K and RT). The emissivity was also adjusted to 0.125 ± 0.001 to fit the data.

The resistance of the Pt heater depends on the deposition technique and is also influenced by the presence of chromium adhesion layer. Knowing the electrical conductivity of the Pt strip, k_{Pt} is calculated from the Wiedemann–Franz law and was found to be 44.89 W m^{-1} K^{-1}. To avoid introducing extra parameters, k_{Pt} was assumed to be independent of temperature since it varies by only 10% from 300 to 1000 K for bulk [27]. In addition, k_{Pt} for our thin layer is expected to be even more stable (less than 5% variation) because the temperature dependence of the electrical conductivity is less than half the tabulated value. Simulation using a 10% higher conductivity did not show significant differences.

In order to test our model, the simulated steady-state thermal profile along the metallic strip was compared to the temperature profile as obtained by IR measurements. Three different currents (12, 16 and 19 mA) were supplied to the c-NC heating the sensitive area to 245, 400 and 515 °C, respectively. The simulations, shown as a solid line in Fig. 10, predict the longitudinal temperature profile obtained by IR measurements (dotted lines) with an accuracy better than 30 °C within the sensitive area, and within 70 °C near the simulation boundary. The discrepancy near the end of the sensitive area is due to the limited resolution in IR imaging. Convoluting our simulation results with a Gaussian smooth of 300 μm yields a match better than 5 °C within the sensitive

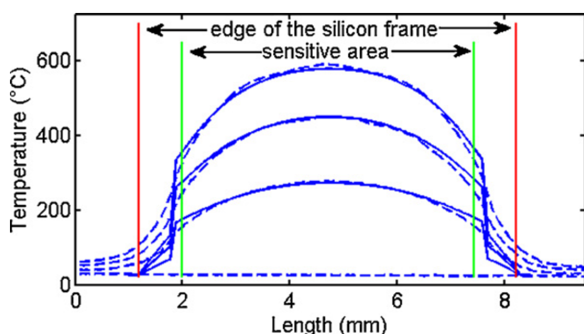

Fig. 10. Steady-state temperature profile measured by IR imaging (dashed line, steady-state) and calculated by finite-element method (solid line, after 1.5 s) along the middle of the heating strip. The average temperatures are 245, 400 and 515 °C for currents of 12, 16 and 19 mA, respectively.

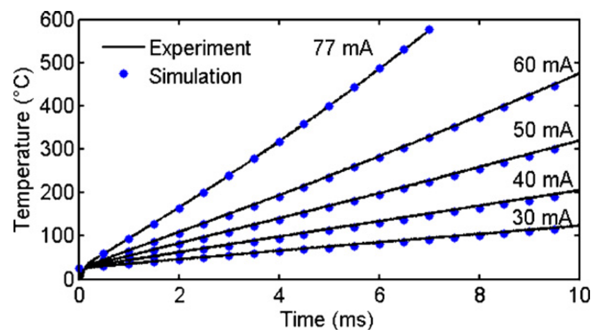

Fig. 11. Measured (solid line) and simulated (dots) average temperature in the sensitive area as a function of time and current.

area (not shown for clarity). Moreover, the remaining mismatch near the end of the strip is excepted since the measurements were done in steady-state. In this regime, it is not correct to assume that the surface of the silicon frame stays at a room temperature. During rapid temperature scans, however, this approximation is very good.

The results shown above only allow testing the model in a steady-state regime that is independent from specific heat parameters. On the contrary, in the adiabatic regime, results are mainly sensitive to the specific heat parameters allowing us to adjust them keeping the previously adjusted parameters unchanged. Assuming that the heat capacity of the SiN_x membrane is the same as that of Si [28], the specific heat of SiN_x at RT was estimated to be $0.80 \pm 0.05\,J\,g^{-1}\,K^{-1}$ which is, as expected, close to that of silicon ($0.7\,J\,g^{-1}\,K^{-1}$). Pt specific heat was assumed to behave like bulk Pt for which a value can be found in Ref [29] without temperature dependence as predicted by the Dulong and Petit's law. Fig. 11, which compares the temperature measured using the Pt strip resistance as a function of time for different currents supplied to the simulations, shows that the simulated temperature behavior (dots) matches the experiment (solid lines) within 8 °C for temperatures varying from RT to 600 °C. The agreement is more than satisfactory given the small number of adjustable parameters and the calibration uncertainties. We therefore conclude that the model gives a realistic picture of the device.

We further compared the simulation results to the lower limit of the standard deviation of the temperature distribution ($\sigma = 5.5\,°C$) estimated from the melting peak of Al in Section 5. Simulation for the same type of c-NC predicts $\sigma = 13.5\,°C$ (Fig. 13) which is in fairly good agreement taking into account that the estimated value from the melting experiment yields a lower limit value for the temperature uniformity as discussed in Section 5.

6.2. Design optimization

The design of a calorimeter can have a large influence on its accuracy and thermal uniformity. Various design optimization considerations for standard nanocalorimeters presented in Ref. [11] can be transferred to the c-NC device. Here we will first demonstrate that c-NCs show a better thermal uniformity than standard devices and further apply our numerical model to compare different c-NCs designs in terms of temperature uniformity. A similar strategy was adopted by Quiram et al. to improve thermal uniformity of a different type of membrane based microreactor [30].

6.2.1. Scanning mode

In order to highlight the role of silicon as a thermal plate, we compare the simulated thermal profile of two types of c-NCs. The first one features a c-Si strip spanning along the complete Pt strip and will further be referred to as *full strip c-NC*. The second one only differs from the first one by setting k_{Si} to zero. The later type of NC will further be referred to as *loaded conventional NC* since the heat capacity of the silicon strip is preserved. This would represent the case where a layer is deposited on the membrane with a heat capacity similar to that of the c-Si strip but with a much lower thermal conductivity, e.g. a 330 nm thick SiO_2 layer. The purpose of considering such case is that similar heating rates (within 10% in the worst case) are achieved when the same electrical current is supplied. This allows easier comparison since temperature uniformity depends on the heating rate.

In a first computer experiment we compare both calorimeters by heating them to 660 °C in 7.9 ± 0.1 ms using a current of 77 mA. Fig. 12 shows the temperature profiles after this current pulse. Fig. 12a indicates that the temperature profile along an axis perpendicular to the strip is significantly more uniform for the full strip c-NC as compared to the loaded conventional NC, as a result of the high thermal conductivity of c-Si. Conversely, Fig. 12b shows

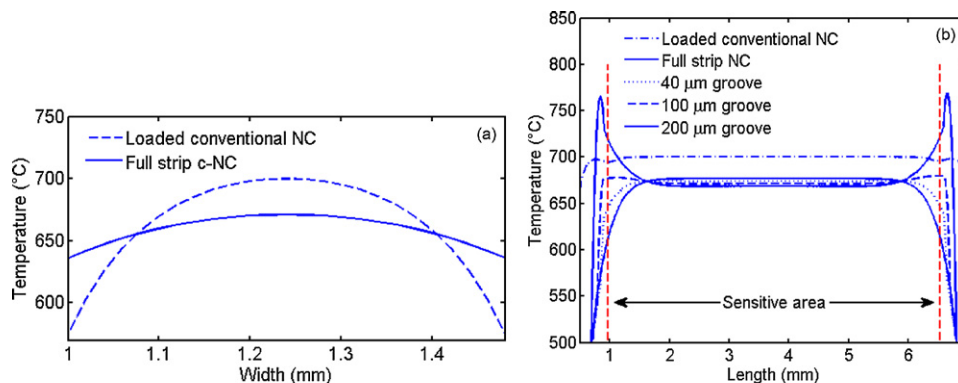

Fig. 12. Temperature profile in scanning mode along the direction (a) perpendicular to the strip and (b) parallel to the strip for nanocalorimeters with different geometries.

that the temperature profile along the middle of the strip is more uniform for a loaded conventional NC than for a full strip c-NC. This result is explained by the good thermal link induced by c-Si between the sensitive area and the NC frame that stays at RT. Nevertheless, calculating σ of the temperature over the whole sensitive area, we found 39 and 15 °C for the loaded conventional NC and full strip c-NC, respectively. This shows a significant improvement of temperature uniformity due to the c-Si acting as a thermal plate.

One could improve the thermal uniformity in either case by reducing the sensitive area along the axis where uniformity is poor. In the case of a c-NC that would correspond to moving the sensing contacts toward the center of the strip. The situation is more complicated in the case of a conventional NC since the main contribution to non-uniformity is the thermal losses in the SiN_x membrane in the direction perpendicular to the strip affecting the lateral temperature profile along the whole strip. A reduction of strip width does not improve the uniformity significantly because an increasing fraction of the total heat is lost by conduction to the membrane. One drawback in both cases is that the sensitivity of the device decreases with the reduction of the sensitive area.

Another way to improve the uniformity of a c-NC is to pattern two grooves (as shown in Figs. 1 and 3) on each end of the c-Si strip to decouple the sensitive area from the NC frame. The presence of grooves can have two opposing effects depending on their location and size. On the one hand, small grooves might not be efficient in preventing heat losses as a small spacing may lead to a steep temperature gradient in this region resulting in significant heat conduction through the membrane and Pt strip. On the other hand, large grooves will induce hot spots due to the low thermal mass of the grooves area compared to the zones covered with c-Si. Such hot spots increase the resistivity, thus increasing the dissipated power and the temperature. This may result in damaging the heating strip or having less heat delivered to the sensitive area. In order to optimize groove dimensions, we simulated the performance c-NC with groove widths ranging from 10 to 300 μm. The temperature profile along the strip for some relevant cases is reported in Fig. 12b. Profiles perpendicular to the strip (not shown) all have the same shape as the full strip geometry. At the particular heating rate (80 000 °C/s on average) investigated, uniformity improves with increasing groove size until around 100 μm where best uniformity is achieved with σ = 12 °C and a peak-to-valley (PV) value of 56 °C. This is an improvement with respect to the full strip geometry that yield σ = 15 °C and a PV value of 102 °C. For larger grooves such as 200 or 300 μm, the temperature uniformity deteriorates to σ = 14 and σ = 22 °C, respectively. In addition, potentially damaging temperature peaks occur in these cases, as seen at each end of the temperature profile (see, for example, the NC with a 200 μm groove in Fig. 12b). Simulation of more sophisticated designs with 2 and 3 grooves of different sizes did not yield significant improvement.

In order to investigate the influence of the heating rate on the thermal uniformity, we monitored the standard deviation σ as a function of temperature for different heating rates. In this set of simulations, different types of NCs are heated at heating rates ranging from 1.8×10^4 to 3.75×10^5 °C/s. The case where there is no material on the backside of the SiN_x membrane will be referred to as *unloaded conventional NC*. For simulating this NC, lower currents were used (roughly half) to compensate for the lower heat capacity and to achieve comparable heating rates. The results are summarized in Fig. 13 where σ is plotted as a function of the average heating rate during the scan. c-NCs clearly have better temperature uniformity over a wide range of heating rates. In contrast, σ for the loaded and unloaded conventional NC increases with increasing heating rate from 10^4 to 10^5 °C/s, reaches a maximum and decreases at higher heating rates. Keeping in mind that temperature variations along the direction perpendicular to the strip have a

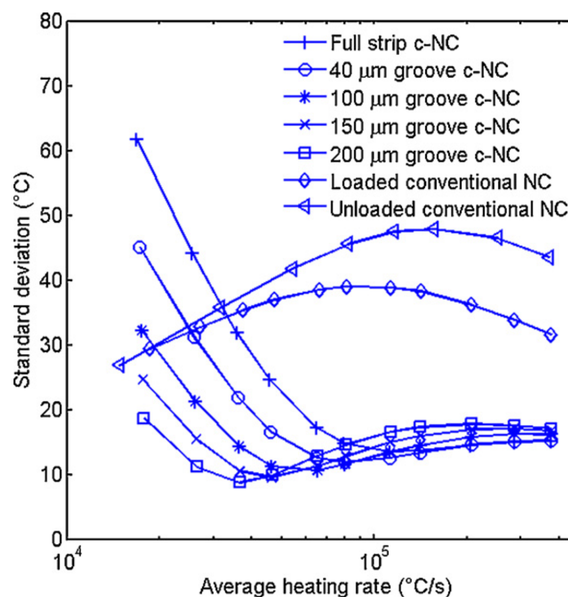

Fig. 13. Standard deviation of the temperature distribution vs. heating rate for conventional NCs and c-NCs with different geometries.

larger impact on σ since it affects the whole sensitive area (Fig. 12a), whereas variations along the strip usually affect a small fraction of the sensitive area (Fig. 12b), this trend can be understood as follows: at low heating rates, uniformity along the strip deteriorates because the heat has more time to leak along and through the Pt strip while uniformity in the direction perpendicular to the strip improves because the Pt strip has the time to act as a thermal plate. For higher heating rates the opposite occurs, uniformity along the strip is better because less heat escapes through the Pt strip and, laterally, through the membrane. On the other hand, Pt no longer acts as an efficient thermal plate that improves the uniformity perpendicularly to the strip. At very high heating rates, there is no time for thermal conduction and the uniformity starts to improve again.

In the case of c-NC, the picture is quite different. The silicon strip contributes about 20 times more to the heat conduction than the Pt strip does because it has about 3 times the conductivity of the Pt film and 7 times the thickness. Therefore, heat losses along the strip are large enough at low heating rates to induce temperature variations over a significant portion of the strip despite of its length. That explains the rather poor temperature uniformity at low heating rates for c-NC. Such an effect can be counterbalanced by the addition of grooves that are sufficiently wide to decouple the sensitive area from the silicon frame. In the direction perpendicular to the strip the thermal profile varies less with changing heating rates as compared to conventional NC.

In the full strip geometry the uniformity improves almost monotonously with increasing heating rate because of the shorter time available for heat losses. In the case of c-NC with grooves, σ passes through a minimum before rising to reach a plateau. The rise in σ from a certain heating rate is caused by the resulting hot spots as explained above. These hot spot only slightly degrade the temperature uniformity since the grooves are located outside the sensitive area. Despite small changes in σ, our simulations predict that these hot spots can reach temperatures up to 200 °C above the sensitive area average temperature. Experimental observations suggest that such hot spots can cause device failure.

It is important to point out that all simulations were carried out assuming a c-Si layer of 330 nm. Thinner c-Si layer will limit heat losses along the strip thus reducing the need to pattern grooves on each end. Meanwhile, thinner layers will be less efficient thermal plates, thus leading to degraded temperature uniformity in the

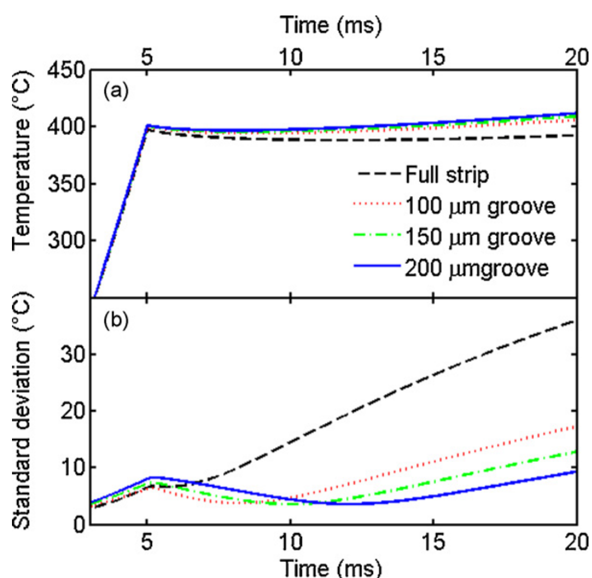

Fig. 14. Temperature evolution (a) and uniformity (b) as a function of time in isothermal mode. A 77 mA current is supplied for the first 5 ms and then decreased to 22 mA thereafter.

direction perpendicular to the strip. For the full strip geometry, our simulations show that the optimal strip thickness is from 300 to 400 nm for a standard heating rate of 80 000 °C/s.

6.2.2. Quasi-isothermal nanocalorimetry

Isothermal calorimetry is used to measure the heat released by a process as a function of time at a fixed temperature. This technique is particularly interesting for investigating kinetic processes. With NC devices, the procedure consists in quickly heating the calorimeter to a certain temperature and then to drastically reduce the current supplied to the calorimeter (within a few microsecond) in order to stabilize the temperature for a few tens of ms. Because of temperature uniformity and stability issues, we call this technique quasi-isothermal nanocalorimetry. We saw in Fig. 10 that thermal uniformity is worse in static mode as compared to scanning mode (Fig. 12). In this section we study the thermal uniformity as a function of time.

For the simulations presented in Fig. 14, a current of 77 mA is supplied to the simulated calorimeter during 5 ms in order to heat the calorimeter up to 400 °C. Then, a current of 22 mA is supplied during 15 ms for the temperature to stabilize within 10 °C. Fig. 14a shows the average temperature evolution as a function of time considering different types of NCs, while Fig. 14b presents the corresponding evolution of σ. In all cases, the temperature slightly decreases upon decreasing the heating current. This is followed by a slow increase over a time period of several milliseconds. This behavior arises as a result of a steep temperature gradient at the end of the initial ramp (Fig. 9), leading to high conductive losses and a temperature decrease. Eventually, the temperature profile smoothens making the conductive losses smaller, and the temperature starts to increase again. Considering the uniformity data in Fig. 14b it is clear that a c-NC design featuring no groove is not suitable for this type of measurement as σ increases continuously to reach 38 °C after 20 ms (Fig. 14b). The fact that the average temperature drops by 10 °C during that time indicates that heat losses are responsible for the increase in σ.

All c-NC with groove operated with the same current settings, follow the same general behavior. σ first exhibits a decrease at the end of the initial temperature ramp. This is followed by a small temperature increase (less than 5 °C) over a time period of 3–9 ms depending on the groove size dimension. As expected from the discussion of Fig. 12 in previous section the NC with the 100 µm groove exhibits the best performance following the initial ramp. However, over the complete 20 ms of the quasi-isothermal part of the experiment, the roles are inverted: the 200 µm groove NC ends with a better uniformity (σ = 10 °C) than the 100 µm one 18 °C. The fact that the presence of grooves improves σ and limits temperature variations highlights the importance of heat losses along the strip. The decrease in σ is due to heat diffusion within the sensitive zone which has a relatively short relaxation time since it is linked by c-Si. In other words, uniformity along the direction perpendicular to the strip gets better at the beginning of the measurement. The rise in σ at the end of the isotherm is due to the thermal link between the sensitive area and the silicon frame. They are linked by the membrane which has a much lower thermal conductivity and thus a longer relaxation time. This link induces temperature variations along the strip which is the main factor in the decrease of uniformity due to heat loss. The wider the groove, the larger the relaxation time for heat loss along the strip is, as reflected in Fig. 14b. The groove can thus be set to the value required to perform a specific experiment. However, large grooves lead to thermal spikes, so a best compromise has to be found.

6.2.3. Modeling nanocalorimetry signals

Our model, which realistically represents the NC behavior, can be used to simulate the voltage signals that one would measure in an actual experiment, assuming a certain process is occurring on the NC. This enables, for example, to discriminate between different types of kinetics by simulating the actual signals that would come out taking into account the influence of temperature non-uniformities and thermal losses. Additionally, the model can be used to test the data processing algorithm accuracy by feeding the algorithm with simulated voltage signals from a known heat release and comparing it to the result given by the algorithm. Furthermore, it allows simulating how certain parameters can influence the measurements, for instance what would be the influence on the signal if there was a misalignment of the sensitive area with the c-Si strip or deposited material.

7. Conclusion

We have presented the fabrication and characterization of a NC exhibiting an atomically flat and clean monocrystalline silicon strip aligned with the sensitive area of the device. The measurement of the melting of Al and the heat released by the recrystallization of ion-implanted Si confirm the functionality and accuracy of the device at high temperature. Based on these experiments the uncertainty on the temperature calibration is estimated to be below 20 °C around 660 °C and the thermal uniformity across the sensitive area is estimated to be better than 16 °C at 900 °C. A realistic finite-element model was developed and the simulations were compared to experimental data. Simulation of the device operation further allowed demonstrating that the Si strip forms a thermal plate which ensures better thermal uniformity when compared to conventional NCs. Additionally it was found that the optimal design of the Si strip depends on the heating rates used in the experiments. Although we only show results here on the temperature profile and uniformity in scanning and quasi-isothermal mode, the described model can be used in a much more general way to interpret experimental results with full account of the effects of the thermal losses on the measurements.

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